EX/EE/ET/T/214/2018

# BACHELOR OF ENGINEERING IN ELECTRICAL ENGINEERING 2ND YEAR 1ST SEM EXAMINATION, 2018

**ELECTRONICS – II** Time: Three hours Full Marks: 100

Use a separate Answer-Script for each Part

## PART-I (50 MARKS)

Answer *Q.1* and any *two* questions from the rest [10+2×20=50]

1. Answer any *five* from the following [5×2=10]
   a) What is tri-state logic?
   b) Draw the truth table of a NAND gate.
   c) What is literal?
   d) $(4C.A5)_{16}=(?)_{10}$
   e) Define Fan in and Fan out.
   f) How many select lines a 16 to 1 multiplexer have?
   g) What is the difference between latch and Flip-Flop?

2. a) What is the 2's complement binary number representation of +63 and -63. Use 7 bits. [4]
   b)Perform following subtraction [6]
   i) 11001-10110 using 2's complement ii) $(44)_H$-$(1B)_H$ using 16's complement
   c) State and prove De-Morgans' theorems. [5]
   d) Prove the following equations using the Boolean algebraic theorems:
   i) A + A' B + AB' = A + B [2+3]
   ii) A'BC + A B'C + ABC'+ ABC = AB + BC + AC

3. a) Define implicant, prime implicant and essential prime implicant. [5]
   b) Minimize the following logic function using K-maps and realize using
   F(A,B,C,D) = ∑m (1, 3, 5, ,8, 9,11,15) + d(2,13) [5]
   c) Implement the following function using i) 8 to 1 multiplexer ii) 4:1 Multiplexers
   F(A,B,C,D) = Π M(0,1,2,5,9,11,13,15) [5+5]

4. a) Design a Full adder using Half Adders. Design a Full adder using a suitable decoder. [4+4]

   b) Explain a full adder/subtractor circuit operation with help of a flow chart . [12]

5. a) Explain the operation of S-R Flip-Flop using NAND gate only. [6]

   b) Explain the operation of D flipflop. Use Preset and Clear for external control of initial state. [6]

   b) What is Race around condition in J-K flip-flop and how Master Slave combination helps to solve the problem? [8]

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B. E. ELECTRICAL ENGINEERING 2ND YEAR 1ST SEMESTER EXAMINATION, 2018

Subject: Electronics-II | Time: 3.0 Hours | Full Marks: 100

**Use separate Answer - Script for each Part**

**50 marks for each part**

**PART-II**

| No. of questions | Answer any **TWO (2)** questions from the followings: 2×25 | Marks |
|---|---|---|
| 1. | (a) What do you meant by an ***oscillator***?<br>(b) Classify the ***oscillators*** in accordance with ***frequency generation***.<br>(c)Explain the ***oscillator principle***.<br>(d) Give the circuit diagram of a ***Wien-bridge oscillator*** using ***OPAMP***. Explain how oscillation principle is satisfied in this circuit? How the frequency of oscillation is determined for such oscillator?<br>(b) Design a ***Wien-bridge oscillator*** that oscillator that oscillates at ***25 KHz***. Given that $C_1 = C_2 = 0.001\ \mu F$. | 2+3+5+(4+4+3) +4 |
| 2. | a) Distinguish between ***multivibrator*** and ***oscillator***.<br>(b) Mention the area of application of ***oscillator***?<br>(c) Gives the internal circuit diagram of ***IC 555*** and specify the components and devices are used.<br>(d) Explain the operation of ***Monostable multivibrator*** using ***555 IC*** with necessary circuit diagram.<br>(e) How ***IC 555*** can be used as a voltage controlled oscillator? | 4+3+(3+2)+(4+4) +5 |
| 3. | (a) Define a ***constant current*** and ***voltage source***. How a ***JFET*** can be used as ***constant current source***? Explain clearly with suitable circuit diagram and output characteristic.<br>(b) Give the block diagram of a voltage regulator and explain the function of each block. Describe how a ***transistorised shunt voltage regulator*** provides a steady state output voltage against the input voltage fluctuation?<br>(c) Calculate the current gain of Darlington pair transistor configuration with following data Beta (β) of one is transistor is 100 and another is 150. | 4+(4+6)+8+3 |
| 4. | (a) Explain the operation of a 2-input **CMOS NOR** gate with suitable circuit diagram.<br>(b) Draw a transistor transistor logic (TTL) circuit. Explain how the output of this circuit becomes high when one of the emitter inputs is low.<br>(c) Give the circuit diagram of IC 7805 voltage regulator. Explain the operation of this circuit. | 7+(4+5)+(4+5) |