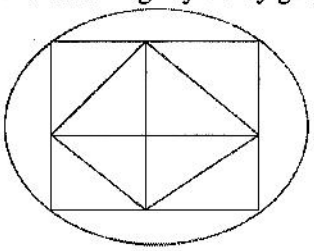
Bachelor of Computer Science and Engineering 4th Year Examination – 2018

Subject: VLSI Systems

Time : Three hours **Full Marks: 100**

Different parts of the same question should be answered together.

CO1 [10]	Answer any one from (a) and (b) in this block [1] (a) (i) Implement the Boolean function $f = ab + bc + cd$ using single complex cell designs in four different ways (consider that for any input, its complement is also available). (ii) Implement the Boolean function $f = ab + bc + cd$ =using CMOS NAND gates (consider that for any input, its complement is not available). 6+4 (b) (i) What is the significance of stick diagram, as applicable in the design of VLSI? What is its advantage and limitation? (ii) Draw the coloured stick diagram for implementing the following Boolean functions using CMOS : $g = (A + \bar{B} + D)(\bar{A} + BD)$ 5+5
CO2 [20]	[2] (i) What is semiconductor? (ii) What is Moore's Law? Why and how was it modified in 1975? (iii) Explain the basic processing steps in fabrication. (iv) What are the advantage and disadvantage of CMOS? (v) Explain VLSI design Cycle. [2+3+7+3+5]
CO3 [20]	*Answer any* **two(2)** from **(a), (b)and (c)** *in this block:* [3] (a) (i) Define sliceable and non-sliceable floorplan with examples. State with an example how a sliceable floorplan can be represented by a binary tree. (ii) Obtain the rectangular dual of the following adjacency graph below.  5+5 (b) (i) Explain the force directed placement algorithm. (ii) Explain the different procedures for Breuer's Algorithm. 4+6 (c) What is the concept of simulated annealing? How is it applied in floorplanning and placement? 10
CO4 [10]	*Answer any* **one(1) from (a) and (b)** *in this block:* [4] 10 (a) State Kernighan-Lin algorithm for partitioning. The following matrix provides 4 modules a,b,c,d with their entries representing the number of connections between the two modules. Apply Kernighan-Lin heuristic to obtain the partitioning. (b) What are the drawbacks of Kernighan-Lin algorithm? Present the Fiduccia-Mattheyses Algorithm. Find out its time complexity.
CO5	*Answer any* **two(2)from (a), (b) and (c)** *from this block:*

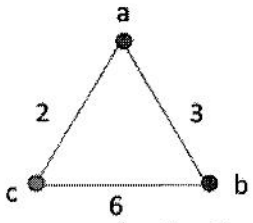
	a	b	c	d
a	0	1	2	3
b	1	0	1	4
c	2	1	0	3
d	3	4	3	0

[40]

[5]

(a) (i) Consider a hypergraph H, where each hyperedge interconnects at most three vertices. We model each hyperedge of degree-3 with three edges of weight ½, on the same set of vertices, to obtain a weighted graph G. Prove that an optimal balanced partitioning of G corresponds to an optimal balanced partitioning of H.

(ii) Consider the following adjacency graph of following Figure below where the edge weights are providing the distance between two vertices. Estimate the routing cost in different sliceable floorplans.



(iii) State the various approaches for placement problem- Top-down, iterative, constructive.

[7+7+6]

(b) (i) What are the objectives of Routing? What are constraints of routing?

(ii) Explain Global Routing and Detailed Routing.

(iii) Give an example or counter example as the case may be for the following statement: Soukup's maze router always produces the shortest path.

(iv) Route the following channel of 11 columns using the Left edge algorithm, where 0 indicates an empty Position.

TOP = 3 4 0 1 2 4 3 5 2 1 0

BOT = 1 0 3 0 4 0 5 2 1 4 5

4+4+5+7

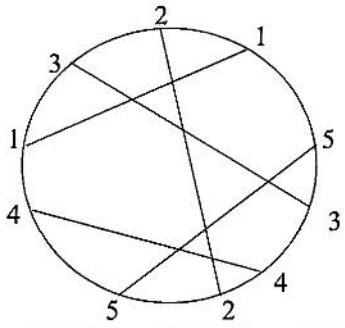
(c) (i) What is digleg in routing? Use Dogleg router to to route the following channel.

1 0 0 3 0 2 0 1 0 3 0 4 1 2 0 3 0 4 5

0 2 1 3 0 4 0 2 0 5 0 5 0 4 0 3 4 1 0

(ii) Explain the via minimization problem.

(iii) Get the solution for unconstrained via minimization for the following graph.



[10+2+8]