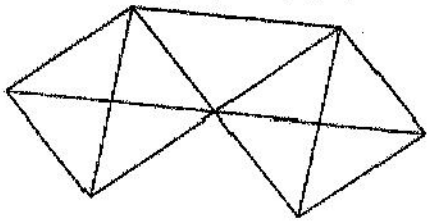
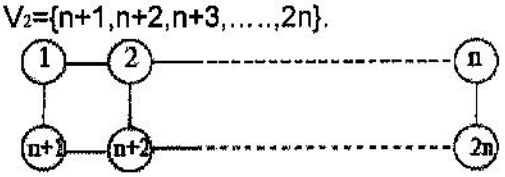
Bachelor of Computer Science and Engineering 3rd Year 1st Semester (old) Examination – 2018

Subject: VLSI Design

Time : Three hours **Full Marks: 100**

Different parts of the same question should be answered together.

CO1 [10]	Answer any one from (a) and (b) in this block [1]
	(a) (i) Explain Bipolar junction transistor. Explain its three modes of operation. How does it act as an amplifier? How does it act as a switch?
	(ii) Implement the Boolean function $f = ab + bc + cd$ =using CMOS NAND-NAND gates (consider that for any input, its complement is not available). 6+4
	(b) (i) What is the significance of stick diagram, as applicable in the design of VLSI? What is its advantage and limitation?
	(ii) Draw the coloured stick diagram for implementing the following Boolean functions using CMOS : $g = (A + \bar{B} + D)(\bar{A} + BD)$ 5+5
CO2 [20]	[2]
	(i) How do you define LSI and VLSI?
	(ii) What is Moore's Law? Why and how was it modified in 1975?
	(iii) What is photoresist? Explain its use in fabrication process.
	(iv) What are the advantage and disadvantage of CMOS? How does CMOS work as an inverter?
	(v) Explain VLSI design Cycle. [2+3+4+6+5]
CO3 [20]	*Answer any* **two(2)** from **(a), (b)and (c)** *in this block:*
	[3]
	(a) (i) Define sliceable and non-sliceable floorplan with examples. State with an example how a sliceable floorplan can be represented by a binary tree.
	(ii) Obtain the rectangular dual of the following adjacency graph below.
	 5+5
	(b) (i) Explain the force directed placement algorithm.
	(ii) Explain the different procedures for Breuer's Algorithm. 4+6
	(c) What is the concept of simulated annealing? How is it applied in floorplanning and placement? 10
CO4 [10]	*Answer any* **one(1) from (a) and (b)** *in this block:*
	[4] 10
	(a) State Kernighan-Lin algorithm for partitioning. Show how the Kernighan-Lin Heuristic works on the ladder graph with 2n vertices, starting with initial partition of $V_1 = \{1,2,3,\ldots\ldots,n\}$, and $V_2 = \{n+1, n+2, n+3, \ldots\ldots, 2n\}$.
	
	(b) What are the drawbacks of Kernighan-Lin algorithm? Present the Fiduccia-Mattheyses Algorithm. Find out its time complexity.

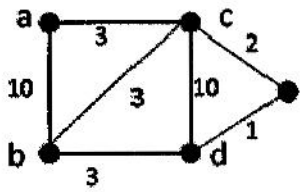
CO5 [40]

Answer any **two (2)from (a), (b) and (c)** *from this block:*

[5]

(a) (i) Consider a hypergraph H, where each hyperedge interconnects at most three vertices. We model each hyperedge of degree-3 with three edges of weight ½, on the same set of vertices, to obtain a weighted graph G. Prove that an optimal balanced partitioning of G corresponds to an optimal balanced partitioning of H.

(ii) State the steps in hierarchical floorplan with bottom-up greedy procedure for the following adjacency graph with nodes having same weights.



(iii) State the various approaches for placement problem- Top-down, iterative, constructive.

[7+7+6]

(b) (i) Define routing problem. What are different routing regions?

(ii) Define Channel, terminal switch with respect to routing.

(iii) Explain Global Routing and Detailed Routing.

(iv) Route the following channel using the Left edge algorithm, where 0 indicates an empty Position.

TOP = 3 4 0 1 2 4 3 5 2 1 0

BOT = 1 0 3 0 4 0 5 2 1 4 5

4+5+4+7

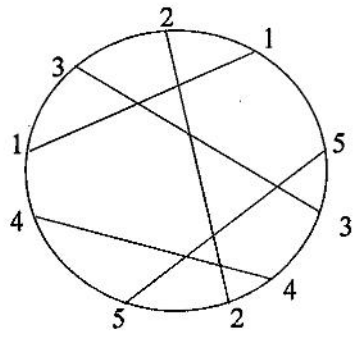
(c) (i) What are the drawbacks of left edge algorithm? How are they tackled in dogleg routing?

TOP = 1 1 2 3 2

BOT = 2 0 0 0 3

(ii) What is via? Explain the via minimization problem.

(iii) What are constrained and unconstrained via minimization? Get the solution for unconstrained via minimization for the following graph.



[7+4+9]