BACHELOR OF COMPUTER SC. ENGG. EXAMINATION, 2018

(2nd Year, 1st Semester)

Digital Circuits

Time : Three hours | Full Marks : 100

Answer any ***five*** questions

(a) What is semiconductor? In the light of energy band theory, explain semiconductor, metal, insulator.

(b) Explain Ideal diode equation. Let V_σ =0.75V is the voltage across a diode when it is in saturation. Let us consider that the current which is 1% of the current corresponding to V_σ, the diode becomes just forward biased at the corresponding voltage be V_γ. Calculate V_γ at room temperature where nkT/q=0.026V at room temperature T, k= Boltzman constant, n= emission coefficient.

(c) What is σ for transistor? How does it vary in active and saturation region?

(d) How does the transistor act as a switch? Explain CE, CC and CB mode for the transistor to work as switch. Which mode is better for switch and why?

5+7+2+6

(a) Compare bipolar transistor versus Junction field effect transistor.

(b) How do you compare FET, enhancement type NMOS, depletion type NMOS with respect to operating point?

(c) How is CMOS working as a switch?

(d) Prove that the ratio of impedances Z_{pu} and Z_{pd} of the pull-up to pull-down transistors of an nMOS inverter is 4 :1.

3+5+3+9

(a) What is the disadvantage of Diode logic?

(b) Consider the following circuit (Fig. 1). The voltage across the diode is 0.75 when forward biased. Deduce the voltage at C for 4 different combinations of A and B and each such combination for three different values of R_L – (i) α (infinity), (ii) 500 Ω and (iii) 1 KΩ. From the results conclude the logic performed by it.

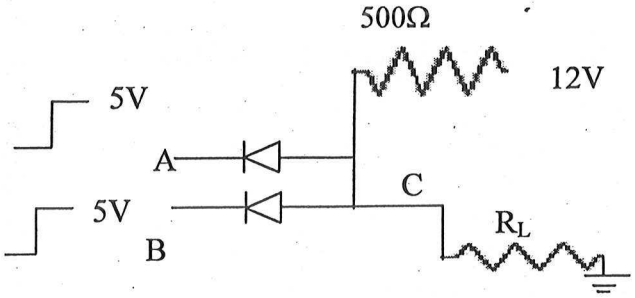

Fig. 1

(c) Explain the operation of a DCTL gate. Explain the current hogging problem.

2+10+8

(a) Draw the two inputs AND gate using RTL. Explain its operation.

(b) What is the output of parallelization of RTL gates.

(c) Consider the circuit (Fig.2) in next page. The voltage across the diode is 0.75V when forward biased. The base emitter junction voltage of the transistor during saturation and active mode are 0.75V and 0.70 respectively. Deduce the voltages at Base and Collector of the transistor for 2 different combinations of Input and each such combination for four different values of R_L – (i) α (infinity), (ii) 100 Ω (iii) 500Ω and (iii) 1 KΩ. From the results conclude the logic performed by it.

(d) In Fig.2, what will be the base voltages for two different combinations at input, if -12V is changed to +5V.

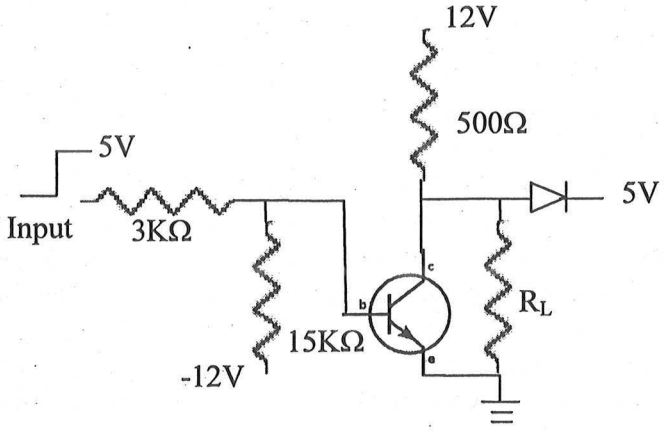

Fig. 2

5+2+9+4

5. (a) Draw an IIL gate. What is the advantage of IIL gate? Why is IIL gate called merged-transistor logic?
   (e) With the help of a circuit diagram explain the operation of a DTL gate.
   (f) How is the circuit of DTL modified for integrated version? What are its advantages over the discrete version?

6+7+7

6. (a) Draw HTL gate. What is its advantage over DTL?
   (b) Calculate the number of fan-out of HTL gate.
   (c) Explain the operation of a TTL NAND gate. Compare DTL and TTL.
   (d) Explain - why is TTL having more speed?

6+4+7+3

7. (a) What is the common problem of RTL, DTL and TTL gates?
   (b) Explain the operation of an ECL gate. What is its advantage?
   (c) Implement a four-word, four-bit ROM using diode and resistances for the following encoder with I1,I2,I3,I4 as inputs and Z1,Z2,Z3,Z4 as outputs.

I1	I2	I3	I4	Z1	Z2	Z3	Z4
0	0	0	1	1	0	1	1
0	0	1	0	1	1	1	0
0	1	0	0	1	1	0	1
1	0	0	0	0	1	0	1

   (d). With reference 7(c), show the implementation of Z3 using transistor and resistance.

3+6+8+3

8. (a) What is the use of Sample-Hold circuit?
   (b) Design a 3-bit successive approximation A/D converter. Explain its operation.
   (c) Explain the operation of a R-2R ladder type DAC.

3+10+7