BACHELOR OF COMPUTER SC. ENGG. SUPPLEMENTARY EXAMINATION, 2018

(2nd Year, 1st Semester)

Digital Circuits

Time : Three hours | Full Marks : 100

Answer any ***five*** questions

1. (a) Why Si, Ge are semiconductors?
   (b) Explain Ideal diode equation. Let V =0.75V is the voltage across a diode when it is in saturation. Let us consider that the current which is 1% of the current corresponding to V , the diode becomes just forward biased at the corresponding voltage be V . Calculate V at room temperature where nkT/q=0.026V at room temperature T, k= Boltzman constant, n= emission coefficient.
   (c) For an npn transistor with emitter grounded draw the I_c versus V_{CE} characteristics. Show the saturation region. Generally the term 'saturation' implies something becoming constant, which one is becoming constant here and with respect to whom?
   (d) How does the transistor act as a switch? Explain CE, CC and CB mode for the transistor to work as switch. Which mode is better for switch and why?

   3+6+5+6

2. (a) Explain MOSFET. What are the advantages of MOSFET over JFET?
   (b) Compare the transfer characteristics in JFET, depletion type MOSFET, enhancement type MOSFET.
   (c) How is CMOS working as a inverter?
   (d) Prove that the ratio of impedances Z_{pu} and Z_{pd} of the pull-up to pull-down transistors of an nMOS inverter is 4 :1.

   3+5+3+9

3. (a) What is the advantage of Diode logic?
   (b) Consider the following circuit (Fig. 1). The voltage across the diode is 0.75 when forward biased. Deduce the voltage at C for 4 different combinations of A and B and each such combination for three different values of R_L – (i) α (infinity), (ii) 500 Ω and (iii) 1 KΩ. From the results conclude the logic performed by it.

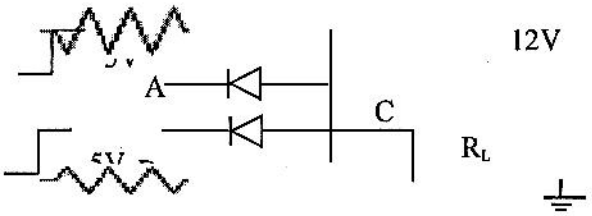

Fig. 1

   (c) Explain the operation of DCTL gate. Explain input-output characteristics of a DCTL gate.

   2+10+8

4. (a) Explain the operation of a RTL NOR gate.Explain its input-output characteristics.
   (b) Consider the circuit (Fig.2) in next page. The voltage across the diode is 0.75V when forward biased. The base emitter junction voltage of the transistor during saturation and active mode are 0.75V and 0.70 respectively. Deduce the voltages at Base and Collector of the transistor for 2 different combinations of Input and each such combination for four different values of R_L – (i) α (infinity), (ii) 100 Ω (iii) 500Ω and (iii) 1 KΩ. From the results conclude the logic performed by it.
   (c) In Fig.2, what will be the base voltages for two different combinations at input, if -12V is changed to +5V.

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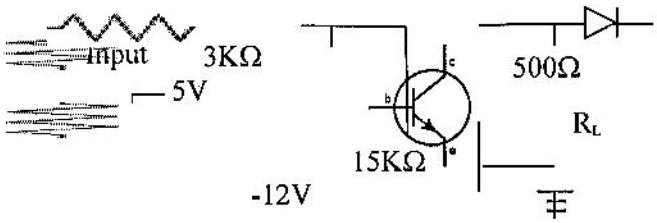

Fig. 2

7+9+4

5. (a) What problems of RTL and DCTL gates are solved in IIL gates?
   (b) Explain the input-output characteristics of DTL gate. Show the noise immunities in its characteristics.
   (c) Explain the propagation delay in case of a DTL gate.
   (d) Calculate the number of Fan-out in DTL gates.

4+6+5+5

6. (a) With the help of a circuit diagram explain the operation of a HTL gate.
   (b) What is the advantage of HTL gate over DTL?
   (c) Explain Multi emitter transistor in case of TTL gates.
   (d) Explain the input-output characteristics of TTL neglecting input transistor.

6+4+4+6

7. (a) What is the advantage of ECL gate over other gates ?
   (b) Explain the transfer characteristics of an ECL gate. Find the noise margins in this characteristics.

   (c) Implement a four-word, four-bit ROM using diode and resistances for the following encoder with I1,I2,I3,I4 as inputs and Z1,Z2,Z3,Z4 as outputs.

I1	I2	I3	I4	Z1	Z2	Z3	Z4
0	0	0	1	1	0	1	1
0	0	1	0	1	1	1	0
0	1	0	0	1	1	0	1
1	0	0	0	0	1	0	1

   (d). With reference 7(c), show the implementation of Z3 using MOS transistor and resistances.

3+6+8+3

8. (a) What is the use of Sample-Hold circuit?
   (b) Design a 3-bit successive approximation A/D converter. Explain its operation.
   (c) Explain the operation of a R-2R ladder type DAC.

3+10+7