B.E. COMPUTER SCIENCE AND ENGINEERING

SECOND YEAR FIRST SEMESTER SUPPLEMENTARY EXAM - 2018

Subject: Computer Organisation

Time: 3hrs **Full Marks:** 100

Answer any **five**

Answer all the sub-parts of a question in *adjacent* location

1	Compare the following (any five):		5x4
	a.	Fan-in vs. Fan-out	
	b.	Combinational circuit vs. Sequential circuit	
	c.	LRU vs. FIFO	
	d.	RISC vs. CISC	
	e.	2-address machine vs. 3-address machine	
	f.	Access time vs. Cycle time	
2	a.	Describe with an example the design aspect of Carry Look Ahead adder.	10
	b.	With the help of circuit diagram explain the design issues of Serial-Parallel adder.	10
3	a.	With a suitable example show how modified Booth's algorithm works.	10
	b.	Write down the working principles of associative and set-associative cache memory-mapping techniques.	10
4	a.	Describe the implementation issues of *Wilkes'* design to develop microprogrammed control unit.	10
	b.	Discuss the restoring and non-restoring division algorithms for unsigned integer.	10
5	a.	Discuss the different design issues of a basic liner-pipeline processor.	6
	b.	Define the pipeline classification scheme according to the Ramamoorthy and Live.	4
	c.	What are possible solutions of the different kinds of data and control hazards?	10
6	Write short note on the following (any two)		2x10
	a.	Nan-programming	
	b.	Content addressable memory	
	c.	Virtual Memory	