Ref. No.:Ex/CSE/T/225A/2018

B.E. COMPUTER SCIENCE AND ENGINEERING SECOND YEAR SECOND SEMESTER -2018
COMPUTER ARCHITECTURE

Time: Three Hours **Full Marks:100**

Group-A

Answer twenty-eight (28) questions. **$28 \times 3 = 84$**

Choose the unique correct answer

For Q1..Q4.:
A pipelined processor has five stages: IF,ID,EX,MEM,WB. The register file is accessed for reading in ID, and for writing in WB. Register writes are performed in the first half of a clock cycle and register reads are performed in the second half of a clock cycle.

Now consider the following instruction sequence:

```
DADD   R1, R2, R3
DSUB   R4,R1,R5
AND    R6,R1,R7
OR     R8,R1,R9
XOR    R10,R1,R11
```

Suppose the instructions are issued in consecutive clock cycles, starting with cycle-1 when DADD is issued.

1.DSUB executes
(a) correctly
(b) incorrectly

2. AND executes
(a) correctly
(b) incorrectly

3.OR executes
(a) correctly
(b) incorrectly

4. XOR executes
(a) correctly
(b) incorrectly

For Q5..Q7:
In the 5-stage pipeline of Q1..Q4 above, consider the execution of the following instruction sequence:

```
LD      R1, 0(R2)
DSUB    R4, R1,R5
AND     R6,R1,R7
OR      R8, R1,R9
```

Suppose no stall is inserted and instructions are issued in consecutive cycles,starting with the issue of the LD instruction in cycle-1.

5. To operate correctly,the DSUB instruction
(a) needs forwarding
(b) does not need forwarding
(c) can never operate correctly

6. To operate correctly, the AND operation
(a) needs forwarding
(b) does not need forwarding
(c) can never operate correctly

7. To operate correctly, the OR operation
(a) needs forwarding
(b) does not need forwarding
(c) can never operate correctly.

For Q8..Q10:
Consider a multiprocessor using write-back invalidation protocol with snooping cache coherence. Consider a memory location X with value 0. Two CPUs A and b generate the following sequence of events:

Event name	Event
E1	CPU A reads X
E2	CPU B reads X
E3	CPU A writes a 1 to X
E4	CPU B reads X

Of course, each event will initiate some bus activity and cache read/write. Assume that initially X is not cached by A or B. In the following, we consider the state of the system after the bus activity resulting for the named event.

8. After E1, CPU A's cache contains
(a) 0
(b) 1
(c) some unknown value

9. After E2, CPU B's cache contains
(a) 0
(b) 1
(c) some unknown value

10. After E3, the memory location X contains
(a) 0
(b) 1
(c) some unknown value

---

11. Consider a multiprocessor having an interconnection network (rather than a bus) and implementing directory-based cache coherence. Processor P incurs a write-miss at address A. A message is then sent from the local cache to the home directory. The function of the message is to
(a) request data and make P the exclusive owner
(b) request data and make P a shared reader
(c) invalidate a shared copy of data at address A
(d) none of the above

12. The path actually taken by a message to reach its destination is determined by
(a) flow control
(b) routing
(c) topology
(d) none of the above

13. An interconnection network is said to be non-blocking if
(a) it never allows a message to be dropped
(b) it has very large buffers at each node
(c) it can handle all circuit requests without any conflicts (shared channels)
(d) none of the above

14. A 4×5 crossbar switch can be implemented with
(a) 5 4:1 multiplexers
(b) 4 5:1 multiplexers
(c) 1 4:5 multiplexer
(d) none of the above

For Q15..Q16:
Consider a (m=3, n=3, r=4) symmetric Clos network. The naming is specified below:

Entity	Name
Input switch	S1..S4
Middle switch	M1..M3
Output switch	D1..D4
Input port	x.y (y-th input of Sx; y= 1..3 x = 1..4)

Output port	p.q (q-th output of Dp; q = 1..3, p = 1..4)
Connection	(input port – output port)

Routing from (x.y) to (p.q) is specified as (x,m.p) implying that it passes through Sx, Mm, Dp.

15. The desired connections are {(1.1-3.2), (1.3-4.3), (2.1-1.2)}. This can be achieved by the routes
(a) (1,1,3), (1,1,4), (2,2,1)
(b) (1,4,3), (1,3,4), (2,4,2)
(c) (1,2,3), (1,2,4), (2,2,2)
(d) (1,2,3), (1,3,4), (2,1,1)

16. The desired connections are {(2.1-4.3), (2.3-1.1), (3.1-2.2), (4.1-1.2)}. This can be achieved by the routes
(a) (2.1.4), (2,2,1), (3,3,2), (4,2,1)
(b) (2,1,4), (2,1,1), (3,2,2), (4,2,1)
(c) (2,3,4), (2,4,1), (3,3,2), (4,3,1)
(d) (2,3,4), (2,3,1), (3,4,2), (4,3,1)

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17. Network resources are allocated to packets rather than messages because
(a) messages are in ASCII format
(b) messages may be arbitrarily long
(c) packets can travel over any type of hardware
(d) none of the above

18. The basic unit of routing and sequencing is a
(a) flit
(b) message
(c) packet
(d) phit

19. The basic unit of bandwidth and storage allocation is
(a) flit
(b) message
(c) packet
(d) phit

20. In a distributed memory MIMD architecture
(a) each PE can freely access the memory of any other PE
(b) no PE can ever access the memory of any other PE directly
(c) memory is logically shared but physically distributed
(d) none of the above

21. Static networks are typically used in
(a) multiprocessors
(b) multicomputers
(c) vector processors
(d) none of the above

22. Dynamic networks are typically employed in
(a) multiprocessors
(b) multicomputers
(c) vector processors
(d) none of the above

23. Scalable MIMD architectures are necessarily based on
(a) shared memory
(b) distributed memory
(c) cache memory
(d) single-bus architectures

24. Intensive data copying can result in significant performance degradation in
(a) multiprocessors
(b) multicomputers
(c) both multiprocessors and multicomputers
(d) none of the above

25. Complex synchronizing constructs are needed in
(a) multiprocessors
(b) multicomputers
(c) pipelined architectures
(d) none of the above

26.In centralized arbitration of a bus, a requesting master gains control of the bus
(a) immediately after activating its request
(b) if the bus busy line is passive
(c) if the grant line is active
(d) none of the above

27. In a daisy-chained grant scheme for bus arbitration
(a) each master has its own request line
(b) requests are also daisy-chained
(c) there is only one shared bus request line
(d) none of the above

28. In a daisy-chained grant scheme for bus arbitration, if a master, which does not require the bus, receives an active grant line, it
(a) activates its output grant line
(b) stops propagation of the grant line
(c) activates the bus busy line
(d) none of the above

29. In a decentralized rotating arbitration method, an arbiter grants its coupled master if
(a) the master has activated its bus request line
(b) the bus busy line is passive
(c) priority input line is active
(d) all of the above

30. In the MESI protocol, if a cache in the E(exclusive) state gets a PrWr request, it
(a) moves to the I state
(b) moves to the M state
(c) moves to the S state
(d) remains in the E state

31. In the MESI protocol, if a cache in the S (shared) state observes a BusRdX bus transaction, it moves to the
(a) E-state
(b) I-state
(c) M-state
(d) S-state

32. In the MESI protocol, if a cache in the I-state observes a PrRd transaction from the processor, it moves to
(a) E-state if 'shared' signal is inactive
(b) S-state if 'shared' signal is active
(c) both (a) and (b)
(d) none of the above

33. Consider a multiprocessor employing a directory-based cache coherence. If a node incurs a read-miss to a block, it first
(a) sends a read request to the owner node which provides the data
(b) sends a read request to the home node which provides the data
(c) sends a read request to the directory
(d) none of the above

34. The instruction sequence

```
load    r1,a
add     r2,r1,r1
```

exhibits
(a) RAW dependence
(b) WAR dependence

(c) WAW dependence
(d) no dependence

35.The instruction sequence

```
mul   r1,r2,r3
add   r2,r4,r5
```

exhibits
(a) RAW dependence
(b) WAR dependence
(c) WAW dependence
(d) no dependence

Group-B

36. Consider a superscalar processor with two(2) execution units. Each execution unit can execute any operation. However, at most one of the instructions issued in a cycle could be a memory (load or store) operation, and at most one of the instructions could be a non-memory operation. Load operations have a latency of 3 cycles, and other operations have a latency of 2 cycles. (The latency between an instruction I_1, and an instruction I_2 dependent on I_1, is the time-delay (cycles) between their issue cycles.) Each processor has a 6-stage pipeline [IF(Fetch instruction),ID(Decode instruction), RR(Read registers), EX(execute, 2 cycles), WB (write result back into registers)]. Instructions cannot be executed out-of-order (i.e., the instructions cannot be reordered). Now consider the following instruction sequence:

```
-------------------------
LD    r4, (r5)
LD    r7,(r8)
ADD   r9,r4,r7
LD    r10,(r11)
MUL   r12,r13, r14
SUB   r2,r3,r1
ST    (r2), r15
MUL   r21,r4,r7
ST    (r22),r23
ST    (r24),r21
-------------------------
```

How long would the program take to issue ?

(An instruction is said to have issued when it passes from the RR stage to the EX stage). **16**