Ref. No.: **EX/CSE/T/115A/2018(S)**

B.C.S.E. 1^{st} Year, 1^{st} Semester Supplementary Examination, 2018
Digital Logic

Full Marks: 100 Time : 3 Hr

Answer all questions (Q1 - Q3). Write answers to the point and state all the assumptions (wherever required).
ALL PARTS OF THE QUESTION SHOULD BE ANSWERED TOGETHER

Q 1) Attempt **all** questions (1a - 1k) (40)

(a) Convert the following $(1100101010)_2$ to octal, decimal and hexadecimal format (3)

(b) Convert the following decimal number, $(347)_{10}$ to binary, octal and hexadecimal formats (3)

(c) Perform the following addition: $(FFF)_{16} + (A34)_{16}$ (2)

(d) Perform the following subtraction using two's complement $(1101011)_2 - (111010)_2$ (2)

(e) Represent $(28)_{10}$ in binary form using : $(2 \times 2 = 4)$
(i) BCD Code (ii) Excess-3 Code

(f) Describe about the standard representation for logical functions. (4)

(g) Explain the operation of NAND and NOR gates using figures and truth-tables. Why are these gates important in digital electronics (5)

(h) Design 3 to 8 line decoder. (4)

(i) What is Race-around problem? How can you rectify it? (5)

(j) Compare combinational and sequential logic circuit. (4)

(k) Explain the operation of a JK flip-flop. (4)

Q 2) Answer any **two** questions $(2 \times 20 = 40)$

(a) (i) **Make a K-Map for the following function and consequently minimize it:** (10)

$$f = AB + A\overline{C} + C + AD + A\overline{B}C + ABC$$

(ii) Design the full subtractor using NOR gates only. (5)

(iii) Explain the working of bi-directional shift registers. (5)

(b) (i) Convert the following 30_{16} to binary. Show each step clearly. (3)

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(ii) Perform the following: 555 − 332 using 9's complement Binary Coded Decimal (BCD) subtraction. (4)

(iii) A four-variable Boolean function is given by

$$F = A.B.C + B.C.D + A.\overline{C}.D$$

and

$$\phi = \{A.B.\overline{C}.\overline{D}, A.\overline{B}.C.D, \overline{A}.\overline{B}.C.D\}$$

is a **don't-care** function. Using a Karnaugh map or otherwise :

(I) Find the simplest sum of products expression for F. (5)

(II) Design a circuit to implement F using NAND gates only (4)

(III) Design a circuit to implement F using NOR gates only. (4)

(c) (i) State the logic circuit, truth table and derive the equivalent logic expression from the truth table of the following Boolean expression $Y = A\overline{B} + \overline{B}C$ $(3 + 4 + 3 = 10)$

(ii) Explain the operation of a left/right shift register. Use diagrams to explain the operation. (10)

Q 3) Answer any **two** question $(2 \times 10 = 20)$

(a) Solve the following using Quine-McCluskey Method

$$F(A, B, C, D) = \Sigma(23, 7, 9, 11, 13) + \Sigma\phi(1, 10, 15)$$

(b) Design a 3 bit binary DOWN counter.

(c) Design a digital circuit for generating a sequence $1 - 3 - 5 - 7 - 1 - 3 - 5 - \ldots$. Give its corresponding timing diagram