Ex./PG/PE/T/113B/2018

Master of Power Engineering First Semester 2018
Digital Systems

Time 3 hours Full Marks 100

All questions carry equal marks

Answer any Five

1. Formulate the state transition diagram for a 4 bit parallel down counter starting with a initial state of 1111. Design the counter using the state transition diagram formulated.

   Calculate the maximum clock frequency at which a serial 8 bit counter can operate if the propagation delay for each F/F is 40ns..

   5+10+5

2. With the help of a neat schematic, deduce an expression for frequency and duty cycle of a 555 Timer as an a stable multi-vibrator. Hence design a circuit to produce a 5 KHz. pulse train and compute its duty cycle. **15+5**

3. Define fan-in, fan-out and Threshold Voltage for a logic gate.
   Assuming representative values compute the following:
   (i) fan-out of a TTL gate
   (ii) noise margin of a TTL gate
   With a supply of 5V for both design a suitable circuit to interface the output of a TTL gate to a CMOS date. **6+14**

4. Deduce the z-transform of $x(n) = (0.5)^{(n-5)}u(n-5)$ where $u(n-5)$ is 0 for $n < 5$ and 1 otherwise. Compute the ROC. Deduce any formula used by you.

   Obtain $G(z) = \frac{y(z)}{u(z)}$ using the difference equation $y[n] - 0.5y[n-1] = 2.5u[n]$

   15+5

5. Deduce a transformation between the s plane and z plane using bilinear transformation and hence deduce a map of the stable region of the s plane in the z plane. **10**.
   How does a pole at $z = -5$ appear in the s plane? **10**

6. Starting from Fourier Series representation of a function $X(t)$ derive its Fourier Transform $X(\omega)$. Find the Fourier .Transform of a causal exponential function $f(t) = e^{-at}$

   5+5

7. What is the conversion time for a 12 bit Successive Approximation ADC.driven by a 1 MHz. clock? Draw its transfer characteristics assuming that the MSB is a sign bit. And calculate its resolution if the supply voltage is ±5V dc. **4+6**

Design a 3 bit Flash ADC and represent it by a schematic **4**
With suitable approximations for quantization error compute the improvement of Signal to Noise Ratio(SNR) due to addition of a single bit in a ADC. **6**

8. Define star, bus and ring topologies of interconnection of digital systems and hence represent a standard topology for a SACA used in industrial applications. If star topology implemented using an n port M Mbps switch, what should be the bandwidth of the switch.. **10**

Deduce the electrical signal for a bit string 10110110 communicated from the sender to the receiver over a standard RS-232C line. Compute the bit wise efficiency if a 8 bit no parity frame is used with 2 stop bits. **2+4**

How is the bit string represented using Manchester coding" **4**