Ref. No.: Ex/PG/ETCE/T/128D/2018

Department of Electronics and Telecommunication Engineering, Jadavpur University

M. E Electronics and Telecommunication Engineering 1st year 2nd semester Examination 2018.

Attempt any five questions and all question carry equal mark. The figures in the right hand margin indicate marks. *Symbols carry usual meaning.*

Time : Three hours Subject : VLSI Design Full Marks: 100

Q1. a). Why low power has become an important issue in the present day VLSI circuit realization?

b). Draw the ideal characteristics of a CMOS inverter and compare it with the actual characteristics. What is noise margin? Find out the noise margin from the actual characteristics of an inverter. 8+12 =20

Q2. (a) What is body effect? How does it influence the threshold voltage of a MOS transistor?

(b) What is transconductance of a MOS transistor? Explain its role in the operation of the transistor. What are the various ways to reduce the delay time of a CMOS inverter?

(c) What is short circuit power dissipation? On what parameters does it depend? Justify the statement; "there is no short circuit power dissipation in a static CMOS circuit if Vdd < (Vtn + |Vtp|)".

(d) What is subthreshold leakage current? Briefly discuss various mechanisms responsible for this leakage current? (4 + 7 + 5 + 4 =20)

Q3. (a) How the transfer characteristic of a CMOS NAND gate is affected with increase in fan-in?

(b) Calculate the threshold voltage of a MOSFET based NAND Gate converted to Inverter when V_{DD}=1.2V, μ_n=570cm^2/V-S, μ_p=190cm^2/V-S, Wp=2Wn, Ln=Lp, V_{tn}=$|V_{tp}|$=0.35V.

(c) Write the expression for the equivalent threshold voltage of a NOR Gate when it is converted to an inverter. Explain the expression and the VTC curve of the converted inverter. (4 + 8 + 6 = 20)

Q4. (a). What are high and low –skewed logic gates? Explain GDI logic with an example.

(b). Implement two-input (i) XOR and (ii) NOR gates with GDI logic. Explain their operations.

(c). Explain pseudo and Ganged CMOS logic. (6+ 8 + 6 =20)

Q5. (a) Compare the constant field and constant voltage scaling approaches in terms of area, delay, energy and power density parameters.

(b) How can you combine sizing and supply voltage scaling to realize low power circuits?

(c) Why leakage power is an important issue in deep submicron technology? (12 + 5 + 3 = 20)

Q6 (a) Explain the problems associated with the resistive load inverter and probable solutions. Why Depletion load inverter is better?

(b) Describe CMOS design constraints.

(c) Draw a two input XOR/ XNOR CMOS Gate and explain its operation. (9 + 5 + 6= 20)

Q7. A problem deals with the design of a control unit for a simple coin operated candy vending machine. The candy cost 3 Rs. and the machine accepts 2 Rs and Rs 1 coins. Change should be returned if more than 3 Rs. is deposited. No more than 4Rs. can be deposited on a single purchase; therefore, the maximum change is one Rs. A block diagram of the candy machine is given in fig A. The control unit has two inputs N and D which are outputs of the coin detector. The coin detector generates a 1 on signal N if a 1Rs coin is deposited and a 1 on signal D if a 2Rs. coin is deposited. The N and D lines automatically reset to 0 on the next clock pulse. We shall assume that it is physically impossible to insert two coins at the same time, and therefore we cannot have N=D=1 in the same clock period. The control unit has two outputs R and C. The candy is released by a 1 appearing on signal R. The state of the control unit represents the total amount of money deposited for the current purchase. Design this candy machine control unit. 20Marks

Q8 Write notes on any four 5x4 = 20

(a) limitation of contemporary CAD tools (b) transmission Gate based XOR Gate (c) an area optimized transmission Gate based full adder (d) Ganged CMOS logic (e) Non-threshold Logic