Ref No . Ex/PG/ETCE/T/129F/2018

MASTER OF ENGINEERING IN
ELECTRONICS & TELE-COMMUNICATION ENGINEERING EXAM -2018

(First Year, 2nd Semester)

ELECTRONIC DESIGN AUTOMATION (ED)

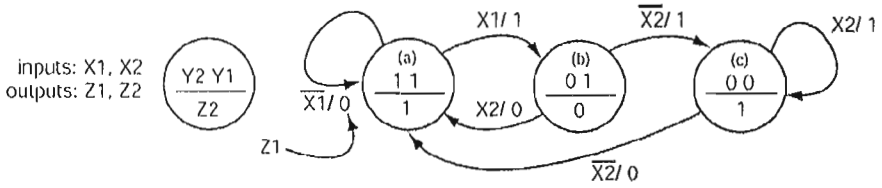
Time : Three Hours **Full Marks : 100**

Answer any four questions.

1.

a. What is test bench? Write test bench program to verify XOR gate . **2+8=10**

b. Write the VHDL code of following FSM **8**



c. Explain with example about multiple processes? **7**

2.

a. What is delta delay in VHDL? How Transport and inertial delays are described? **4+6= 10**

b. Design a 8:1 MUX using suitable MUX tree. Write the code using structural model. Use process for input sensitivity list. **8**

c. Write a program of 3 bit ripple counter by using structural model. **7**

3.

a. What is resolved signal? Write a short code to describe the resolution function **2+8=10**

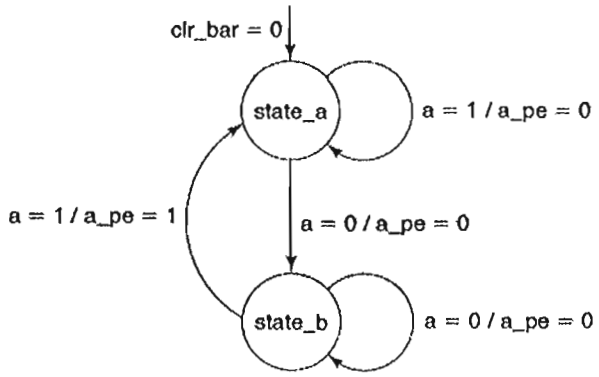
b. Write the VHDL code for a 7 segment decoder where an additional input blank that override the BCD input and cause all the segments blank **7**

c. Write a program of n input OR gate. **8**

4.

a. Write the VHDL code of Mealy FSM state diagram for a positive edge detector.

12



b. Write a code on 3 bit ring counter **6**

c. Write a program of single bit magnitude comparator in VHDL with proper circuit. Write proper syntax and there is no restriction on logic gate usage.

7

5.

a. Explain the MOS small signal model and describe MOS capacitor. **10**

b. What is SPICE Level -1 model what are the primary net-list parameters? **7**

c. What is the difference between full custom and semi custom ASIC. How the design load affects in structured gate array? **4+4=8**

6.

a. What is design for manufacturability? What is different process variation and how it changes the device, circuit and system? **10**

b. What are the designable and noise parameters and how the distribution function of noise behaves? **8**

c. What is parametric yield? Why Different model is required for performance verifications? **7**

7.

a. What are the operational process in Floor planning and Placement? **8**

b. What are the differences between global and detailed routing? **6**

c. What is response surface model (RSM)? Explain the factorial design method for a three parameter design. **5+6 =11**