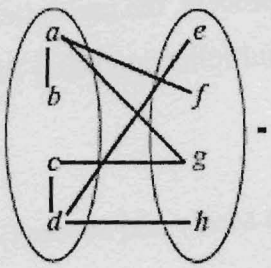
M. E. (ELECTRICAL) EXAMINATION, 2018
(2nd Semester)

SUBJECT: - DESIGN AND APPLICATION OF EMBEDDED SYSTEMS

Full Marks 100

Time: **Three hours**

No. of Questions		Marks
	Answer any five.	
1.		
	a) Explain the advantages of multiple threshold CMOS logic gate.	6
	b) Compare the performances of the Look up table type and the static CMOS gate type logic elements with suitable example.	6
	c) Explain the operation of Anti-fuse. Also describe how the anti-fuse can be programmed to configure the programmable interconnect system.	8
2.		
	a) Discuss the differences among Carry Save adder, Carry Look ahead Adder and Carry select adders, showing necessary functional diagrams. Also compare the delays for these types of adders.	6
	b) Illustrate the design of Wallace Tree Multiplier. Explain how it speeds up the multiplication process.	8
	c) In a multiplication process, the multiplicand is -5 and multiplier is 2. Show the steps of multiplication using Booth algorithm.	6
3.		
	a) Distinguish between Mealy and Moore type finite state machines with suitable examples.	5
	b) Consider a two phase sequential system in which all the combinational logic are connected between the output of the latches and the inputs of the latches.	
	(i) Draw a block diagram of such system.	

	(ii) Draw two such systems, connected so that the outputs of one feed the inputs of the next. Does this system satisfy the two phase clocking requirements? Explain.	5
	c) A unit control process in a elevator system has the state names as i) Going Up, ii) Going down , iii) Idle and iv) Door open . Draw state diagram, declare all necessary variables, and list all possible transitions and actions. Write down the sequential program for Program Models of Unit control.	10
	If two states are added as Fire Going Down and Fire Door Open, then draw a state diagram adding hierarchy.	
4.		
	a) Explain the purpose and goals of logic optimization. What are the methods of Logic synthesis?	5
	b) A Boolean function is given as : $Y = a.b + a.c + b.c$ Represent each SOP term as cube with on and off sets .Also represent the Boolean function as set of cubes or covers.	5
	c) Partition a circuit using **Kernighan–Lin** algorithm, into two parts, such that every node is within a prescribed range and number of connections among the nodes is minimized. Show the cost of reduction in each iterative step.	10
		
5.		
	Compare: a) Control unit of general-purpose processor and single-purpose processor. b) One-Time programmable switch (OTP) and Re-Programmable (RP)	4x5 =20

	switch. c) Programmable Logic Array (PLA) and Programmable Array Logic (PAL) d) Princeton Architecture and Harvard Architecture.	
6.	a) A watchdog timer has been constructed using a prescaler, an overflow register 'scalereg' and a time-count register 'timereg' connected in cascade in usual sense. It is intended to generate a timeout signal of 2 minute based on an input clock frequency of 12MHz. Design an appropriate watchdog timer to carry out the task as mentioned above. Explain your solution with appropriate schematic diagram. b) Configure an LCD controller to display a group of characters '**123**' on LCD screen. Draw required schematic diagram representing hardware connection and explain the steps of your program.	10 10
7.	Write short notes on any *two*: i) Application-Specific Instruction-set Processors (ASIPs). ii) Addressing modes of generalized processors. iii) Sub-operations in instruction cycles.	10+10
8.	a) What is a JTAG port? Discuss in brief the functions of its pin-outs and the role of the port as a whole. b) What is a macrocell? How does a macrocell contribute to the versatility of a processor? Explain with an example.	10 10