Jadavpur University
B.Power Engg.3rd Year 2nd Semester Examination 2023
Microprocessors & Microcontrollers

Time: 3hrs
Full Marks 100

Answer All Questions

1. **Evaluate the following**
   a. **Express the following**
   (i) $(4124)_{10}$ and $(-2283)_{10}$ using a signed 2Byte Hexadecimal representation
   (ii) $(-1562)_{10}$ in 2s complement binary notation
   (iii) $(56.24)_{10}$ in binary form using a fixed point and an exponent form representation (4+2+4) CO(1)
   b. **Compute the following using suitable binary representations**
   (i). $(112)_{10} + (43)_{10}$
   (ii). $(13)_{10} - (28)$　　　　　　　　　　　　　　　　　　　　　　　　　　　　10 CO(1)

Or

Derive the schematic representation of a 4 bit parallel Counter　　　　　　20 CO(1)

2. Represent the functioning of a Full Adder with Carry using a Moore Machine. If this FSM is used to add two Binary numbers A=$(1101)_2$ and $(1011)_2$ what is the final state of the FSM at the end of computation and what are the outputs corresponding to this state.　　　　12+8 CO(2)

Or

   (i) Name the different General Purpose registers in a 8085 Micro-processor.
   (ii) A micro-processor has a 16 bit data bus and 20 bit Address Bus. Compute its General Purpose Register size and its Memory Size.
   (iii) With a suitable timing diagram represent the RD cycle of a 8085 Micro-processor.
　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　(4+6+10)CO(2)

3. Write an Assembly Language program for a 8085 Microprocessor to add 10 consecutive unsigned 8 bit integers, with the starting number represented in Hexadecimals by the last two digits of your exam roll number and stored in 10 consecutive locations starting from 2000H and store the result in location 2020H.　　　　　　　　　　　　　　　　　　　　　　20 CO(2)

Or

With suitable assumption of data already loaded in the memory, write a program to sort 10 8 bit numbers in descending order　　　　　　　　　　　　　　　　20 CO(2)

4. Enumerate the different types of Machine Cycles in a 8085 Microprocessor
   Design a Memory System with Address Decoding Logic for an 8085 Microprocessor for a 32K Memory System with 8K×1 Memory Chips and derive the chip select logic　　6 +14 CO(3)

Or

If the content of the HL register pair is 0x2030,
   (i)　　What does the following code segment MVI M 0x25 do?
   (ii)　　How many Machine Cycles (and which ones) does the Instruction require and in which sequence?
   (iii)　　How many Bytes in Memory does it require?　　　　　　4+4+2 CO(3)

   Enumerate the different Hardware Interrupts in a 8085 Microprocessor and state their Activation Logic (Level and/or Edge Triggered). With a neat schematic show the functioning of RST 7.5 Interrupt
　　　　　　　　　　　　　　　　　　　　　　　　　　　　　4+6 CO(3)

5. (i) With a neat schematic represent a Wave-Drive, Full-Drive and Half-Drive mode of operation of a Stepper Motor with 4 coils A,B,C,D.　　　　　　　　　　　10 CO(4)

   (ii) Derive the base addresses for Port A, Port B, Port C and CR of an 8255 with IOCS$_2$ used for Chip Select and represent the interface with a suitable schematic.　　　10 CO(4)

Or

   Assuming than an API for Keil C programming environment exists write a C-program to control the stepper motor of 5(i) in wave-drive mode.　　　　　　　　　　10 CO(4)