Ref. No.: Ex/IEE/PE/B/T/324A/2023

B. INS. & ELEC. ENGINEERING 3RD YEAR 2ND SEMESTER EXAMINATION 2023

ANALOG MOS CIRCUIT DESIGN

TIME: 3 HOURS **FULL MARKS: 100**

List of Course Outcomes (CO):

CO1: Classify and analyze different types of MOS amplifiers (K4, A1-recognize)

CO2: Explain and interpret the importance of differential amplifiers (K3, A1)

CO3: Describe and explain the behavior of current mirrors (K2, A1)

CO4: Explain and analyze the frequency response of MOS amplifiers (K4, A1)

Instructions to the Examinees:

- Each module is mapped with the corresponding CO
- Attempt questions from **ALL** the modules
- Alternative questions exist within a module, not across the modules
- Different parts of same question should be answered together
- Clearly state any assumption and derive the necessary equation(s) for calculation
- Unless otherwise stated, use the device data shown in Table I and assume $V_{DD} = 3\ V$ where necessary

Table I

Symbol	Value	Unit
$V_{th,n}$	0.7	V
$V_{th,p}$	-0.8	V
γ_n	0.45	$V^{1/2}$
γ_p	0.4	$V^{1/2}$
$\mu_n C_{ox}$	50	$\mu A/V^2$
$\mu_p C_{ox}$	25	$\mu A/V^2$
λ_n	0.1	V^{-1}
λ_p	0.2	V^{-1}

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MODULE 1

(ATTEMPT **Q. NO. 1** AND ANY **THREE** FROM THE REST)

1. Fill in the blanks with **most appropriate** answer:

   (a) n-MOS is fabricated on _ _ _ _ _ substrate.

   (b) _ _ _ _ _ is identified as second order effect in MOS device.

   (c) MOSFET biased in _ _ _ _ _ region can be used as a current source.

   (d) For a constant drain current, variation of trans-conductance with the overdrive voltage follows a _ _ _ _ _ curve.

   (e) Source-body potential difference _ _ _ _ _ the threshold voltage of MOS.

   (f) Equivalent resistance of a diode connected MOSFET is _ _ _ _ _ proportional to trans-conductance.

   (g) Common-source stage with current source load _ _ _ _ _ the gain of the amplifier.

   (h) Drain current becomes a linearized function of input voltage in _ _ _ _ _ common source amplifier.

   (i) Common source stage followed by a common gate stage is fondly known as _ _ _ _ _ stage.

   (j) Output resistance of source follower is _ _ _ _ _ than that of common source stage.

   1X10=10

2.

   (a) What do you mean by trans-conductance of MOSFET? Find out the expression for trans-conductance in saturation region of operation in a MOSFET.

   (b) Plot the variation of trans-conductance as a function of drain to source voltage when the MOSFET is driven by a constant gate voltage.

   (2+3)+5

3.

   (a) Considering the second order effects, draw and explain small-signal model of an n-MOS.

   (b) Prove that for a MOS device: $g_{mb} = \eta g_m$, where the symbols enjoy their usual significances.

   5+5

4. Calculate the voltage gain of a degenerated common-source amplifier with $\lambda \neq 0$ *and* $\eta \neq 0$. Hence, find out the simplified expression for gain when both of the second order effects are ignored.

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5. Sketch v_{out} versus v_{in} for the circuit in Fig. 1 as v_{in} varies from 0 to V_{DD}. Identify the important transition points.

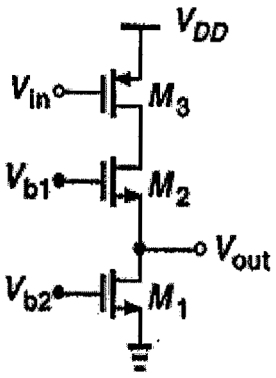

Fig. 1

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6. For a common-gate amplifier with $W/L = 50$ *and* $\lambda = 0$, calculate the maximum value of the source resistance. Find out the value of the voltage gain under this condition. Maximum power rating of the MOS is provided as 1.5 mW.

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MODULE 2

(ATTEMPT **Q. NO. 7** AND ANY **TWO** FROM THE REST)

7. Select **one or more** correct option(s) from the choices given below:

(a) Tail current source in differential amplifier is added in order to

(i) Suppress the effect of input common-mode level variations

(ii) Suppress the variation of trans-conductance of both the MOSFETs

(iii) Maintain the maximum allowable output swings

(iv) Suppress the variation of output common-mode level

(b) Input common-mode level of a differential amplifier is limited by

(i) Upper bound only

(ii) Lower bound only

(iii) Both upper and lower bound

(iv) A fixed value

(c) For a differential amplifier, a common-mode change at the input introduces a differential component at the output when

(i) The tail current source provides a finite output impedance

(ii) There is a mismatch between the properties of two MOSFETs

(iii) The drain supply is not constant

(iv) All of the above

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8.

(a) What do you mean by differential signal?

(b) Mention few advantages of differential amplifier over a conventional amplifier.

(c) Draw and explain the large signal transfer characteristics of a differential amplifier.

2+3+5

9. Show that the equivalent G_m for a differential amplifier falls to zero for $|\Delta v_{in}| = \sqrt{\frac{2I_{ss}}{\mu_n C_{ox}\frac{W}{L}}}$, where the symbols enjoy their usual significances.

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10. Due to a manufacturing defect, a large parasitic resistance has appeared between the drain and source terminals of M_1 in Fig. 2. Assuming $\lambda \neq 0$ and $\gamma \neq 0$, calculate the small signal gain of the amplifier circuit.

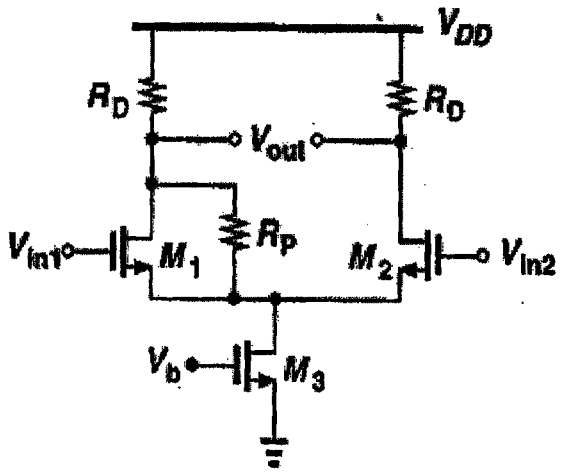

Fig. 2

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11. A differential pair uses input NMOS devices with $W/L = 100$ and a tail current of 0.5 mA. What is the maximum allowable output voltage swing if $V_{in,CM} = 1.2\ V$? What is the voltage gain under this condition?

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MODULE 3

(ATTEMPT **Q. NO. 12** AND ANY **TWO** FROM THE REST)

12. Select **one or more** correct option(s) from the choices given below:

(a) Current mirror circuits can be constructed using

(i) n-MOS only

(ii) p-MOS only

(iii) Both n-MOS and p-MOS in the same circuit

(iv) Both n-MOS and p-MOS in different circuits

(b) Cascode current mirror circuit is used to

(i) Suppress the effect of channel length modulation

(ii) Improve the voltage headroom

(iii) Minimize the requirement of MOS transistors

(iv) Reduce the power consumption

(c) Active current mirrors are those which

(i) Carry bias current only

(ii) Carry time varying current

(iii) Do not carry any current through it

(iv) None of the above

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13. Consider the circuit in Fig. 3. Assuming I_{REF} to be ideal, sketch I_{out} vs V_{DD} as V_{DD} varies from 0 to 3 V.

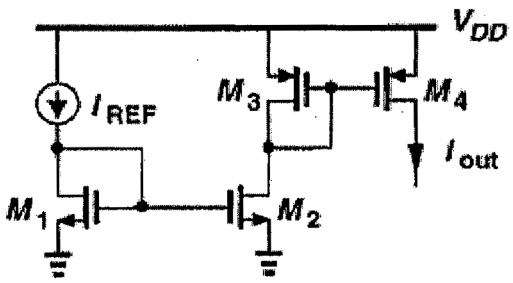

Fig. 3

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14. Draw and explain the operation of a cascode current mirror circuit. Hence, illustrate on accuracy-voltage headroom trade-off in the design.

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15. Assuming perfect symmetry, sketch the output voltage of the circuit in Fig. 4 as V_{DD} varies from 3 V to 0. Assume that for $V_{DD} = 3\ V$, all of the devices are saturated.

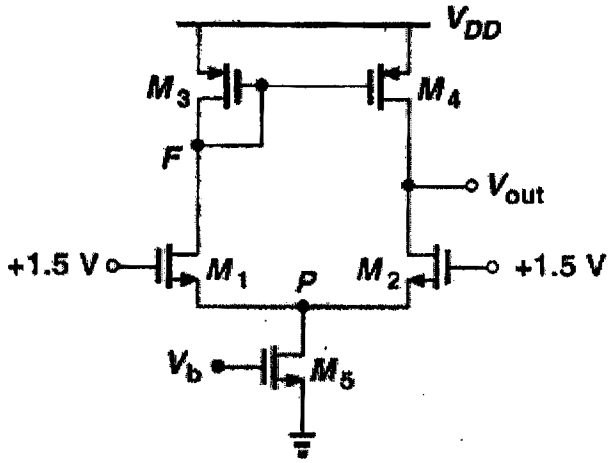

Fig. 4

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MODULE 4

(ATTEMPT ANY ONE FROM THE FOLLOWING)

16. Calculate the output impedance of a common source amplifier circuit driven by a resistive load.

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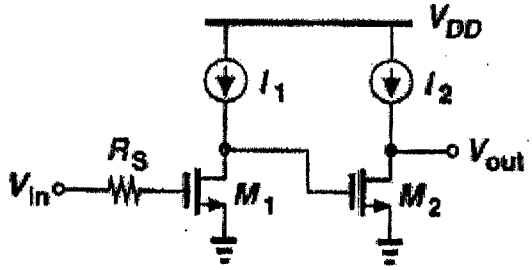
17. Estimate the poles of the circuit in Fig. 5 below.



$\lambda \neq 0$

Fig. 5

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