Bachelor of Instrumentation and Electronics Engineering, 2023
2nd year, 1st semester
DIGITAL ELECTRONICS

Time : Three hours **Full Marks : 100**

ANSWER ALL MODULES

Module – I (4 Marks)

Q1. What decimal number corresponds to the binary pattern **10100110**, when it is in

(a) **Excess-3 BCD** format, (b) **2's complement** format, (c) **sign-magnitude** format, and

(d) **Gray** format. (4)

Module – II (6 Marks)

Q2. Perform the following arithmetic operations :

(a) **(-25) + (-121)** using **8-bit 2's** complement number system.

(b) **(963) + (3086)** using Excess-3 BCD numbers.

Represent the final results in decimal. (3+3)

Module – III (40 Marks)

(Answer Q3 and ANY ONE from Q4 and Q5)

Q3. (a) Why are **CMOS transmission gates preferred** over both **n-MOS and p-MOS pass transistors** for connecting signals to a bus ?

(b) Draw the circuit of a **2-input TTL NOR** gate with totem-pole output.

(c) Draw the CMOS circuit to realize a **Full-Subtractor**. (5 + 5 + 10)

Q4. (a) Use **Karnaugh Map** technique to obtain the minimized expressions for the following functions as indicated :

(i) **F(W, X, Y, Z) = W'Y'Z' + WX'Y' + XY'Z + W'X'Y' + WX'Z + W'XZ' + WXYZ'**; using **only NAND** gates

(ii) **F(A, B, C, D) = ∏M(2, 5, 7, 8, 13, 15) + d(0, 1, 4, 10)**; in **minimized SOP** form

(iii) **F(A, B, C, D) = ∑m(3, 4, 5, 7, 9, 13, 14, 15)**; in **minimized POS** form

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(b) In **Positive Logic** certain logic circuit corresponds to the function

f = AB′C + A′BC+ AB′

What will be the expression of the output from the same logic circuit in **Negative Logic** ?

(3 x 5 + 5)

Q5. (a) Using **one** 8:1 Multiplexer and **one** 2:1 Multiplexer **(if needed)**, realize the following function :

F(W, X, Y, Z) = W′X′Z′ + WX′ + WX′Y′ + X′Y

(b) Realize a **3-input Priority Encoder** using a suitable **PROM** of **minimal configuration** and necessary **logic gates in minimum number**. Explicitly mention the priority order chosen for the inputs and corresponding output codes. **Draw** the **necessary diagram.** (10 + 10)

Module – IV (50 Marks)
(Answer Q6 and and ANY ONE from Q7 and Q8)

Q6. (a) The circuit shown in **Fig. P6(a)** represents a certain **3-bit counter**. **Initial state** of this counter is $Q_2Q_1Q_0$ **= 000**. Draw **the state transition diagram** for this counter. What is the **modulus of this counter** ? Can this counter face **lock-out problem** ? Establish your answer. (10 + 1 + 4)

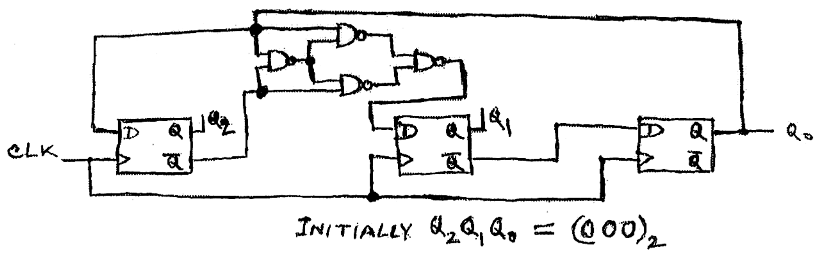

Fig. P6(a)

(b) For the circuit shown in Fig. **P6(b)** realize and draw the **State Transition Diagram.** Input to the circuit is **A** and the output is **Z.** Is it a **Moore** machine **or** a **Mealy** machine ? (9+1)

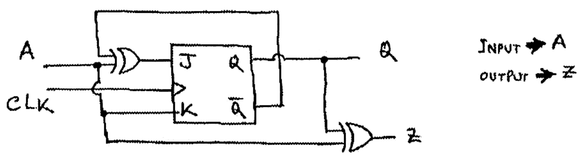

Fig. P6(b)

Q6. (c) Design a **2-bit** synchronous **binary down counter**. Use **T-FFs** as memory elements. (5)

Q7. Design a **Sequence detector** which detects the presence of input sequence "**11**" and **sets the output to logic 1 state**. The output is **reset again** by the presence of a "**00**" sequence. Use **D-FFs** as memory elements. Is there **any lock-out possibility** in your design ? Justify.

(18 + 2)

Q8. (a) Design a sequence generator which generates the sequence "**100110**" repeatedly. Use minimum number of **D-FFs**.

(b) Using **SR-FF** as memory element, realize a sequential **Gray to Binary** code converter. The input Gray bits are **coming serially starting from the MSB**. (10 + 10)

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