BE Instrumentation and Electronics Engineering, 2nd Year 1st Semester Supplementary Examination 2023

DIGITAL ELECTRONICS

Time : **Three hours** Full Marks : **100**

Answer *ALL* questions from ***GROUP-A*** and ***ANY THREE*** from ***GROUP-B***

GROUP - A

Q1. (a) A Mod-3 counter is cascaded with a Mod-5 counter as shown in Fig. P1(a). What is the modulus of the resulting counter ? Identify the count states ($Q_4Q_3Q_2Q_1Q_0$) in a tabular form.

(b) With the help of an example, explain how the occurrence of overflow in 2's complement arithmetic is detected. Design a logic circuit for this overflow detection.

(10 + 10)

Q2. (a) Use Karnaugh Map technique to obtain the minimized expressions for the following functions as indicated :

(i) $F(W, X, Y, Z) = \prod M(1, 4, 6, 7, 9)$; **in minimized SOP form**

(ii) $F(A, B, C, D) = AB'D + A'B'D' + AB' + B'C$; **in minimized POS form**

(iii) $F(A, B, C, D) = \prod M(3, 4, 5, 6, 7, 9, 13, 15)$; **in minimized NAND-NAND form**

(b) In **Positive Logic** certain logic circuit corresponds to the function **F = AB'C + A'BC'+ BC**. What will be the expression of the output from the same logic circuit in **Negative Logic** ?

(5 + 5 + 5 + 5)

GROUP - B

Q3. Design a sequence generator which generates the sequence "110101" repeatedly. Use minimum number of D-FFs. Draw the circuit diagram.

(20)

Q4. Design a MOD-6 synchronous UP-DOWN counter. It has a mode control input X. When X = 1, the counter counts in the upward direction and when X=0, it counts in the downward direction. Use D-FFs as the memory elements.

(20)

Q5. Design a synchronous sequential machine that detects the input sequence "101" without overlapping. Use T-FFs as the memory elements.

(20)

Q6. (a) Using one 8:1 Multiplexer and one 2:1 Multiplexer (if needed) realize the following function :

$$F(W, X, Y, Z) = WXZ' + W'X'Z' + W'X + X'Y$$

(b) Realize a T-FF using one SR-FF as the memory element.

(12 + 8)

Q7. Write short technical notes on : (4 x 5)

(a) Use of tri-stated TTL logic.

(b) Switched-tail ring counter.

(c) Race-around problem in JK Latch.

(d) Use of NAND gate as Universal Logic Gate.

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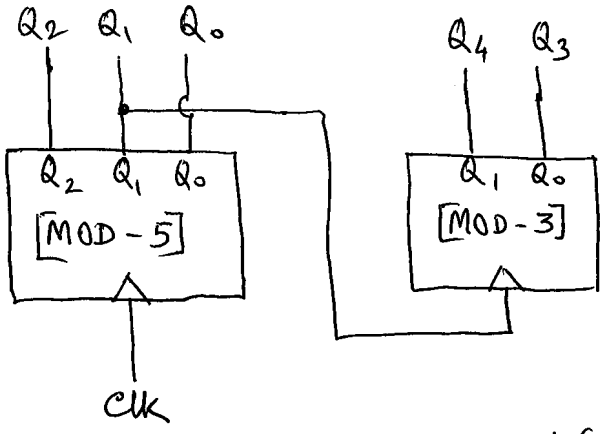

FIG - P1(a)