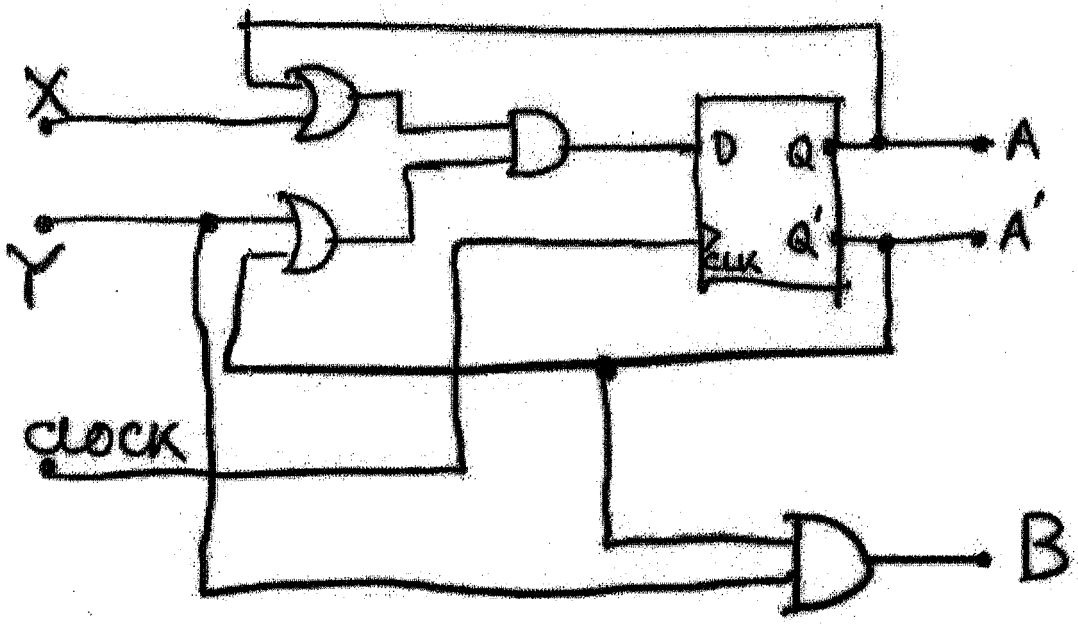
BE INFO TECH 2nd YEAR 1st SEMESTER EXAMINATION, 2023

Computer Organization and Architecture

Time: 3 Hours Full Marks: 100

Answer All 10 Questions

1.a) Study the following sequential circuit. Write down the Equation, State Table and State Diagram of this circuit.



b) Write a short note on USB. (6+4)[CO1]

2.a) With proper examples, explain Booth Multiplier.

b) Using proper examples explain Overflow Conditions while performing Integer Arithmetic. In your examples, please use both positive and negative numbers. (6+4)[CO2]

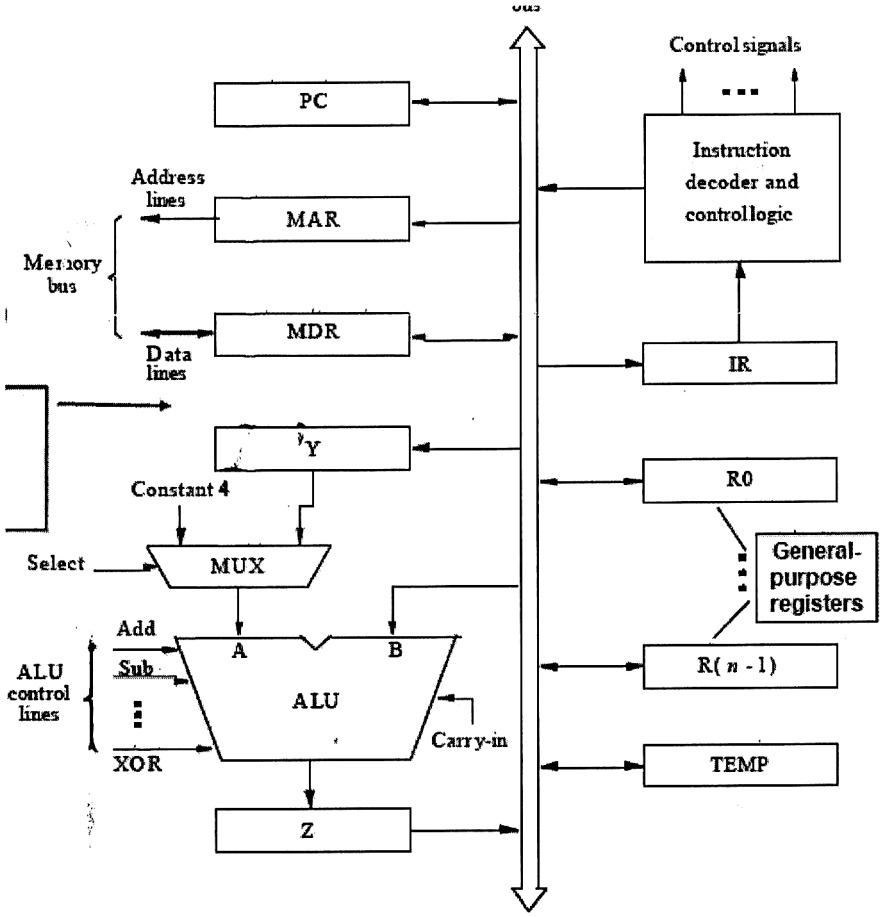
3.a) With proper examples, explain different types of IEEE 754 Rounding Modes.

b) With proper examples, show how two IEEE 754 Floating Point Number (Single Precision) can be added.

c) Show the range of numbers which can be represented using IEEE 754 Double Precision Floating Point Numbering System. (4+4+2)[CO2]

[Turn over

4.a) With respect to the diagram shown below, write down and explain the complete sequence of micro-operations performed by the CPU to execute the instruction "Add (R4), R3, (R2)" [((R4)+R3)-->(R2)].



b) Explain the various methods of generating control signals by the CPU to execute instruction. (7+3) [CO3]

5.a) Write down the sequence of instructions needed to evaluate the expression "X=A+B*C+D" for a Three-Address, One-Address and Zero-Address instruction format CPU.

b) The memory locations 100, 200 and 300 contain 200, 300 and 100 respectively. What will be the contents of the CPU registers R1 after executing the Assembly Language Instructions "Mov #300, R1; Add (100), R1". Justify your answer.

c) Write a short note on "Encoding of Machine Instruction". (3+3+4) [CO3]

6.a) List down the "Typical Characteristics of a Classic RISC CPU".

b) With proper examples and diagrams, explain how Pipelining is done in a RISC CPU. (5+5) [CO3]

7.b) Using 16Kx4 memory device, realize a byte addressable Memory System of 128 Kbyte. Please do a neat drawing of all the necessary circuits.

c) With proper examples and diagrams, explain the concept of Memory Interleaving.

d) With regard to the 4 way set associative mapping cache (byte addressable memory); the size of the cache is 16KByte, the size of one Cache block is 32Byte and the size of the memory 256 Kbyte. What will be the size of the TAG field and the Set field (in bits)? Justify your answer. (3+4+3) [CO4]

8.a) An approximate specification of a Toshiba P300 Hard Drive (HDWD130 3.5") is given below.

No of Surfaces = 6
Individual Sector Size = 4096 byte
No of Sectors per track = 256
Average No of tracks per surface = 345078
Rotational Speed = 7200RPM
Maximum seek time = 20ms
Average seek time = 10ms
Track-to-track seek time = 2ms

What is the capacity of the Disk?

b) With respect to the disk mentioned above, what will be the total time required to read the entire disk one cylinder at a time? [Assume that the starting position of the Read/Write Arm is at outer most track]

c) If 8 disks (of 1TB each) are arranged in a RAID configuration of Level 0, 1, 4, 5 and 6 successively; what will be the total usable capacity for each of these configurations? Justify your answer. (3+4+3) [CO4]

9.a) Draw HyperCube Network of depth 1, 2, 3 and 4. For each case compute Diameter and Bisection width.

b) Draw the diagram of UMA, NUMA and Multicomputer architecture. (5+5) [CO5]

10.a) With proper numerical examples, explain the concept of Speedup, Algorithmic Scalability and Architectural Scalability.

b) With proper examples, show how Sorting can be done in parallel. (5+5) [CO5]