BE Electronics and Telecommunication Engineering Examination 2023
(2nd Year 1st Semester)
Digital Logic Circuits

Time: 3 Hours **Full Marks: 100**

Answer all the parts of a question in the same place
***Answer question no. 1, any three questions from* Group-A, any four *questions* from Group-B and any two *questions* from Group-C**

1. a) Explain weighted and non-weighted codes with example.
   b) Convert: i) $(34.7)_8$ into Hexadecimal
   ii) $(C6.AE)_{16}$ into Octal
   iii) Gray code (111110011) into binary
   iv) $(9CD.4)_{16}$ into decimal

(4+6)

Group-A

2. a) Design a 4-input OR gate using one 4:1 multiplexer and one 2-input OR gate. Assume constants 0 and 1 are available.
   b) Write the truth table and output expressions of a full subtractor. Implement the full subtractor using minimum number of two input NAND gates.

(3+7)

3. a) What is a counter? What is *MOD* value of a counter?
   b) Design a MOD-3 down synchronous counter using J-K flip-flops and logic gates. Also sketch the corresponding counter circuit.

(2+8)

4. a) Draw the circuit of a master-slave J-K flip-flop using NAND gates only and briefly explain the operation of the circuit.
   b) Derive the characteristic equation of a J-K flip-flop.
   c) What do you mean by universal shift register?

(5+3+2)

5. What do you mean by priority encoder? Write the truth table of an 8 lines-to-3 lines priority encoder and implement corresponding circuit using NOR gates only.

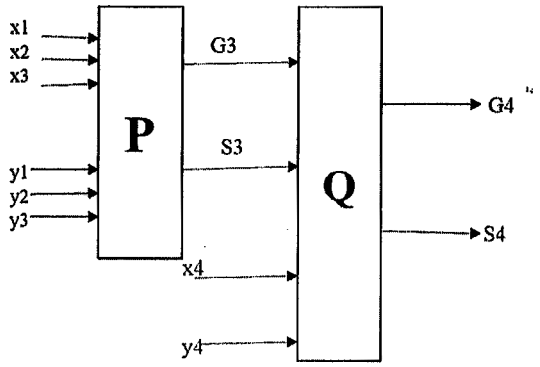
(2+3+5)

Group-B

6. a) Simplify the logic function F (w, x, y, z) = Σ(0, 1, 3, 7, 8, 9, 11, 15) using Quine-McCluskey method.
   b) If AB′+A′B = C then show that AC′+A′C = B

(7+3)

7. a) Implement the Boolean function F(A, B, C) = A′B + BC + AC′ using minimum number of 2:1 multiplexers and one inverter only.
   b) Given logic module P that compares the magnitudes of two 3-bit number X_3 = x1x2x3 and Y_3 = y1y2y3, where x3 and y3 are the least significant bits. Module P has two outputs G3 and S3, such that G3 = 1 if $X_3 > Y_3$; S3 = 1 if $X_3 < Y_3$; and G3 = S3 = 0 if $X_3 = Y_3$. Design the logic unit Q such that together with module P it will serve as a comparator for two 4-bit numbers X_4 = x1x2x3x4 and Y_4 = y1y2y3y4 as shown in the following figure. Find the expressions for G4 and S4 in terms of the inputs to unit Q and show a realization of these expressions using NAND gates only.

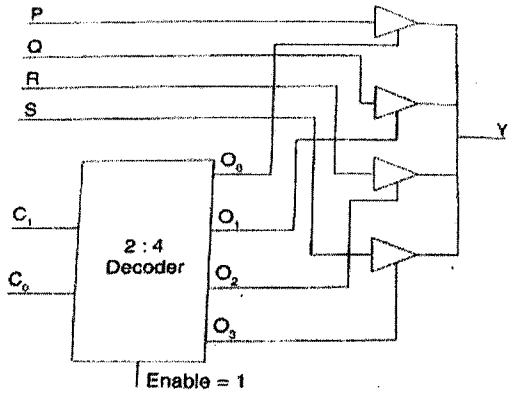


(3+7)

8. a) Four Boolean functions are defined as.
   F_1 (A, B, C) = Σ (0, 1, 3, 5, 6); F_2 (A, B, C) = Σ (4, 6, 7);
   F_3 (A, B, C) = Σ (1, 4, 5, 7); F (A, B, C) = F_1 F_2 + F_3
   Find F (A, B, C) in sum of minterms form.

b) An 8:1 multiplexer has inputs A, B, C connected to the selection inputs S_2, S_1 and S_0 respectively. The data inputs I_0 through I_7 are as: $I_1 = I_2 = I_7 = 0$; $I_3 = I_5 = 1$; $I_0 = I_4 = D$; and $I_6 = D'$. Find the Boolean function that multiplexer implements.

c) Identify the functionality of the following circuit.

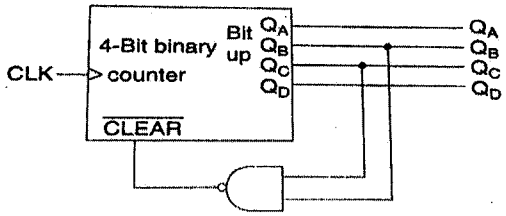


(2+5+3)

9. a) Define propagation delay and noise margin for a logic family. Write the advantages of CMOS logic circuit.
   b) Draw the CMOS circuit of the logic function F (A, B, C) = AB + BC + CA

(6+4)

10. a) Determine the MOD value of the synchronous counter shown in the following figure. Also write corresponding counter states.



b) Design a sequence generator circuit to produce the output sequence 1110100. Also sketch the corresponding circuit.

(3+7)

Group-C

11. a) Explain the operation of a 4-bit R-2R ladder Digital to Analog Converter (DAC) with a neat sketch.
    b) An 8-bit successive approximation ADC is driven by a 2 MHz clock signal. Find the required conversion time.

(8+2)

12. a) Draw a 5-stage ring counter circuit. Write the main disadvantage of the circuit.
    b) The output of a three stage Johnson (switch-tail ring) counter is fed to a DAC. Assume that the counter initially at reset state. Draw the waveform at the DAC output.
    c) A 12-hour digital clock is used to display time in this format 12:00, 12:01...12:59, 1:00, and so on.
        i) How many counters are required to design it efficiently? Write corresponding MOD values.
        ii) Draw a block diagram (connection between counters, seven segment displays, etc.) for the said digital clock.

(3+3+4)

13. a) Draw a 3-bit comparator type ADC circuit to represent output in sign magnitude form and briefly explain the operation of the circuit.
    b) An 8-bit ADC accepts an input voltage of range 0 to 10 volt.
        i) Find the minimum value of the input voltage required to change the LSB?
        ii) What will be the digital output for an input voltage of 4.8 volt.

(3+3+4)