B.E. ELECTRONICS AND TELE-COMMUNICATION ENGINEERING SECOND YEAR SECOND SEMESTER - 2023

DIGITAL CIRCUITS AND SYSTEMS

Time: Three Hours | Full Marks: 100

*Answer **any ten** questions*

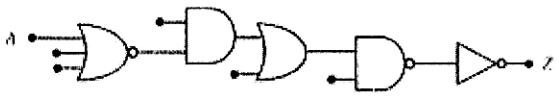
1. Design of SIC Hazard-free circuits for T(x,y,z) = ∑(2,3,5,7). Define S-A-0 and S-A-1 faults. 8+2

2. a) Minimize the following Moore machine using the implication table

PS	NS		Output
	X=0	X=1	Z
A	D	C	0
B	F	H	0
C	E	D	1
D	A	E	0
E	C	A	1
F	F	B	1
G	B	H	0
H	C	G	1

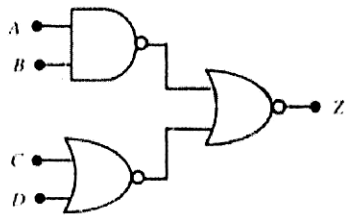
b) Briefly describe Mealy machine with an example. 7+3

3. a) Explain the path-sensitizing method. What are the advantages and disadvantages of the path-sensitizing method? Use the path-sensitizing method for the following circuits:



2+4+4

4. What are the properties of Boolean differences? Obtain the test faults in the following circuit using Boolean difference method: 8+2



5. Multiply the two numbers 23 and -9 by using the Booth's multiplication algorithm. What is Hazards? Briefly describe their types. 6 + 1+3

6. Multiply the two numbers (1 0 1 0) and (0 1 1 0) by using the Partial Sum Approach. What is Implication Table? 7+ 3

7. Explain briefly Booth's algorithm with flowchart. 10

8. What are ROM and RAM? Compare these two memories. Draw the structure of a 4096-bit ROM. 2+2+6

9. Draw the structure of a decimal-to-binary diode-matrix encoder. Draw and briefly explain an SRAM sell using Six-transistor NMOS RAM Cell. 5+5

10. Draw and briefly explain an SRAM sell using CMOS RAM Cell. Briefly describe EPROM with suitable diagram. 6+4

11. What is Verilog Module? Write a Verilog code of an 8-bit adder. What is the difference between wire and reg? What is the difference between $monitor and $display. 2+4+2+2

12. Briefly describe the various steps of modern digital design flow. What is EDA? 8+ 2

13. What is data flow modelling in Verilog? What are the advantages of data flow modeling in Verilog? What does the Verilog code timeframe 1 Ns/ 1 Ps mean? What is the difference between === and ==? 2 + 3 + 3 + 2

14. Show the organization of ROM for storing the following logical equations:
    1. AB'CD' 2. ABCD 3. A'BCD 4. A'BC'D 5. A'B'C'D 6. AB'C'D' 7. ABC'D' 8. ABCD'
    Define the types of parameters used in Verilog with an example. 6+4