Ref. No.: Ex/ET/PC/B/T/215/2023(S)

B.E. Electronics And Tele-Communication Engineering Second Year

First Semester Supple Exam, 2023

ANALOG CIRCUITS- I Time: Three hours Full Marks: 100

(All parts of the same question must be answered together)

Module I [Answer any one (2×10=20)]

1. a) Define PIV of diodes in rectifier circuits. Determine PIV of a diode for center tapped full wave rectifier with and without using capacitor. Input voltage is sinusoidal with 8V peak. Assume diode drop of 0.6 V. [2+4]

   b) Draw the transfer characteristics and output voltage waveform of the clipper circuit shown in Fig.1. V_{B1}=5 V and cut-in voltage of diode =0.6 V. [4]

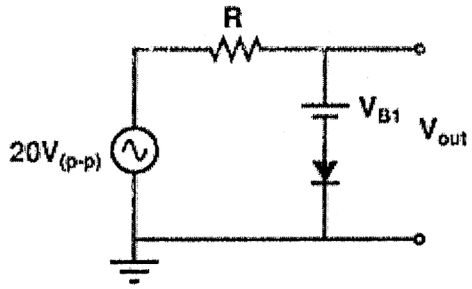

Figure 1

2. a) Find the expression and value for ripple factor of a full wave rectifier. [5]

   b) Draw positive clamper circuit and its output for sine wave input. Explain its operation. [5]

3. a) Draw and explain voltage regulator circuit using Zener Diode. [4]

   b) In a Zener regulator input voltage V_{in}=50V, R_S=2 KΩ and the load having resistance R_L=5KΩ. The output voltage is 30V. Find the current Zener current (I_Z) and load current (I_L). [4]

[Turn over

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Module II [Answer any two (2×15=30)]

4. a) For CE mode amplifier (Fig.2) with emitter feedback the stability factor $S(I_{C0})$ is desired to be 10, determine the value of R_B and R_E. Given that V_{CC}=20V, R_C=3 KΩ, I_C=3mA, β=100, V_{BE}=0.7V and V_{CE}=10V. [5]

b) What do you mean by small signal analysis of an amplifier circuit? For the circuit of part a) find the expression and obtain the value for input and output coupling capacitances to amplify signal of frequency ranging from 1kHz to 20kHz. Given that source resistance is 200Ω and load resistance is 68 kΩ. [2+8]

5. a) With the help load line explain advantage and disadvantage of R_E in Fig. 2. What modification is to be done to overcome the disadvantage? [3+2]

b) With the help of small signal low frequency h-parameter equivalent circuit establish the expression for voltage gain, current gain, input impedance and output impedance for Fig. 2. [10]

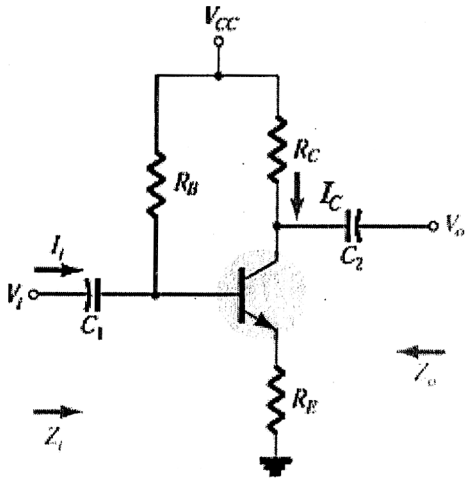

Figure 2

6. a) In a zero bias JFET determine the values of R_D and R_S to achieve maximum output voltage swing. Given that V_{DD}=12 V, I_{DSS}=12mA and V_{GSoff}= -3V. [5]

b) What is Miller effect associated with CS amplifier? Why does source follower circuits are free from Miller effect? With the help of small signal equivalent circuit explain the minimization of Miller effect in Cascode amplifier? [3+1+6]

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Module III [Answer any one (1×10=10)]

7. Draw the basic building block diagram and briefly explain function of each block mentioning appropriate example. Define CMRR of op-amp. Draw the frequency response curve of ideal op-amp. [6+2+2]

8. Write a note on Differential amplifier using npn BJT. [10]

Module IV[Answer any two (2×20=40)]

9. a) Draw an summing amplifier and derive expression for voltage gain. [6]

   b) Draw the output waveform of an integrator using OP-Amp for a square wave input. [4]

   c) Design an analog computer to solve $\frac{d^2y}{dt^2} - 5y = 6$ with y(t=0) = 0. [10]

10. a) Derive the expression for the difference voltage gain of the instrumentation amplifier. [10]

    b) Draw an inverting amplifier using OP-Amp. Determine the expression for voltage gain, input and output resistances considering a practical OP-Amp. [10]

11. a) Draw explain a series voltage regulator circuit. [6]

    b) Using a series voltage regulator design a complete regulated power supply that regulates 220 V, 50Hz input with1% load regulation and 0.1% line regulation. [14]