BE Electronics and Telecommunication Engineering Supplementary Examination 2023
(2nd Year 1st Semester)
Digital Logic Circuits

Time: 3 Hours **Full Marks: 100**

Answer all the parts of a question in the same place
Answer any ten questions

1. a) Using the K-map method, simplify in SOP form the following Boolean function F (W, X, Y, Z) = Σm (0, 2, 3, 6, 7) + Σ d (8, 10, 11, 15). Also implement the simplified expression using minimum number of 2-input NAND gates only.
   b) Express the following function F (x, y, z) = xy + x′z to its canonical POS form.
   (3+4+3)

2. Write the truth table of a 2-bit magnitude comparator circuit, derive output expressions and draw the corresponding gate level circuit.
   (3+3+4)

3. a) Write the truth table of a decimal-to-BCD encoder and derive the output Boolean expressions.
   b) What do you mean by priority encoder? Write the truth table of a four-input priority encoder.
   (6+4)

4. Design a synchronous counter using J-K flip-flops and minimum number of logic gates which has following counting states.
   000→001→011→010→110→100.
   Assume 101 and 111 are don't care states. Also draw corresponding counter circuit.
   (8+2)

5. a) Draw a 4-bit end around carry shift register using J-K flip-flops and logic gates.
   b) What do you mean by sequence generator? Design a sequence generator to produce the output sequence 0010111.
   (3+7)

6. a) Design an 8 bits weighted resistors DAC by cascading two 4-bit weighted resistors DAC and explain its operation.
   b) Draw a functional block diagram for a successive approximation type ADC.

(6+4)

7. a) Write the advantages and disadvantages of TTL logic family.
   b) Why CMOS technology is preferred for designing digital circuits?
   c) Draw a 4-input OR gate using CMOS logic.

(4+2+4)

8. a) Draw a Master-Slave J-K flip-flop with direct set and reset inputs using NAND gates only and explain its operation
   b) With a neat sketch explain set-up time and hold time

(7+3)

9. a) Prove the Boolean expression $(A+B)(A'C'+C)(B'+AC)' = A'B$
   b) Simplify the Boolean function $F(A, B, C, D) = \Pi M(4, 5, 6, 7, 8, 12)$, which has don't care minterms $d(A, B, C, D) = \Sigma m(1, 2, 3, 9, 11, 14)$. Also implement using minimum number of two input NOR gates only.

(3+4+3)

10. a) Implement the Boolean function $F(W, X, Y, Z) = \Sigma m(0, 1, 4, 6, 7, 9, 11, 15)$ using single 4:1 MUX and basic logic gates.
    b) Design a 16:1 MUX using 4:1 MUXs only and briefly explain its operation.

(4+6)

11. a) Draw a 3-bit comparator type ADC circuit to represent output in sign magnitude form. Also explain its operation.
    b) An 8-bit successive approximation ADC is driven by a 2 MHz clock signal. Find the required conversion time.

(8+2)

12. a) Draw a D-type flip-flop circuit and write corresponding truth table as well as characteristic equation.
    b) Draw and briefly explain the operation of a S-R flip-flop where direct set and reset inputs can override the clock.

(5+5)