Ref. No.: Ex/ET/T/215/2023

B.E. Electronics And Tele-Communication Engineering Second Year

First Semester Exam, 2023

ANALOG CIRCUITS- I **Time: Three hours** **Full Marks: 100**

(All parts of the same question must be answered together)

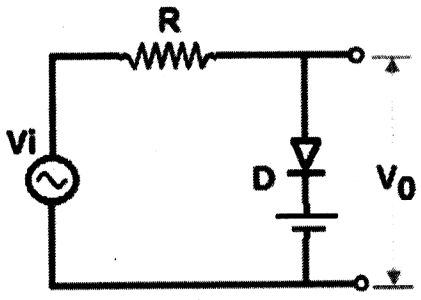
Module I [Answer any one (1×20=20)]

1. a) Write names and briefly explain the operations of the circuits (i, ii, iii, and iv) . [10+10]

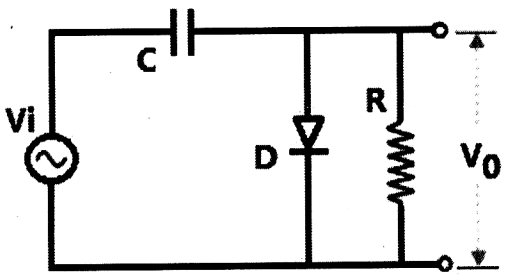
b) Sketch the output waveforms of the following circuits for

i. Sinusoidal input (consider diode drop)
ii. Square input (consider diode drop)
iii. Sinusoidal input (ideal diode)
iv. Amplitude modulated input (ideal diode)

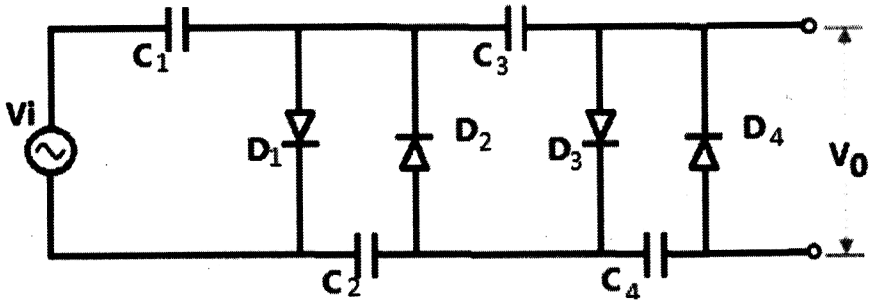
i)



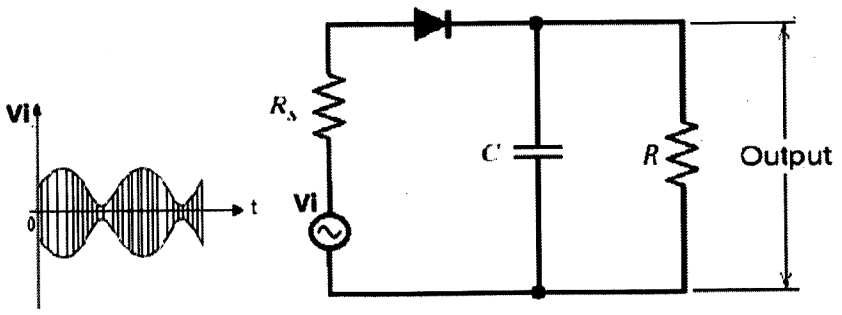
ii)



iii)



iv)



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Ref. No.: Ex/ET/T/215/2023

B.E. ELECTRONICS AND TELE-COMMUNICATION ENGINEERING SECOND YEAR

FIRST SEMESTER EXAM, 2023

ANALOG CIRCUITS- I **Time: Three hours** **Full Marks: 100**

2. a) A Zener voltage regulator has input voltage V_{in}=20V and R_S= 500Ω. The Zener voltage at breakdown voltage is 6V. The Zener current at breakdown (I_{Zk}) is 0.1mA and maximum Zener current (I_{zm}) is 0.1 A. The dynamic resistance is 20Ω. Find the range of load resistance can be used. [10]

b) Explain the output of a RC high pass filter for a pulse input. A pulse of amplitude 10 V and width t_p =10 μs is applied to a high-pass *RC* circuit. Sketch the output waveforms indicating the voltage levels for (i) $RC = t_p$, (ii) $RC = 0.5t_p$ and (iii) $RC = 2t_p$. [10]

Module II [Answer any two (2×15=30)]

3. a) Draw a capacitive coupled CE mode npn BJT amplifier with an un-bypassed emitter resistance. With the help of small signal equivalent circuit (any one) find the expression for the voltage gain, input resistance and output resistance. [12]

b) Explain the effect of coupling capacitances on voltage gain. [3]

4. a) Draw a collector to base feedback biasing of npn CE mode BJT to obtain $S(I_{C0})$=10 and collector current of 1mA. Assume Supply voltage as 10 V. Set operating point at the mid of the load line. [10]

b) Draw and explain the Darlington pair circuit using npn BJT. [5]

5. a) In a zero bias JFET determine the values of R_D and R_S to achieve maximum output voltage swing. Given that V_{DD}=10 V, I_{DSS}=12mA and V_{GSoff}= -6V. [5]

b) Explain Miller effect associated with CS mode FET amplifier with the help of small signal model. Why are source follower circuits free from Miller effect? [7+3]

Module III [Answer any one (1×10=10)]

6. Define Op-amp. Write down six characteristics of an ideal OP-Amp. Explain origins of input offset voltage, input bias current and slew rate of a practical op-amp. [2+3+5]

7. Draw basic differential amplifier using npn BJT. Find out the common mode and difference mode voltage gain for double input balanced mode configuration. [2+8]

Ref. No.: Ex/ET/T/215/2023

B.E. Electronics And Tele-Communication Engineering Second Year
First Semester Exam, 2023

ANALOG CIRCUITS- I **Time: Three hours** **Full Marks: 100**

Module IV[Answer any two (2×20=40)]

8. a) Define line and load regulation of a voltage regulator. Explain the short circuit protection circuit in a series voltage regulator. [4+6]

b) Design a 10 V regulated power supply with a series voltage regulator. (Properly choose the values of resistances, input voltage range and Zener voltage). Assume Zener resistance is as 0Ω and Zener current range is 0.1 mA to 100 mA. [10]

9. a) Draw an inverting amplifier using OP-Amp. Determine the expression for voltage gain, input and output resistances considering a practical OP-Amp. [10]

b) With the help of proper circuit diagram, input and output waveforms explain the operation of an integrator circuit using OP-Amp. [10]

10 a) Explain the super diode using OP-Amp. Draw a negative clipper circuit using OP-Amp and sketch the output for a rectangular input of 5V peak. [10]

b) Draw an op-amp circuit to solve $\mathbf{y = 5xy + 10x^2}$ [10]