Ref. No.: Ex/EE/PC/B/T/225/2023

B. E. ELECTRICAL ENGINEERING 2ND YEAR 2ND SEMESTER EXAMINATION, 2023

Subject: SEQUENTIAL SYSTEMS & MICROPROCESSOR Time: 3 Hours Full Marks: 100

Use a separate Answer-script for each Part

Part I (50 marks)

Question No.		Marks
	Question 1 is compulsory Answer ***Any Two*** questions from the rest (2×20)	
Q1	Answer ***any Two*** of the following:	
	(a) Discuss the differences between Combinational and Sequential logic circuits?	5
	(b) Toggle flip-flop, known as T flip-flop has following input-output relation. When input $T = 0$, the output Q does not change its state. For $T = 1$, the output Q toggles its value. Derive T flip-flop from JK flip-flop.	5
	(c) Starting from the excitation table develop the State Diagram for S-R flip-flop.	5
	(d) A JK master-slave flip-flop has its J and K inputs tied to $+V_{CC}$ and a series of pulses are applied to its clock input. Describe the waveform at its output Q.	5
Q2	(a) Analyze the circuit shown in Figure Q2(a) and draw the timing diagram for the circuit shown in figure for 6 clock pulses.	8

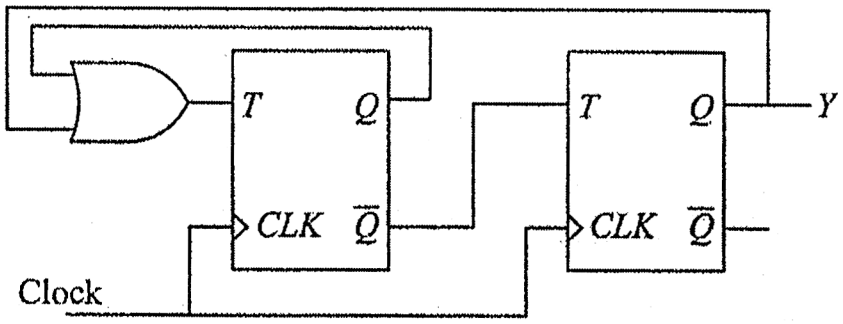


Figure Q2(a)

	(b) What is State Synthesis Table for a Flip-flop? With the help of State Synthesis Table show how SR-flip-flop can be converted to JK-flip-flop.	2+6
	(c) Enumerate, with the help of schematic diagrams, different types of Shift Register configurations that are commercially available.	4
Q3	(a) What are Synchronous and Asynchronous Counters? What are the basic differences between them ?	4

Q3 (b) Show that the circuit shown in Figure Q3(b) combines both Synchronous and Asynchronous counter. With the help of proper characteristic table explain the operation of the circuit. 2+8

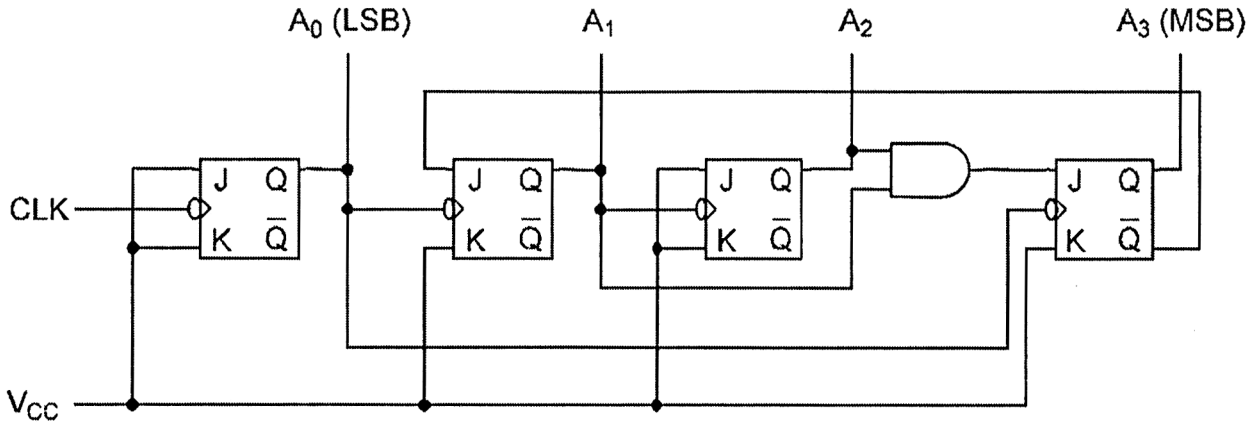


Figure Q3(b)

(c) With the help of a schematic diagram explain the functioning of a 4-bit parallel-in–serial-out shift right register realized using D flip-flops. 6

Q4 (a) Consider the counter specified in Table Q4(a). The count has a repeated sequence of six states, with flip-flops B and C repeating the binary count 00, 01, 10, and flip-flop A alternating between 0 and 1 every three counts. With the help of State Synthesis Table realize the counter using JK flip-flops. 12

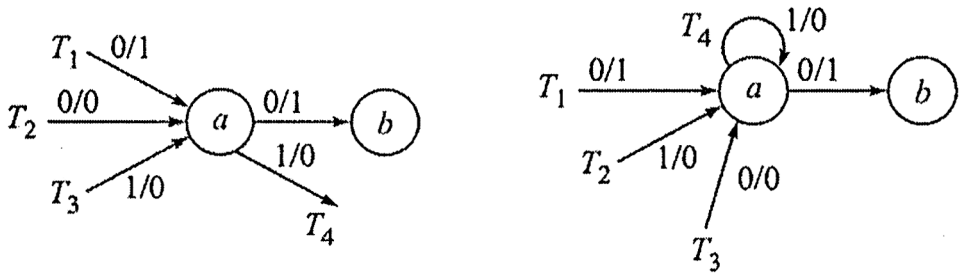
Present State				Next State		
A	**B**	**C**		**A**	**B**	**C**
0	0	0		0	0	1
0	0	1		0	1	0
0	1	0		1	0	0
1	0	0		1	0	1
1	0	1		1	1	0
1	1	0		0	0	0

Table Q4(a)

(b) What is a State Transition diagram?

How does the State Transition Diagram for a Moore Machine differ from that for a Mealy Machine? 2+2

Q4 (c) Show how the State Transition Diagram for a Mealy Model as shown in Figures Q4(c) (i) and (ii) can be converted to their equivalent Moore Model diagrams. 2+2



(i) (ii)

Figure Q4(c)

Q5 (a) Consider the following Vending Machine Design Problem:

The task is to design a synchronous logic control unit of a vending machine. The machine can take only two types of coins of denomination 1 and 2 in any order. It delivers only one product that is priced ₹3. On receiving ₹3 the product is delivered by asserting an output D = 1 which otherwise remains 0.

If it gets ₹4 then product is delivered by asserting X and also a coin return mechanism is activated by output Y = 1 to return a ₹1 coin.

There are two sensors to sense the denomination of the coins that give binary output as shown in the following table. The clock speed is much higher than human response time, i.e. no two coins can be deposited in same clock cycle. 6+6

I	*J*	**Coin**
0	X	No coin is inserted
1	0	One rupee Coin
1	1	Two rupees Coin

Draw the ASM chart for a Mealy Model of the problem and derive the corresponding State Transition Diagram.

(b) Design a synchronous sequential circuit having a State Transition Diagram as shown in Figure Q5(b) with the help of D flip-flops.

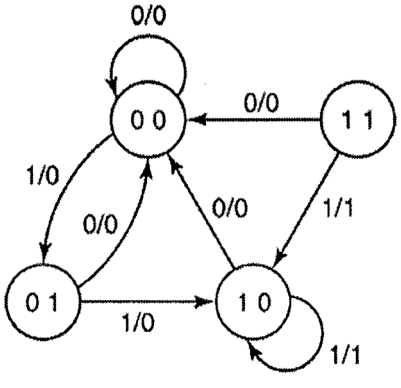


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Figure Q5(b)

Ex/EE/PC/B/T/225/2023

B.E. ELECTRICAL ENGINEERING SECOND YEAR SECOND SEMESTER - 2023

SEQUENTIAL SYSTEMS AND MICROPROCESSORS

Time: Three hours (50 marks for each Part) Full Marks: 100

Use a separate Answer-Script for each Part

PART- II

Answer ***any five*** questions.

1. Answer any **five** of the following: (5 x 2)
   - i. State the relation between the number of address pins and physical memory space.
   - ii. State the difference between ALU and CPU.
   - iii. What is meant by Bus idle machine cycle?
   - iv. State the relation between wait state and READY signal.
   - v. In which T-state does the CPU send the ALE signal for demultiplexing?
   - vi. How are the interrupts affected by system reset?

2.a) Draw the internal block diagram of an 8085 microprocessor. (7)

b) Explain the importance of program counter in 8085 microprocessor. (3)

3.a) If a 4MHz crystal frequency is connected with 8085 microprocessor, what is the value of system clock frequency? Compute the execution time of instruction STA 8050H for the same microprocessor. (3)

b) Draw and discuss the timing diagram of IN 05H the corresponding hex code being DBH. (7)

4. Interface 2kb RAM and 256 x 8 ROM with 8085 processor to satisfy the total memory of 8kb RAM and 1kb ROM with suitable interfacing diagram and explanation. If required address lines are connected to address decoder for interfacing, then what will happen? (8+2)

5. Write an assembly language program for Intel 8085 to (4+6)
   - i. perform the same task as XTHL
   - ii. convert Hexadecimal to Binary

   or, find the nth Fibonacci number, the value of n being 4.

6.a) Explain the functions of the following set of instructions and also specify the content of registers A, D, HL after execution of the program. (7)

```
        LXI H, 8000H
        SUB B
        MVI D, 0FH
Loop:   MOV M,A
        INX H
        DCR D
        JNZ  Loop
        HLT
```

b) Explain the function of Intel 8085 instruction 'DAA'. (3)

7.a) Explain how RIM instruction is used to sense the pending interrupts with the help of word format and programming. (7)

b) What is masking and why is it required in 8085 interrupts? (3)

8. Explain how SIM is used to mask vector interrupts with proper example. (10)