Ex/CSE/PC/B/T/215/2023(S)

B.E. Computer Science and Engineering 2nd Year 1st Semester

Supplementary Examination 2023

Subject: Computer Organisation

Time: 3hrs **Full Marks:** 100

Answers of all sub-parts of a question must be in *adjacent* locations

1 a. Draw the Von-Neumann architecture and give a brief description about all components. 8

OR

Discuss the IAS instruction set.

b. Explain the **any two** addressing modes. 4

c. Develop the instruction sets to execute the expression C=(A+A) + (A+A) + (A+A) by using a 1-address **OR** 2-address machine. 3

2 a. Design the Adder and Subtractor circuit. 4

b. Give an example of restoring **OR** non-restoring type division of 2's complement numbers with mentioning all the steps clearly. Give the flowchart of the algorithm you used. 6+5

3 a. With a suitable example illustrate the implementation issues of Direct **OR** Set-associative mapping scheme used in cache memory. 10

b. With an appropriate example show LRU **OR** LFU page replacement algorithm. 5

c. With a suitable example show how Hamming Code is used for error detection/correction. 10

d. With a pictorial diagram briefly describe the SSD architecture. 10

OR

Discuss the data recoverability issues in different RAID levels.

4 a. With a description of working principle, diagrammatically show the Wilke's design for implementing micro-programmed control unit. 12

OR

Formulate the space reduction procedure in the nano-programmed control unit.

b. What are the advantages and limitations of the control unit design you have answered above? 3

[Turn over

5 a. Discuss the features of **any three** categories of device identification techniques used in any I/O system. 6

b. With a short description show the flowchart for the programmed-driven **OR** interrupt-driven I/O technique. 4

c. Mention some problems and corresponding solutions related to Data Hazard **OR** Control Hazard. 10