B.E. Computer Science and Engineering 2nd Year 1st Semester Examination 2023

Subject: Computer Organisation

Time: 3hrs   Full Marks: 100

Answer **all**

Answers of all sub-parts of a question must be in *adjacent* locations

1   a. Describe key roles of operating system.   2

    b. Sketch the Von-Neumann architecture and give a very brief description about each   6
        component.

        OR

        Discuss the IAS instruction set.

    c. Explain the **any two** addressing modes – direct, indirect, immediate, and indexed.   2

    d. Develop the instruction sets to execute the expression C=(A*A) + (B*B) by using a   3
        1-address **OR** 0-address machine.

    e. In a complete execution cycle, mention the scenarios/locations, where there may be   2
        a possibility of occurring an interrupt.

2   a. Design the Carry Look-ahead adder (show circuit diagram also).   8

    b. Give an example of Restoring **OR** Non-restoring type division of 2's complement   7
        numbers with mentioning all the steps clearly.

3   a. Illustrate the implementation issues of Direct **OR** Associative-mapping scheme used   7
        in cache memory. Give a suitable example.

    b. With an appropriate example show the LRU **OR** FIFO page replacement algorithm.   3

    c. Give a block diagram for Pentium 4 cache memory.   4

    d. "Hamming code is used to detect/correct soft errors" – is it a correct statement? With   8
        a suitable example show how it is used for error detection/correction.

    e. Write some characteristics of typical SDRAM **OR** DDR-SDRAM.   2

    f. Give the details of the Winchester Disk format.   5

    g. With a pictorial diagram briefly describe the SSD architecture.   6

        OR

        Discuss the data recoverability issues in RAID levels 2, 4 and 6.

[Turn over

4   a. Discuss the usage and design issues of stack.   5

     b. With a brief description of working principle, pictorially show the Wilke's design 8
for implementing micro-programmed control unit.

       OR

       Formulate the space reduction procedure in the nano-programmed control unit.

     c. What are the limitations of the control unit design you have answered above?   2

5   a. Give a block diagram for an external device **OR** an I/O module.   2

     b. Discuss the features of **any two** categories of device identification techniques used 4
in any I/O system.

     c. With a short description show the flowchart for the programmed-driven **OR** 4
interrupt-driven I/O technique.

     d. What are the two main pre-requisites for designing a pipeline architecture?   2

     e. Mention some problems and corresponding solutions related to Data Hazard **OR** 8
Instruction Hazard.