Development of Improved MLI Topology with Low Switching Loss and Low Output Voltage Harmonics Suitable For PV-Grid Integration

A thesis submitted for fulfilment of the requirement for the degree of Doctor of Philosophy (Engineering) in the Faculty of Engineering &Technology, Jadavpur University

By

Rupali Mohanty

Department of Electrical Engineering
Faculty Council of Engineering & Technology
Jadavpur University
Kolkata, India

2023

FACULTY OF ENGINEERING & TECHNOLOGY
JADAVPUR UNIVERSITY
KOLKATA-700032, INDIA

INDEX NO: 234/20/E

1.	**Title of the Thesis:**	**Development of Improved MLI Topology with Low Switching Loss and Low Output Voltage Harmonics Suitable for PV-Grid Integration**
2.	**Name, Designation & Institution of the Supervisor/s:**	**Name: Dr. Debashis Chatterjee** Designation: Professor, Department: Electrical Engineering, Institution: Jadavpur University, Kolkata 700032; West Bengal, India

1. List of Publications:

I. JOURNAL PUBLICATIONS

[1] R. Mohanty, D Chatterjee, S. Suman and M. Anand, "A Reduced Switch Count Multilevel Inverter for PV Standalone System using Modified JAYA Algorithm," **International Journal of Electronics, Taylor and Francis**, 2022, DOI: 10.1080/00207217.2022.2164073.

[2] R. Mohanty, D Chatterjee, S. Suman, "Honey Badger Optimization based grid interactive asymmetrical cascaded MLI with minimum voltage distortion," **Evolving Systems, Springer**, 2023, DOI:10.1007/s12530-023-09493-1.

[3] R. Mohanty, D Chatterjee, Satyajit Mohanty, Dhanamjayulu C, Baseem Khan, "THD Reduction of Improved Single Source MLI using Upgraded Black Widow Optimization Algorithm ," **International Transaction on Electrical Energy System**, 2023, DOI:10.1155/2023/6724716.

[4] R. Mohanty, D. Chatterjee, S. Suman, "Red Deer Optimization based Asymmetrical Reduced Switch MLI with Low Switching Loss and Minimum Voltage Harmonics," **International Journal of Power Electronics, Inderscience**, 2023, DOI: 10. 1504/IJPELEC.2024.10056817.

[5] R. Mohanty et.al, "Lower Output Voltage Harmonics with Optimum Switching Angles of Single PV-Source Based Reduced Switch Isolated Multilevel Inverter using BWO Algorithm," **IEEE Access (Under Review)**.

II. BOOK CHAPTER PUBLICATION

[1] R. Mohanty, S. Suman, D. Chatterjee, "Comparison Analysis of THD Optimization Using PSO and Jaya Algorithm in Reduced H-bridge Multilevel Inverter," In: Mahanta P., Kalita P., Paul A., Banerjee A. (eds) **Advances in Thermofluids and Renewable Energy. Lecture Notes in Mechanical Engineering. Springer**, 2022, Singapore. DOI:10.1007/978-981-16-3497-0_55.

III. CONFERENCE PUBLICATION

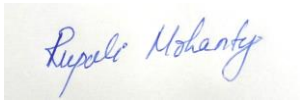
[1] R. Mohanty, D. Chatterjee, S. Suman and G. Sengupta, "PSO Based Improved Topology for MLI Considering Low THD and Low Switching Loss," 10th **International Conference on Computing, Communication and Networking Technologies** (ICCCNT), 2019, pp. 1-5. DOI: 10.1109/ICCCNT45670.2019.8944546.

Statement of Originality

I Rupali Mohanty registered on 13. 02. 2020 do hereby declare that this thesis entitled "Development of Improved MLI Topology with Low Switching Loss and Low Output Voltage Harmonics Suitable for PV-Grid Integration" contains literature survey and original research work done by the undersigned candidate as a part of Doctoral studies.

All information in this thesis have been obtained and presented in accordance with existing academic rules and ethical conduct. I declare that, as required by these rules and conduct, I have fully cited and referred all materials and results that are not original to this work.

I also declare that I have checked this thesis as per the "Policy on Anti Plagiarism, Jadavpur University, 2019", and the level of similarity as checked by iThenticate software is **5%**.



Signature of Candidate

08/06/2023

Date

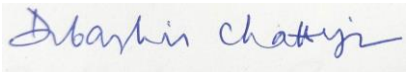
Certified by the Supervisor

08/06/2023

Date

Certificate from the Supervisor

This is to certify that the thesis entitled "Development of Improved MLI Topology with Low Switching Loss and Low Output Voltage Harmonics Suitable for PV-Grid Integration ", submitted by Rupali Mohanty, who got her name registered on 13th February 2020, for the award of Ph. D. (Engg.) degree of Jadavpur University, is absolutely based upon her own work under the supervision of Prof. (Dr.) Debashis Chatterjee and that neither her thesis nor any part of the thesis has been submitted for any degree/diploma or any other academic award anywhere before.



Signature of the Supervisor

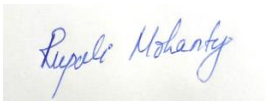
ACKNOWLEDGEMENT

To my advisor, Professor (Dr.) Debashis Chatterjee of the Electrical Engineering Department at Jadavpur University, I am eternally grateful. Without his tremendous help and direction, it would not have been possible to finish the job. His inspiration, insight, and faith guided me towards investigation and originality.

I would like to thank the department chair of Electrical Engineering at Jadavpur University for providing the environment and opportunity for research. I am grateful to the members of the research committee for their insightful criticism and helpful recommendations.

I would like to express my appreciation to my co-authors, Ms. Swati Suman and Mr. Mukul Anand for their contribution. I acknowledge the inspiration of my senior colleagues, Dr. Anagha Bhattacharya and Dr. Subhendu Bikash Santra. Author would like to thanks her lab mates Mr. Boni Sai Satya Varun and Mr. Snehesh Sharma for their support and help to get the results of research work.

Last but not the least, I would like to show appreciation and acknowledgement to my parents and family for the never-ending support, comprehension, and blessings they have bestowed upon me. If it were not for them, I never would have been able to finish this research and this thesis.



Department of Electrical Engineering

Jadavpur University

Rupali Mohanty

Dedicated to

Lord Krishna

And

My Grand Father late Sri Basanta Kumar Behera

Contents

SWITCHED MULTILEVEL INVERTER for PV STANDALONE SYSTEM

List of Symbols and Abbreviations

Symbols

V_l	Output Voltage level
N	Number of DC voltage source
N_{sw}	Number of power switches
V_{max}	Maximum value of output voltage
V_D	Voltage at each step
$\alpha_1, \alpha_2 \ldots\ldots\ldots \alpha_{ai}$	Switching angles
n	Number of odd harmonics
S1,S2,…SN	Power switches in the circuit
V_1	Fundamental output voltage
F	Fitness function
V_n	Odd harmonic voltages
V_{c1}	Input Voltage to flyback converter
P_L	Power loss of the device
P_s	Switching loss of the device
$P_{conduction}$	Conduction loss of the device
V_T	Transistor on state voltage drop
V_d	Diode reverse voltage drop
$r_{T,} r_D$	Resistance of transistor and diode
P_{LT}, P_{LD}	Conduction loss of transistor and reverse diode
β	Gain constant
E_{on}	On state energy loss
E_{off}	Off state energy loss
N_{on}	Number of times the switch is getting on
N_{off}	Number of times the switch is getting off
V_{sd}	Voltage across a switch before switching on or after

	switching off
I_s	Current across switch after switching on or before switching off
V_o	Boost output voltage
V_i	PV output voltage
D	Duty ratio of the device
V_{out}	Output of flyback converter
K1	Transformation ratio
k1,k2….ki	Input voltage ratios
V_g^*	Reference grid voltage
itr_m	Maximum iteration
θ	Voltage angle
ω	Angular frequency of grid voltage
ai	Maximum number of switching angles
V_{lmax}	Maximum level of voltage
p	Probability value
s_α	Level of significance
TSV_{MLI}	Total standing voltage of MLI

Abbreviations

MLI	Multilevel Inverter
THD	Total Harmonic Distortion
CHBMLI	Cascade H-bridge MLI
ACHBMLI	Asymmetrical Cascade H-bridge MLI
TSV	Total Standing Voltage
MI	Modulation Index
PWM	Pulse width modulation
SPWM	Sinusoidal Pulse width modulation
PSO	Particle Swarm Optimization

GWO	Grey Wolf Optimization
MGWO	Modified Grey Wolf Optimization
CSMLI	Cross switched MLI
BWO	Black Widow Optimization
NLC	Nearest level control
PUC	Packed U-cells Converter
HybMLI	Hybrid Multilevel Inverter
MJAYA	Modified JAYA algorithm
MPSO	Modified PSO algorithm
RDO	Red Deer Optimization
HBA	Honey Badger optimization Algorithm
GA	Genetic Algorithm
PV Panel	Photo Voltaic Panel
SHE	Selective Harmonic Elimination
RT	Real Time

List of Figures

List of Tables

Chapter-1

INTRODUCTION

Importance of multilevel inverter, its advantages and requirement of reduced switch Multilevel Inverter has been discussed in this chapter. Use of Optimization algorithm to solve the harmonic minimization problem has been discussed. Motivation and Objective of the research work has also been pointed. At the end orientation of the thesis has been mentioned.

INTRODUCTION

1.1 INTRODUCTION

In the current era demand of electricity has reached to its pick. Generation of electricity in the past century mostly depends on fossil fuel, hydro power, and nuclear power. In order to fulfil the huge demand of electric energy, researchers are focusing on to fulfil this demand from renewable energy sources. Solar energy is the most convenient and clean form of energy that has been used as an alternative energy source without affecting the environment.

Storage of solar radiant and energy conversion are the vital issues [1.1] that has been focused to provide the continuous power supply from this inexhaustible source of energy. In addition to this for proper utilization of solar energy and to fulfil the energy demand during its peak, researchers have developed the suitable storage device and also heat transfer techniques are implemented for solar based thermal power plant. Choosing the suitable material for storage device makes the solar energy dispatchable for commercial purpose [1.2]. Generation of electricity from thermal energy of sunlight has been carried out through concentrating solar power and thermal energy storage has improved the efficiency of the solar power plant and made profitable [1.3], [1.4]. Apart from that, utilization of solar energy for commercial purpose or domestic purpose are done through photovoltaic (PV) cell. PV cells are assembled to form PV panels, which are mounted in a larger area or smaller area according to the energy demand. PV energy is integrated to grid with proper control arrangement and the PV panels are also installed for off-grid system to supply the energy independently. The main advantage of PV panel is, it can use for small scale power generation or can use as an independent energy source for different loads in remote area. In order to generate the constant solar energy from the PV power plant and to make an active participant in electricity market, optimization of energy management and estimation of daily solar energy for PV power plant has been developed [1.5], to improve the performance of the power plant and to make it more reliable, controller for solar energy is also proposed [1.6].

The measure drawback of PV energy is nonuniform power supply due to the weather condition, varying irradiation of solar energy and ambient temperature. This leads to lower efficiency of power conversion. To harness maximum solar energy and to operate the load under maximum power condition, maximum power point tracking (MPPT) mechanism has

been developed. Some efficient methods are introduced to track the maximum power and minimize the power loss with enhance power quality [1.7] - [1.10]. In addition to this to improve the MPPT techniques in different varying condition and to converge the maximum power among multiple peaks occurred due to varying irradiation, different optimization methods are adapted [1.11] - [1.14].

Apart from this, power conversion of solar energy is highly needed for different AC loads, industry application and integrating this energy with medium/high power grid or islanded grid. The efficiency of solar power has been improved in two stage power conversion. Initially the DC-DC boost converter is employed to step up the PV output voltage and maintains consistency voltage during dynamic behaviour of PV input. In second step inverter circuit is used to convert the DC voltage or power to AC power [1.15]. In order to provide reliable, stable and ripple free AC voltage to the grid or micro grid different inverter topologies with control techniques have been proposed [1.16] - [1.19]. In these schemes additional filter circuits and higher rated transformers are implemented for improved power quality or distortion free voltage and current at the grid side but use of filter circuits or transformer makes the system heavier and overpriced.

In order to overcome the above challenges researchers are aiming on developing different topologies of Multilevel Inverters (MLI) for efficient power conversion. MLIs are providing staircase voltage waveforms across output with less distortion. The Total harmonic Distortion (THD) and switching frequency of the MLI is lower than the three level conventional inverter. But the limitations that observed in MLIs are, to increase the output voltage level, clamping devices are required that increases the size of MLI and the design becomes more complex [1.20]. Cascaded H-bridge MLI (CHBMLI) has been widely used for PV-grid interconnection due to its transposable and compact size, symmetry behaviour across output which avoids higher magnetic interference [1.21] - [1.24]. In addition to this, researchers have developed different advanced MLI topologies for power conversion with reduced number of power switches that reduces the switching loss and makes the system efficient and cost effective [1.25] - [1.29]. With the proposed topologies, different switching schemes for MLIs have also been proposed to obtain lower THD, lower dv/dt stress and lower switching stress. These techniques provide smooth operation of MLIs for different applications [1.30] - [1.33].

1.2 MULTILEVEL INVERTER and ITS VARIOUS TOPOLOGIES

Power converters for high voltage and high power application is enlightened by multilevel converters. Multilevel Inverters provide higher quality output voltage from various DC input voltages with different modular structure. In present decades Multilevel Inverters (MLIs) have been used widely for medium to high power application. MLI uses lower rating devices with number DC voltage sources for high power application in industry and PV-Grid integration with lesser distortion of output voltage. The conventional three level inverter provides square wave voltage and current during the power conversion, which leads to higher Total Harmonic Distortion (THD) of output voltage nearly 40%. MLI provides smoother voltage waveform by combining the input voltage sources with suitable switching combination.

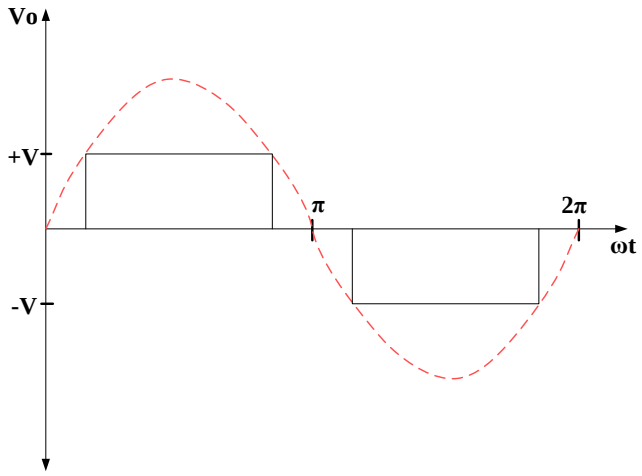


Figure 1.1. Voltage waveform of 3 level inverter

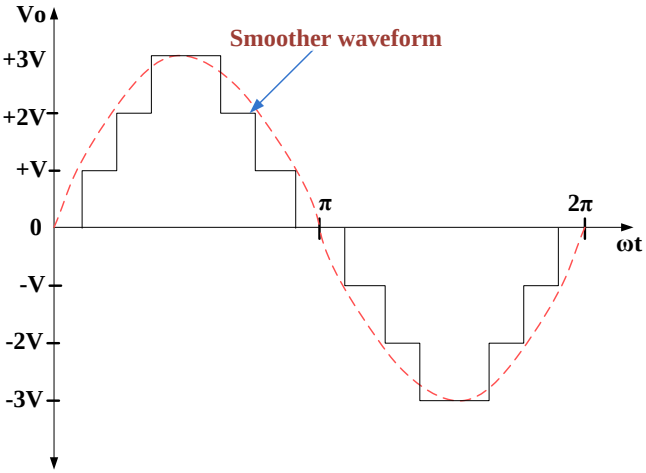


Figure 1.2. Voltage waveform of Multilevel Inverter

In the early stage of multilevel inverter three developed topologies are shown in figure 3. Their working principle, merits and demerits are discussed in [1.20].

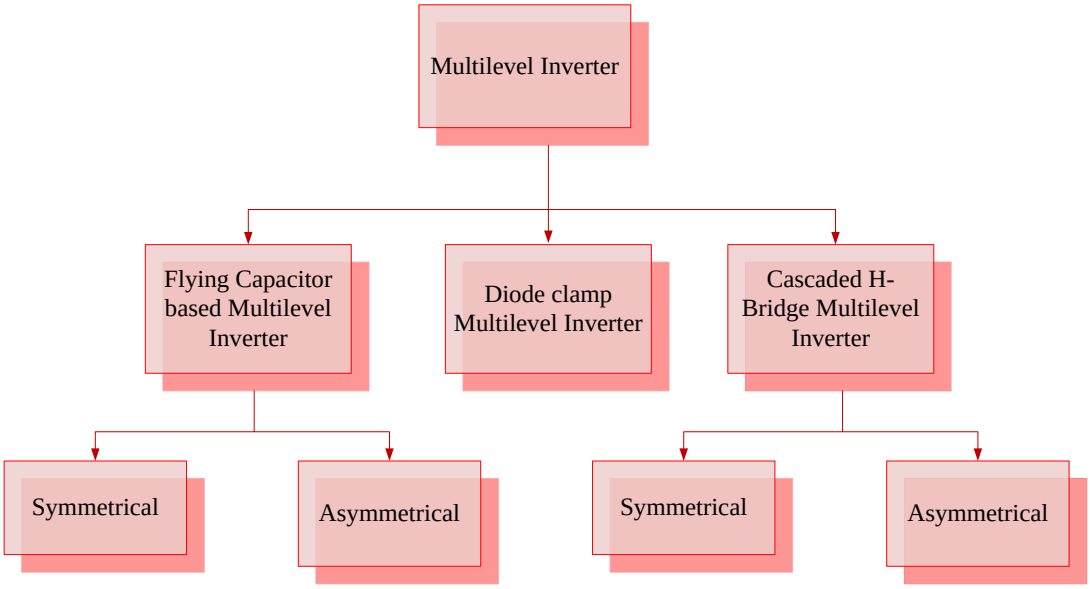


Figure 1.3. Different topology of Multilevel Inverter

Flying capacitor based MLI and Cascaded H-bridge MLI are categorised in to symmetrical and asymmetrical source based MLI. The MLIs with equal magnitude of DC input voltages are known as symmetrical source based MLI where the output voltage level (V_l) can be expressed by,

$$V_l = 2N + 1 \tag{1.1}$$

Here N is the number of input DC sources of the MLI.

The MLIs with unequal magnitude of DC input voltages are called asymmetrical source based MLI and the output voltage level depends on the topology of that respective MLI.

Among the three basic topologies of MLI shown in figure 3, the switching control of diode clamped MLI is simpler due to its horizontal roofing structure. But, to generate higher voltage level across output it requires higher number of clamping diodes. Another measure demerit is to control real power flow for each converter. In case of flying capacitor based MLI both reactive and real power can be controlled and it can be used for high voltage DC transmission. This MLI needs larger number of capacitor bank for developing higher output voltage level which makes the system heavy and overpriced. Switching frequency of flying

capacitor MLI is higher which leads to higher switching loss. The above failings of diode clamped MLI and flying capacitor MLI are overcome by cascade H-bridge MLI (CHBMLI). In CHBMLI separate DC sources are used for generating each voltage level and the maximum voltage level is the summation of all input voltage sources used in the MLI. It does not require extra capacitors and clamping diodes for obtaining staircase output voltage which makes this MLI compact in structure and cost effective than the above two MLIs. The modular structure of CHBMLI is shown in figure 4.

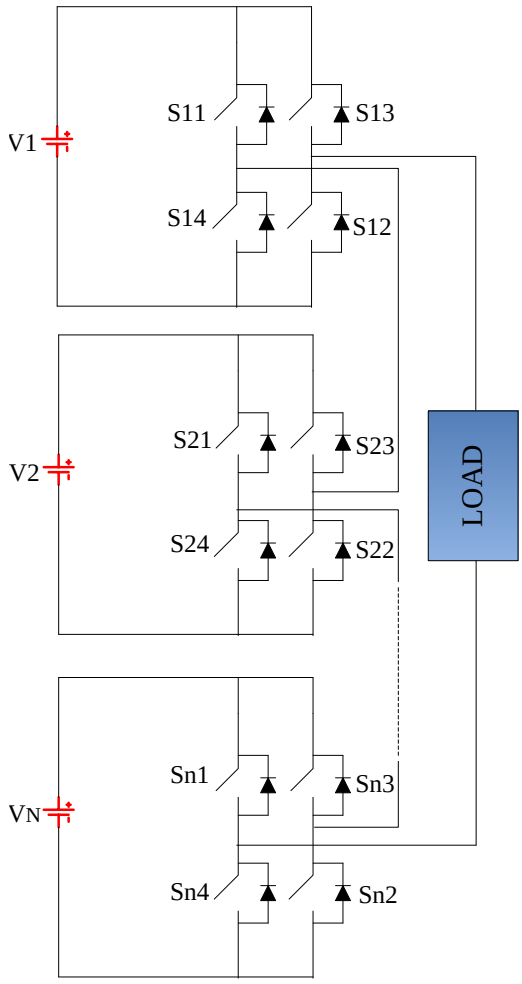


Figure 1.4. Cascaded H-bridge MLI with 'n' number of DC voltage sources

In the above figure 'N' number of H-bridge are connected in the cascaded manner and each H-bridge requires separate DC source. The switching devices required for generating 'V_l' level output voltage is,

$$N_{sw} = 4N \tag{1.2}$$

In case of symmetrical CHBMLI, V1=V2=V3=……=V_N and the maximum output voltage can be expressed as:

$$V_{max} = V1 + V2 + \cdots + V_N \tag{1.3}$$

If each DC source voltage value is V_s, then the maximum output voltage can be,

$$V_{max} = NV_s \tag{1.4}$$

The stepped output AC voltage waveform obtained from CHBMLI is shown in figure 5.

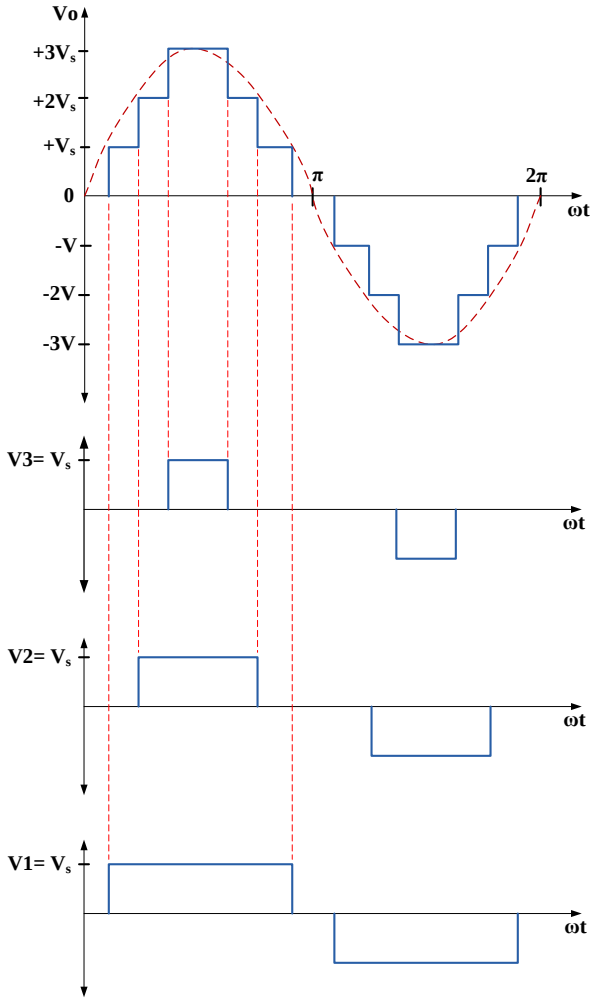


Figure 1.5. Output voltage waveform of a 7-level CHBMLI

A 7-level voltage waveform has been shown in figure 1.5 to explain the cascading of input voltages across load. The stepped voltage waveform has been attained by suitable switching combination of the MLI. The major points that to be considered, for developing a higher voltage level CHBMLI to reduce the output voltage and current distortion are:

a- Higher number of separate DC sources are required.

b- Higher number of switching devices are needed, which increases the inverter loss.

c- Increase of Total Standing Voltage (TSV).

As discussed in the introduction section, for PV-grid integration or high voltage application, efficient power conversion through MLI can be carried out with higher voltage level. Considering the above points of CHBMLI, the research has been diverged towards inventing the MLI topologies with reduced number of switching devices and input voltage sources.

1.3 REDUCED SWITCH MULTILEVEL INVERTER

Reduced switch MLIs are invented to develop the higher-level output voltage with the help of smaller number of semiconductor switches and avoids the use of higher number of driver circuits. Reduced Multilevel inverters are cost effective, smaller in size and bear lower switching loss. Some of the developed reduced switch MLIs with their circuit design are discussed in this section.

a- A cascaded half bridge based MLI with H-bridge has been proposed by E. Babaei in the year 2009. The circuit diagram of the proposed topology has been shown below.

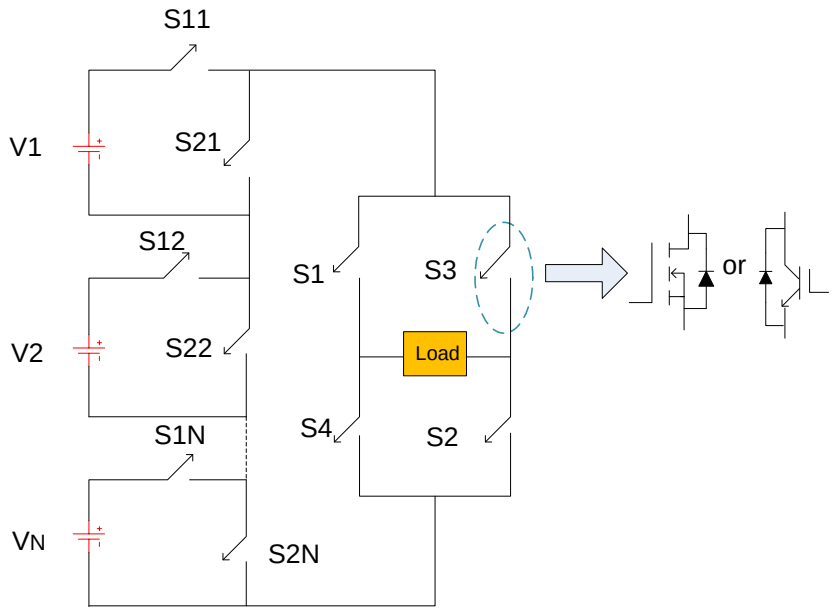


Figure 1.6. Cascaded half bridge based MLI reference [1.34]

MOSFET or IGBT is used for MLI design to operate it in high voltage application. The performance of an 11-level cascaded half bridge MLI with 5 DC voltage sources has been explained thoroughly in [1.34].

b- To reduce the number of switches, installation area, and converter cost E Babaei has introduced a new cascaded MLI in the year 2008. The extended design of the proposed MLI by combining number of submodules has also been presented in [1.35]. The basic structure of the MLI is shown in figure 1.7.

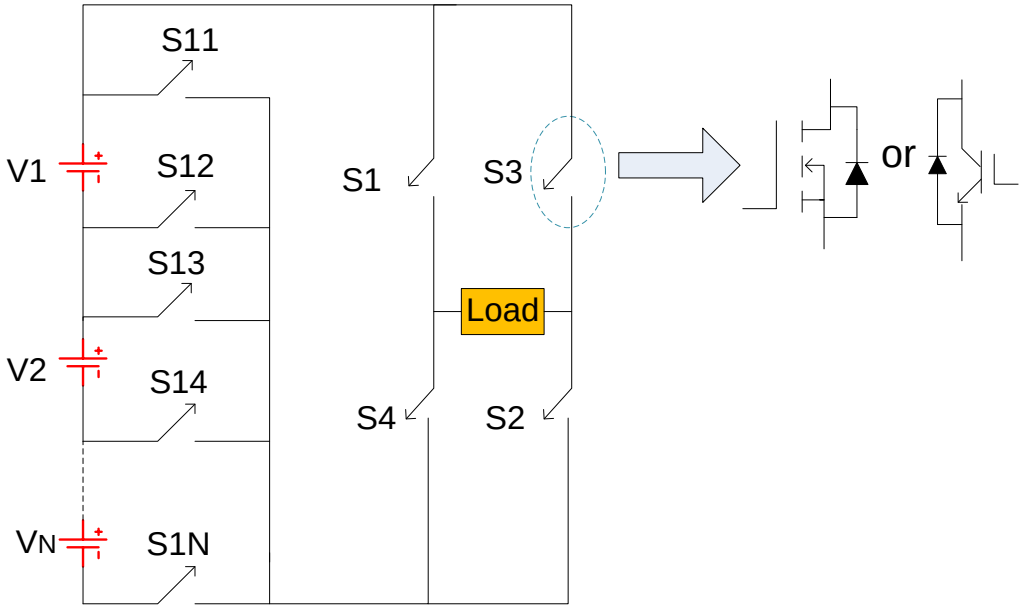


Figure 1.7. Cascaded MLI with reduced structure [1.35]

c- A novel topology of H-bridge based MLI has been introduced by WK Choi and Feel-Soon Kang in the year 2009. In the literature [1.36], the working of a 7-level proposed MLI with PWM switching technique has been discussed. This MLI results same output voltage level for both symmetrical and asymmetrical input voltage sources.

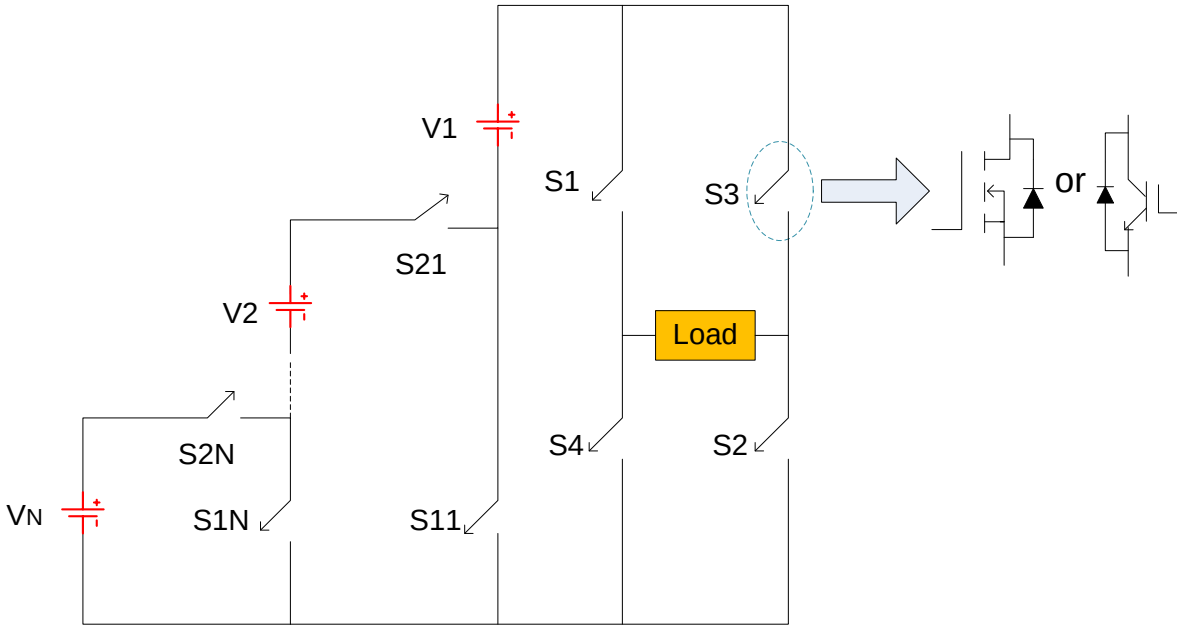


Figure 1.8. Reduced switch H-bridge MLI [1.36]

d- A new 7-level reduced switch MLI has been introduced by EN Najafi and AH Mohamed Yatim in the year 2012. This reduced MLI can be designed for higher output voltage level with suitable number of power switches across the DC voltage sources as shown in figure 1.8.

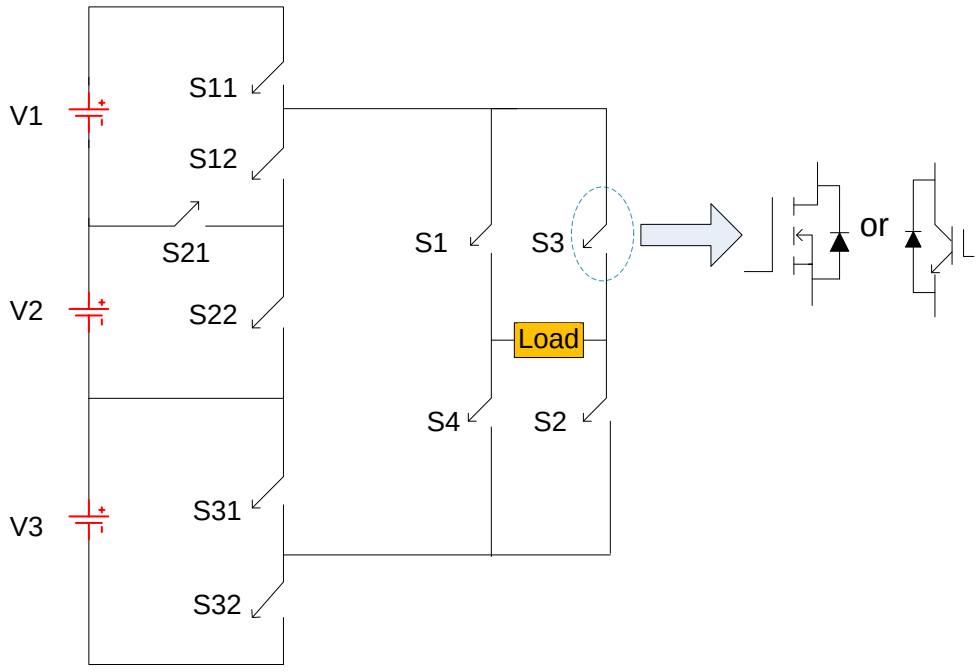


Figure 1.9. 7-level reduced switch MLI [1.37]

The above reduced MLIs use an H-bridge across the load to develop the staircase voltage waveform for both half cycles.

The requirement of switching devices, driver circuits with respect to the output voltage level and number of input DC voltage sources for the above discussed MLIs and CHBMLI is presented in Table 1.1.

Table 1.1 Comparative study of existing reduced MLI with CHBMLI

MLI Topologies	No of input sources	Output Voltage level	No of power switches	No of diodes	No of Driver circuits
CHBMLI	N	2N+1	4N	4N	4N
[1.34]	N	2N+1	2(N+2)	2(N+2)	2(N+2)
[1.35]	N	2N+1	N+5	N+5	N+5
[1.36]	N	2N+1	2(N+1)	2(N+1)	2(N+1)
[1.37]	N	2N+1	2(N+2)	2(N+2)	2(N+2)

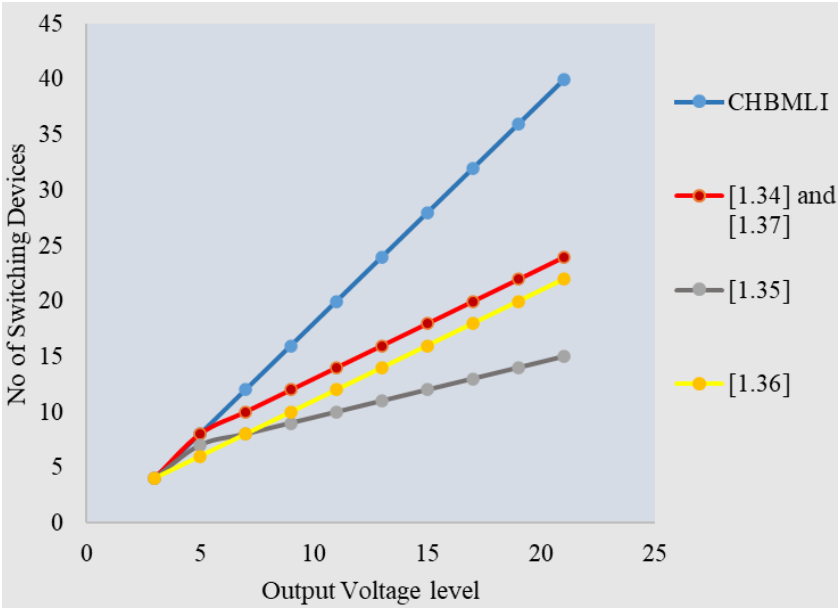


Figure 1.10. No of Switching devices vs Output voltage level for different MLIs

The reduced MLIs that has discussed in this section require smaller number of power switches to develop higher output voltage level using symmetrical DC voltage sources in comparison to CHBMLI. Among the above discussed MLIs, topologies developed in [1.34] and [1.37], and CHBMLI can able to generate higher output voltage level using 'N' number of asymmetrical DC sources than the same number of symmetrical DC sources. For obtaining higher voltage level the number of switching devices required for the above MLIs are presented graphically in figure 1.10 according to Table 1.1.

Apart from these some novel reduced MLI topologies are invented by the researchers with better efficiency and compact structure without H-bridge. The literature reviews on these topologies are discussed in next chapters.

1.4 INTRODUCTION TO OPTIMIZATION FOR HARMONIC REDUCTION

1.4.1 Optimization

Optimization problem is all over the place, just like reaching to a destination with minimum time, higher profit with minimum investment, maximum production to fulfil the demand with minimum resources, and minimizing the error to achieve the best result. In short optimization defines maximizing or minimizing the function satisfying some boundary conditions or constraints. The Constraints are the essential part of optimization problem which need to satisfy for obtaining the best solution. There are various boundary conditions established in different engineering problems or real-life problems which increases the difficulties to design the mathematical formulation. To optimize a function and to achieve the best solution three basic steps are followed.

i. Designing the mathematical formulation.
ii. Implementing the suitable algorithm to solve the problem.
iii. Verifying the best solution that satisfies the demand.

Mathematically the optimization problem can be represented as:

Maximize or Minimize $y = f(x_1, x_2, \dots x_n)$ (1.5)

Based on

$g_j(x) = or \leq or \geq 0, j = 1,2 \dots . s$ (1.6)

Where x_1, x_2….x_n are the variables to be controlled.

There are different mathematical optimization methods are implemented to solve the problem like gradient method, linear and nonlinear programming, network flow theory, simplex algorithm, dynamic optimization and so on. But these optimization techniques have the limitations with the variable size. If the numbers of variable incorporated with the problem increases, the computational cost also increases which makes the process slower.

Instead of these mathematical techniques, some algorithms are developed based on the behaviour of different organism. Evolutionary Computing (EA) and Swarm intelligence are implemented to design the optimization algorithm for solving the complex engineering problem in a simpler way. Genetic Algorithm (GA) is an evolutionary computing technique which inspired from the evolution of the chromosomes. To get the best solution set of population are initialized and the population are evolved through crossover and mutation process. After the mutation the new population gives the better solution than the former one. Another optimization algorithm based on evolutionary computation has been developed in 2002 known as Bacterial Foraging Optimization Algorithm (BFOA). This algorithm inspired from the foraging behaviour of E Coli bacterial. In this case the best solution has been achieved by following chemotaxis, swarming, reproduction, and dispersal steps of the bacterial. Optimization Algorithm based on swarm intelligence influenced from the biological behaviour of different groups of organism or species to search their food, hunting the prey or mating behaviour like ant colony optimization, particle swarm optimization, firefly optimization, grey wolf optimization etc.

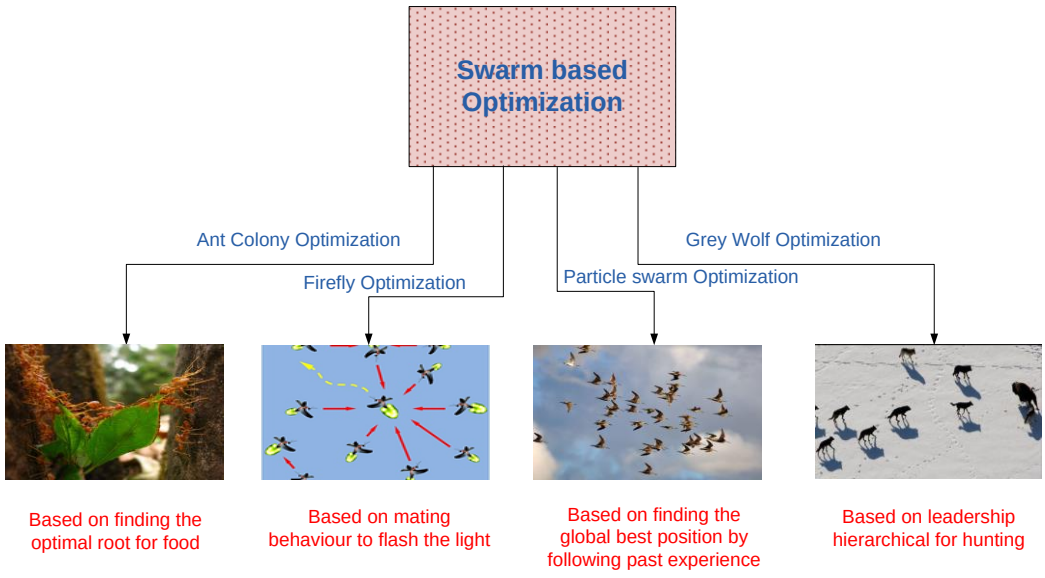


Figure 1.11. Swarm based optimization techniques

In the above discussed algorithms initialization of population is essential to initiate the algorithm and the population size depends on the problem.

1.4.2 Application of Optimization algorithm for harmonic reduction

In this research, application of different MLI topologies for PV-Grid integration, development of new reduced switch MLI with better efficiency and better power quality has been carried out. For efficient power conversion through MLI can be done by obtaining suitable switching angles which minimize the output voltage distortion. Here to obtain the optimal switching angles for the MLI different bio inspired algorithm has been implemented which are discussed in next chapters. The switching angles of the MLI are considered as the population for different algorithm in this research. The basic flowchart diagram in order to get the minimum voltage THD has been given below.

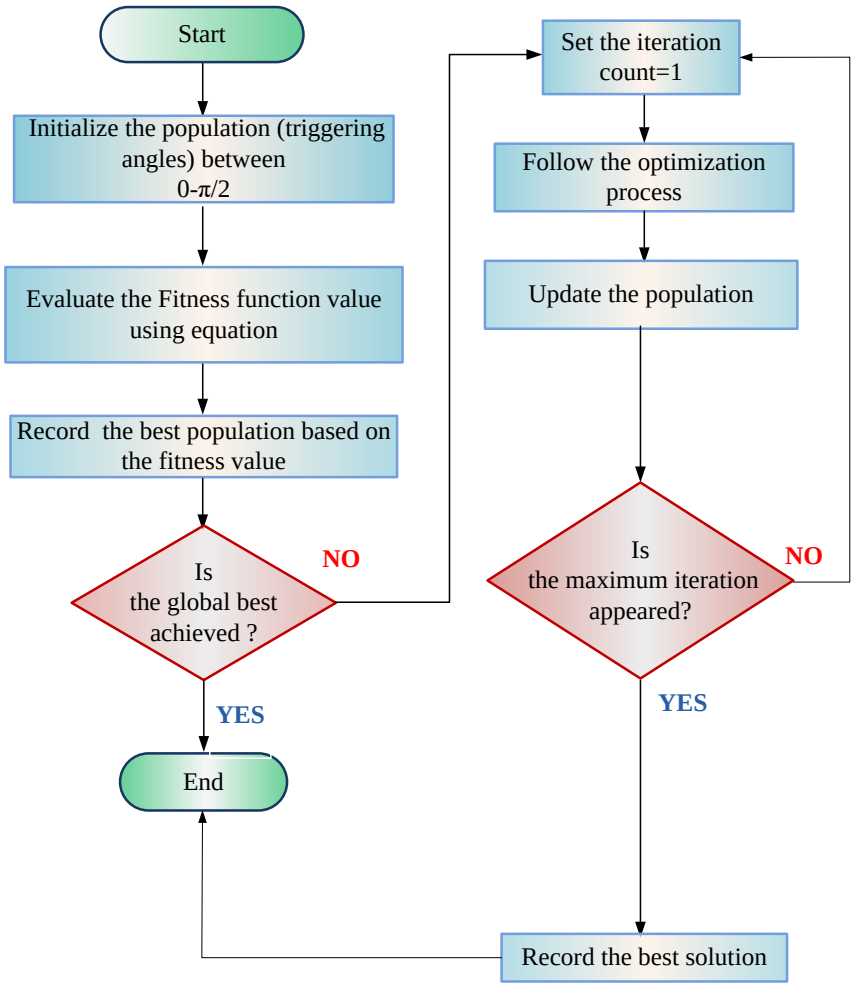


Figure 1.12. Flowchart to get the optimum switching angles for the MLI

1.5 MOTIVATION OF THE RESEARCH

As discussed in the introduction section, Conversion of lower capacity solar energy to higher one and integration with low, medium, and high voltage grid with proper control technique is the biggest challenge. To avoid the bulky step-up transformer in power conversion stage Multilevel Inverter has provided the efficient solution. For higher voltage application the MLI requires higher number of voltage sources and switching devices. Higher number of power devices also increase the complexity in switching techniques. This shortcoming of conventional MLI has motivated this research towards development of reduced switch MLI with smaller number of power devices, use of minimum number of input sources, and developing the optimal solution to generate suitable switching angles for the reduced MLIs with improved power quality.

1.6 OBJECTIVES OF THE RESEARCH

Importance of Multilevel Inverters for grid integration, power conversion and industrial application has already been discussed in section 1.1 and 1.2. For higher voltage application the MLIs with higher voltage level is preferred which increases the input DC voltage sources and power devices. To reduce the distortion across MLI output voltage suitable switching scheme is required. Considering these above issues, the objectives of the research have been designed and discussed below.

a- Design of reduced switch Multilevel Inverter with minimum number of switching devices, minimum switching loss and, higher output voltage level.

b- Implementation of proposed Multilevel Inverters scheme for grid interconnection with better transient response and lower number of input sources.

c- To find out the optimal solution for minimization of THD in a simple manner with less computational time.

d- Implementation of suitable control scheme for grid integration of MLI.

1.7 ORIENTATION OF THESIS

The research work to satisfy the objectives is organised accordingly and presented in different chapters.

Chapter 1: This chapter gives the introductory idea about necessity of multilevel inverters, advantages, and disadvantages of the MLIs developed initially. Review on different topology of reduced switch MLIs and the comparative study with H-bridge MLI is also presented. Overview of optimization technique and application of optimization algorithm to minimize the THD of MLI output voltage has been discussed.

Chapter 2: This chapter presents the working of an 11-level cross switch MLI. The THD minimization of its output voltage using particle swarm optimization has been discussed. The power loss calculation has been carried to determine the efficiency of the MLI. The simulation results of a single phase cross switch MLI with minimum voltage distortion has been discussed.

Chapter 3: In this chapter the proposed scheme for PV-Grid integration using asymmetrical cross switch MLI is discussed. The MLI operation with a single PV source by using an isolated converter is carried out. The voltage distortion across the output of reduced MLI has been minimized with the help of Black Widow Optimization algorithm and the performance of proposed algorithm is verified by comparative study with other existing nature-based algorithm.

Chapter 4: In this chapter a proposed hybrid reduced switch MLI is presented. Operation of this MLI and efficiency has been observed and presented. Application of the proposed MLI for PV standalone system is presented. The output voltage THD of the hybrid MLI is reduced by implementing modified JAYA algorithm which is discussed in this chapter and the results are discussed in detail.

Chapter 5: This chapter presents a single active source based asymmetrical MLI for PV-Grid integration. The optimum switching angles and input voltage ratios are determined through a metaheuristic algorithm called Red Deer Optimization algorithm for minimum voltage distortion. The performance of Red Deer Optimization algorithm has been

demonstrated by designing an 11-level reduced switch MLI. The simulation results and hardware results are presented in this chapter.

Chapter 6: This chapter introduces the operation of asymmetrical cascaded H-bridge MLI for grid integration. The total harmonic distortion across output and grid side has been minimized by suitable switching angles derived from Honey Badger Optimization algorithm. The efficacy of the algorithm has been proved by statistical analysis with other existing nature inspired algorithm. The comparative study has been carried out and shown in this chapter. The performance of the MLI for grid integration has been carried out through real time simulation and results are shown.

Chapter 7: This chapter proposes a S-Cross reduced switch MLI with minimum number of DC voltage sources. The operation of the proposed MLI with minimum number of power switches is explained briefly. The output voltage distortion is minimized with the help of Black Widow Optimization algorithm and overall THD has been shown. The proposed MLI is integrated with grid to verify the efficiency through real time simulator. The prototype of the MLI has been built for both grid connection and isolated condition.

1.8 REFERENCES

[1.1] R. Ramakumar, H. J. Allison, and W. L. Hughes, “Solar energy conversion and storage systems for the future,” no. 6, 1975.

[1.2] A. Gil, A. Castell, E. Oro, B. L. F. Cabeza, and C. Sole, “Review of Solar Thermal Storage Techniques and Associated Heat Transfer Technologies,” vol. 100, no. 2, pp. 525–538, 2012.

[1.3] R. Sioshansi and P. Denholm, “The Value of Concentrating Solar Power and Thermal Energy Storage,” vol. 1, no. 3, pp. 173–183, 2010.

[1.4] B. M. Kleinberg *et al.*, “Different Storage Forms and Functions in Transmission and Distribution Applications,” 2014.

[1.5] H. Beltran, E. Pérez, N. Aparicio, P. Rodríguez, and S. Member, “Daily Solar Energy Estimation for Minimizing Energy Storage Requirements in PV Power Plants,” vol. 4, no. 2, pp. 474–481, 2013.

[1.6] A. K. Barnes, S. Member, J. C. Balda, and S. Member, “A Semi-Markov Model for Control of Energy Storage in Utility Grids and Microgrids With PV Generation,” vol. 6, no. 2, pp. 546–556, 2015.

[1.7] A. Murtaza, M. Chiaberge, M. De Giuseppe, and D. Boero, “Electrical Power and Energy Systems A duty cycle optimization based hybrid maximum power point tracking technique for photovoltaic systems,” *Int. J. Electr. Power Energy Syst.*, vol. 59, pp. 141–154, 2014, doi: 10.1016/j.ijepes.2014.02.009.

[1.8] I. Houssamo, F. Locment, and M. Sechilariu, “Electrical Power and Energy Systems Experimental analysis of impact of MPPT methods on energy efficiency for photovoltaic power systems,” *Int. J. Electr. Power Energy Syst.*, vol. 46, pp. 98–107, 2013, doi: 10.1016/j.ijepes.2012.10.048.

[1.9] L. Zhang, S. Member, W. G. Hurley, and W. H. W, “A New Approach to Achieve Maximum Power Point Tracking for PV System With a Variable Inductor,” vol. 26, no. 4, pp. 1031–1037, 2011.

[1.10] C. Moo, G. Wu, and S. Member, “Maximum Power Point Tracking With Ripple

Current Orientation for Photovoltaic Applications," vol. 2, no. 4, pp. 842–848, 2014.

[1.11] A. I. M. Ali, M. A. Sayed, and E. E. M. Mohamed, "Electrical Power and Energy Systems Modi fi ed e ffi cient perturb and observe maximum power point tracking technique for grid-tied PV system," *Electr. Power Energy Syst.*, vol. 99, no. December 2017, pp. 192–202, 2018, doi: 10.1016/j.ijepes.2017.12.029.

[1.12] A. D. Karlis, T. L. Kottas, and Y. S. Boutalis, "A novel maximum power point tracking method for PV systems using fuzzy cognitive networks (FCN)," vol. 77, pp. 315–327, 2007, doi: 10.1016/j.epsr.2006.03.008.

[1.13] J. Shi, W. Zhang, Y. Zhang, F. Xue, and T. Yang, "MPPT for PV systems based on a dormant PSO algorithm," *Electr. Power Syst. Res.*, vol. 123, pp. 100–107, 2015, doi: 10.1016/j.epsr.2015.02.001.

[1.14] S. Mohanty, B. Subudhi, and P. K. Ray, "A new MPPT design using grey Wolf optimization technique for photovoltaic system under partial shading conditions," *IEEE Trans. Sustain. Energy*, vol. 7, no. 1, pp. 181–188, 2016, doi: 10.1109/TSTE.2015.2482120.

[1.15] Y. Kuo, T. Liang, and J. Chen, "A High-Efficiency Single-Phase Three-Wire," vol. 50, no. 1, pp. 116–122, 2003.

[1.16] N. Afrin, F. Yang, and J. Lu, "Electrical Power and Energy Systems Voltage support strategy for PV inverter to enhance dynamic voltage stability of islanded microgrid," *Electr. Power Energy Syst.*, vol. 121, no. April, p. 106059, 2020, doi: 10.1016/j.ijepes.2020.106059.

[1.17] J. M. Guerrero and D. Ghaderi, "International Journal of Electrical Power and Energy Systems Grid code compatibility and real-time performance analysis of an efficient inverter topology for PV-based microgrid applications," vol. 128, no. April 2020, 2021, doi: 10.1016/j.ijepes.2020.106712.

[1.18] L. S. Gusman, H. A. Pereira, J. M. S. Callegari, and A. F. Cupertino, "Electrical Power and Energy Systems Design for reliability of multifunctional PV inverters used in industrial power factor regulation," *Electr. Power Energy Syst.*, vol. 119, no. July 2019, p. 105932, 2020, doi: 10.1016/j.ijepes.2020.105932.

[1.19] D. Sun, B. Ge, D. Bi, and F. Z. Peng, "Electrical Power and Energy Systems Analysis

and control of quasi-Z source inverter with battery for grid-connected PV system q," *Int. J. Electr. Power Energy Syst.*, vol. 46, no. 2009, pp. 234–240, 2013, doi: 10.1016/j.ijepes.2012.10.008.

[1.20] J. Lai, S. Member, and F. Z. Peng, "Multilevel Converters-A New Breed of Power Converters," vol. 32, no. 3, pp. 509–517, 1996.

[1.21] V. Sonti, S. Jain, and S. Bhattacharya, "Analysis of the Modulation Strategy for the Minimization of the Leakage Current in the PV Grid-Connected Cascaded Multilevel Inverter," vol. 32, no. 2, pp. 1156–1169, 2017.

[1.22] N. Kumar, T. K. Saha, and J. Dey, "Electrical Power and Energy Systems Modeling , control and analysis of cascaded inverter based grid-connected photovoltaic system," *Int. J. Electr. Power Energy Syst.*, vol. 78, pp. 165–173, 2016, doi: 10.1016/j.ijepes.2015.11.092.

[1.23] F. Wu, X. Li, F. Feng, and H. Gooi, "Electrical Power and Energy Systems Efficiency enhancement scheme of cascaded multilevel grid-connected inverter and its improvement to eliminate effect of non-ideal grid conditions," *Int. J. Electr. Power Energy Syst.*, vol. 76, pp. 120–128, 2016, doi: 10.1016/j.ijepes.2015.10.001.

[1.24] A. Lashab *et al.*, "A Reduced Power Switches Count Multilevel Converter-Based Photovoltaic System With," vol. 68, no. 9, pp. 8231–8240, 2021.

[1.25] S. Technique, S. Dhara, S. Member, A. Hota, S. Member, and S. Jain, "Inverter Configuration Based on," vol. 57, no. 2, pp. 1619–1628, 2021.

[1.26] N. M. C. M, P. Jayaprakash, and S. Member, "Realization of Cascaded H-Bridge Multilevel Inverter Based Grid Integrated Solar Energy System With Band Stop Generalized Integral Control," vol. 57, no. 1, pp. 764–773, 2021.

[1.27] R. Agrawal and S. Jain, "Electrical Power and Energy Systems Comparison of reduced part count multilevel inverters (RPC-MLIs) for integration to the grid," *Int. J. Electr. Power Energy Syst.*, vol. 84, pp. 214–224, 2017, doi: 10.1016/j.ijepes.2016.05.011.

[1.28] S. K. Kuncham, K. Annamalai, and S. Member, "A Two-Stage T-Type Hybrid Five-Level Transformerless Inverter for PV Applications," vol. 35, no. 9, pp. 9510–9521, 2020.

[1.29] C. M. N. Mukundan and P. Jayaprakash, “Binary Hybrid Multilevel Inverter-Based Grid Integrated Solar Energy Conversion System With Damped SOGI Control,” *IEEE Access*, vol. 8, no. Mli, pp. 37214–37228, 2020, doi: 10.1109/ACCESS.2020.2974773.

[1.30] C. Cecati, F. Ciancetta, and P. Siano, “A Multilevel Inverter for Photovoltaic Systems With Fuzzy Logic Control,” vol. 57, no. 12, pp. 4115–4125, 2010.

[1.31] P. Manoj, K. Annamalai, S. Member, S. Dhara, G. S. Member, and V. T. Somasekhar, “A Quasi-Z-Source-Based Space-Vector-Modulated Cascaded Four-Level Inverter for Photovoltaic Applications,” vol. 10, no. 4, pp. 4749–4762, 2022.

[1.32] M. Systems, R. Gupta, S. Member, A. Ghosh, and A. Joshi, “Switching Characterization of Cascaded,” vol. 55, no. 3, pp. 1047–1058, 2008.

[1.33] P. C. Loh, D. G. Holmes, and T. A. Lipo, “Implementation and Control of Distributed PWM Cascaded Multilevel Inverters With Minimal Harmonic Distortion and Common-Mode Voltage,” vol. 20, no. 1, pp. 90–99, 2005.

[1.34] E. Babaei and S. H. Hosseini, “New cascaded multilevel inverter topology with minimum number of switches,” *Energy Convers. Manag.*, vol. 50, no. 11, pp. 2761–2767, 2009, doi: 10.1016/j.enconman.2009.06.032.

[1.35] E. Babaei, “A cascade multilevel converter topology with reduced number of switches,” *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2657–2664, 2008, doi: 10.1109/TPEL.2008.2005192.

[1.36] W. Choi and F. Kang, “H-bridge based Multilevel Inverter using PWM Switching Function”.

[1.37] E. Najafi and A. H. M. Yatim, “Design and implementation of a new multilevel inverter topology,” *IEEE Trans. Ind. Electron.*, vol. 59, no. 11, pp. 4148–4154, 2012, doi: 10.1109/TIE.2011.2176691.

Chapter-2

Cross Switch Reduced MLI

The performance of an eleven level Cross Switch Multilevel inverter has been described in this chapter. The switching loss of this MLI has been calculated to determine the efficiency. The switching pulses are generated with the help of PSO algorithm and the overall output voltage THD determined from the simulation is presented.

CROSS SWITCH REDUCED MLI

2.1 INTRODUCTION

Multilevel Inverters are suitable for high power application by using lower rating power devices as discussed in chapter 1. For grid integration and industrial applications, researchers have developed reduced switch MLIs to make up for the shortcomings of CHBMLI. The various multilevel inverter topologies and their underlying operational principles are introduced in [2.1]. The switching control and removal of unwanted harmonics from the output voltage are critical concerns with the new topology. To reduce voltage THD (Total Harmonic Distortion), a number of modulation approaches and algorithms are proposed in [2.2], [2.3], [2.4], and [2.5]. Using the Particle Swarm Optimisation (PSO) technique, this chapter details the functionality of a single-phase reduced switch MLI. As described in [2.7], the inverter with a crossed-switch voltage source has an impact on the design of this reduced-switch MLI. While [2.6] delves into the effectiveness and operating principle of Cross Switch MLI, it fails to specifically address how this MLI might be used to lessen harmonic distortion. Here, the efficacy of the above MLI for THD optimisation is analysed in depth, and the results are presented in Section 2.6.

2.2 WORKING PRINCIPLE of CROSS SWITCH MLI

In this chapter, an 11-level cross switch MLI with equal voltage sources was analysed and simulated using the PSO algorithm to make it appropriate for PV energy conversion, as discussed in the literature [2.8]. In Cascade H-Bridge MLI, the output voltage level is determined by (2N+1) where 'N' the number of voltage sources and the number of power devices is determine by 4N. But in case of CSMLI for getting (2N+1) voltage level, 2(N+1) number of power devices are required. This MLI can be used in both single phase and three phase by proper arrangement. For getting the suitable switching angles to optimize the voltage THD, PSO algorithm has been implemented. It takes 12 power switches and 5 DC voltage sources to build a single phase 11-level CSMLI. The single phase circuit diagram of the reduced MLI with 'N' number of DC voltage sources has been shown in figure 2.1. The switching pattern to operate the 11-level CSMLI has been given in Table 2.1. The operation of the above MLI is explained in five mode and shown in figure 2.3.

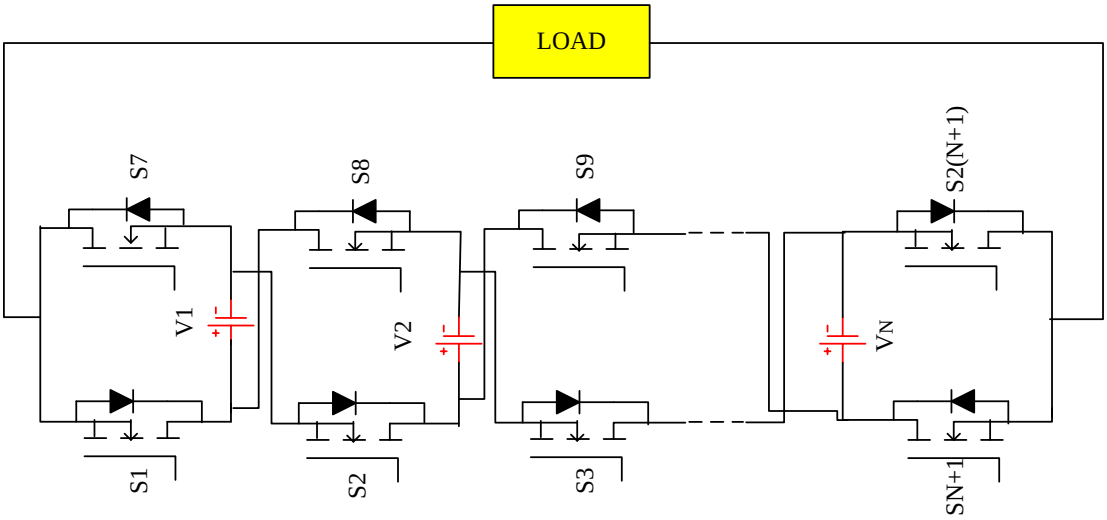


Figure 2.1. Circuit arrangement of single phase CSMLI with 'n' number of sources

In this research, the MLI is powered with equal voltage sources. So, in the above figure it can be considered that V1=V2=V3=…….=V_N= V_D.

Table 2.1. Switching Pattern for 11-level CSMLI

Switching combinations for each voltage level										
Switches	V_D	$2V_D$	$3V_D$	$4V_D$	$5V_D$	$-V_D$	$-2V_D$	$-3V_D$	$-4V_D$	$-5V_D$
S1	1	1	1	1	1	0	0	0	0	0
S2	1	1	1	1	1	0	0	0	0	0
S3	0	1	1	1	1	1	0	0	0	0
S4	1	0	1	1	1	0	1	0	0	0
S5	0	1	0	1	1	1	0	1	0	0
S6	1	0	1	0	1	0	1	0	1	0
S7	0	0	0	0	0	1	1	1	1	1
S8	0	0	0	0	0	1	1	1	1	1
S9	1	0	0	0	0	0	1	1	1	1
S10	0	1	0	0	0	1	0	1	1	1
S11	1	0	1	0	0	0	1	0	1	1
S12	0	1	0	1	0	1	0	1	0	1

In the above table switching ON and switching OFF the switch are presented by state '1' and '0' respectively. The 11-level output voltage of the reduced MLI has been shown in figure 2.2. To obtain this staircase voltage waveform, operation of the MLI has been explained by following the switching pattern given in Table 2.1.

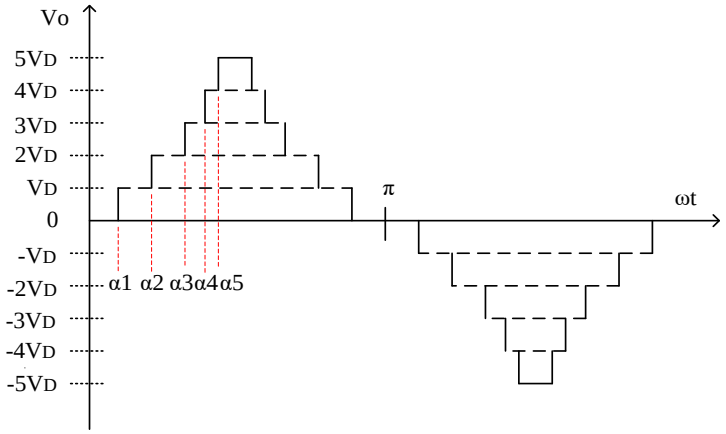
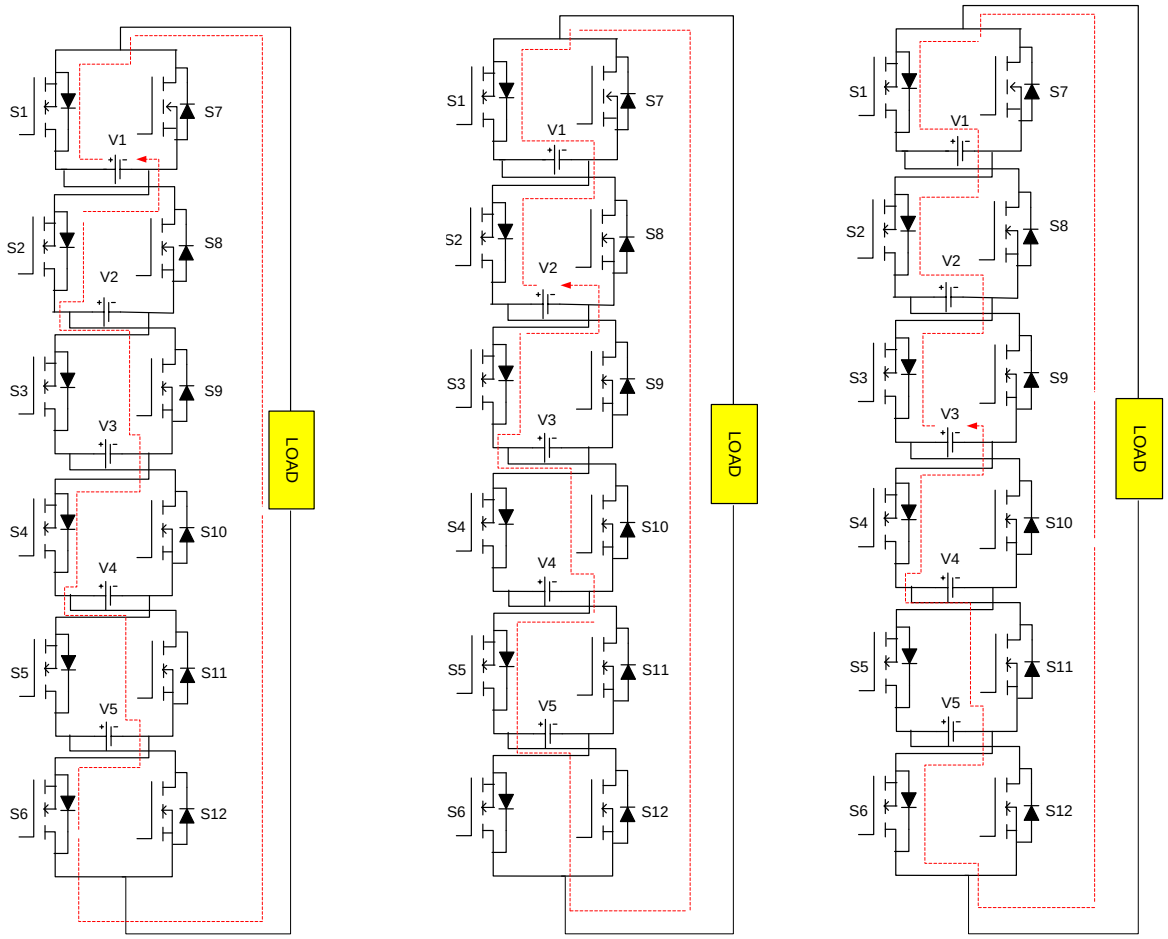
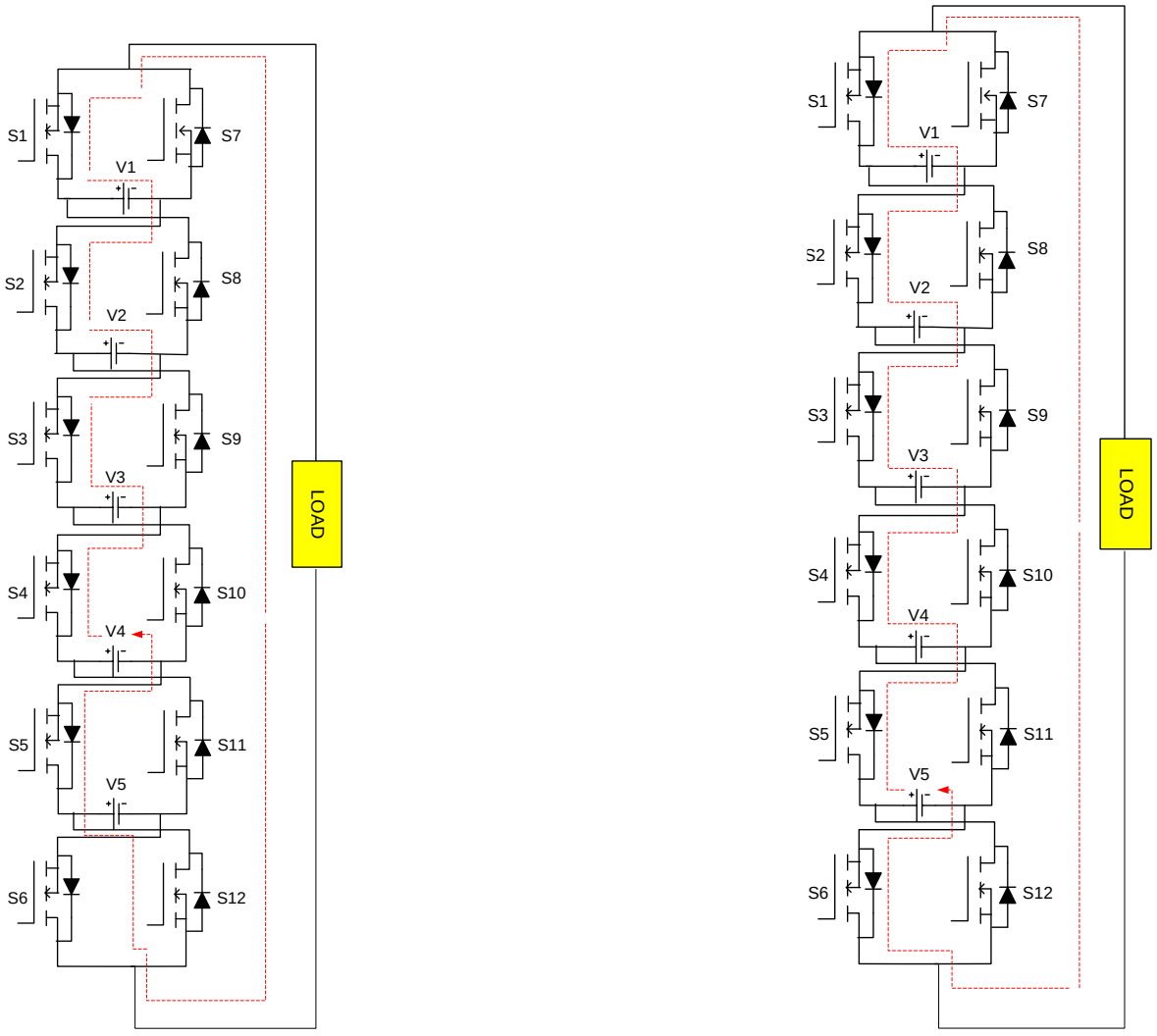


Figure 2.2. 11-level voltage waveform



(a) (b) (c)



(d) (e)

Figure 2.3. Circuit operation of 11-level CSMLI. (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5

In each mode six power switches are triggered on to get the desired output. In mode 1, the MLI output voltage is V_D across the load and the current direction is denoted by an arrow as shown in the figure. In mode 2, V1 and V2 combinedly charge the MLI. Therefore, the output voltage across the load is $V1+V2=2V_D$. Mode 3 has been explained in figure 2.3(c) which results $V1+V2+V3=3V_D$ across the load. In mode 4 the MLI output voltage is $V1+V2+V3+V4=4V_D$ as shown in figure 2.3(d). The maximum positive output voltage across the load is $V1+V2+V3+V4+V5=5V_D$ which is explained in mode 5. Similarly, by following Table 2.1, the circuit can be operated accordingly for generating negative half

cycle voltage across the load. This reduced MLI exhibits maximum positive voltage of $5V_D$ and maximum negative voltage of $-5V_D$ across the load.

2.3 PROPOSED PSO BASED HARMONIC ELIMINATION TECHNIQUE

To get the suitable switching angles for MLI operation unipolar pulse width modulation (PWM) [2.9] or common PWM [2.10] are applied with higher switching frequency which, increases the switching losses. But to operate the MLI in fundamental frequency, swarm based optimization is implemented here. In this research an 11-level reduced multilevel inverter is studied and simulated for obtaining the minimum output voltage THD. For achieving the desired result, PSO algorithm is implemented to get the appropriate triggering angles of CSMLI.

2.3.1 Mathematical Formulation

The expression of output voltage can be determined by using Fourier series analysis. As all the voltage sources are of equal value and the output voltage waveform is quarter wave symmetry, it can be derived as:

$$V(\omega t) = \sum_{\alpha=1}^{ai} \frac{4V_D}{n\pi} (\cos(n\alpha_1) + \cos(n\alpha_2) + \cdots + \cos(n\alpha_{ai}))\sin(\omega t) \quad (2.1)$$

V_D is the DC input voltage to the MLI for each level and $\alpha_1, \alpha_2 \ldots\ldots\ldots \alpha_{ai}$ are the triggering angles which must need to gratify the below condition.

$$\alpha_1 < \alpha_2 < \cdots \alpha_{ai} < \frac{\pi}{2} \quad (2.2)$$

The fitness function which has been optimized in this chapter is Total Harmonic Distortion from load voltage and this has been achieved using PSO algorithm. The fitness function is given by equation (2.3).

$$THD\% = \frac{\sqrt{\sum_{n=3,5\ldots}^{49} V_n^2}}{V_1} * 100 \quad (2.3)$$

The fundamental output voltage is given by V_1 and 'n' is the no of odd harmonics present in the output voltage.

2.3.2 Particle Swarm Optimization (PSO)

Russell Eberhart and James Kennedy has proposed PSO algorithm in 1995.This Algorithm has influenced by the social behaviour of swarm like bird flocks and fish school. Here the system is getting the optimize solution by randomly initializing the population and achieved the optimal value by updating the position of the population. The particles follow the best search of individual (Pbest) and groups (Gbest). As per these records the particle updates their velocity (which accelerate the position of particles) and position with the help of following equations.

$$v(t+1) = \omega[v(t) + C1R1(Pbest - P(t)) + C2R2(Gbest - P(t))] \quad (2.4)$$

Position of the Particle is being updated by equation (2.5).

$$P(t+1) = P(t) + v(t+1) \quad (2.5)$$

Where,

P(t)=Current location of the individual particle.

v(t)=Current velocity of the particle.

P_{best}= Best position determined by the individual particle.

G_{best}=Best position determined by the group of particles.

C1,C2 = Syllogistic and communal parameter.

R1,R2 = Random number between 0 and 1.

The compacting or constriction factor that has been built in to satisfy and upgrade the convergence characteristic of PSO algorithm is given by 'ω'. This is expressed by:

$$\omega = \frac{2}{|2-C-\sqrt{C^2-4C}|} \quad \text{subject to } C=C1+C2;\ C>4 \tag{2.6}$$

2.3.3 Application of PSO Algorithm in CSMLI

Particle current position or the triggering angles vector is presented by the i^{th} particle which is given by $\alpha i = [\alpha i_1, \alpha i_2 \ldots \alpha i_n]$. Particle positions are randomly initiated and the best value is used for solving the harmonic minimization problem. The following steps are designed to solve the THD optimization problem.

Steps:

1- This algorithm is started with by allocating the population size as P and maximum iteration as Itermax. The iteration counter is set to iter=1.

2- Individual particle positions (the triggering angle) are assigned aimlessly between 0 to π/2 and the particle velocity (voltage) are assigned aimlessly between −Vmax and Vmax.

3- Individual particle has been checked out by fitness function of the harmonic optimization problem. Fitness function of the problem is determined by equation (2.7).

$$F = \frac{\sqrt{\sum_{n=3,5\ldots}^{49} V_n^2}}{V_1} \tag{2.7}$$

4- Now the personal best position of the particle has been updated. The present position of the i^{th} particle has been compared with the former personal best position and if the present one is better, then Pi has been replaced with the current position p(t). The personal best (Pbest) and global best (Gbest) of the particle has been compared and if Pbest is better than Gbest then Gbest is replaced with the best position of the personal best.

5- The velocity of all the particles is updated by using equation (2.4) and then the position of the particles is updated using equation (2.5).

6- Termination process: When the iteration count reached to itermax, the algorithm will be terminated. Otherwise, the iteration will start again by counting iter =iter +1 and it will return to step (3).

2.4 SIMULATION RESULTS

The optimum switching angles for the 11-level CSMLI are obtained from the PSO algorithm using MATLAB program. The five switching angles that provided the minimum voltage THD are: α_1=3.65, α_2=17.86, α_3=30.44, α_4=45.68, α_5=60.88 in degrees. The overall voltage THD obtained from the MATLAB program is 4.8% at modulation index 0.8. Where modulation Index can be determined by:

$$MI = {Fundamental\ Output\ Voltage(V_1)}\Big/{Maximum\ Voltage\ (V_{max})} \quad (2.8)$$

The characteristic of voltage THD with respect to modulation index developed from PSO algorithm is shown in figure 2.4

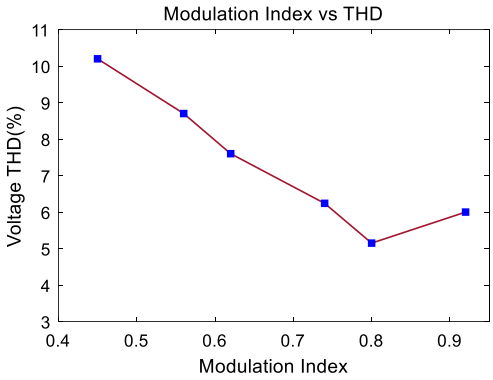
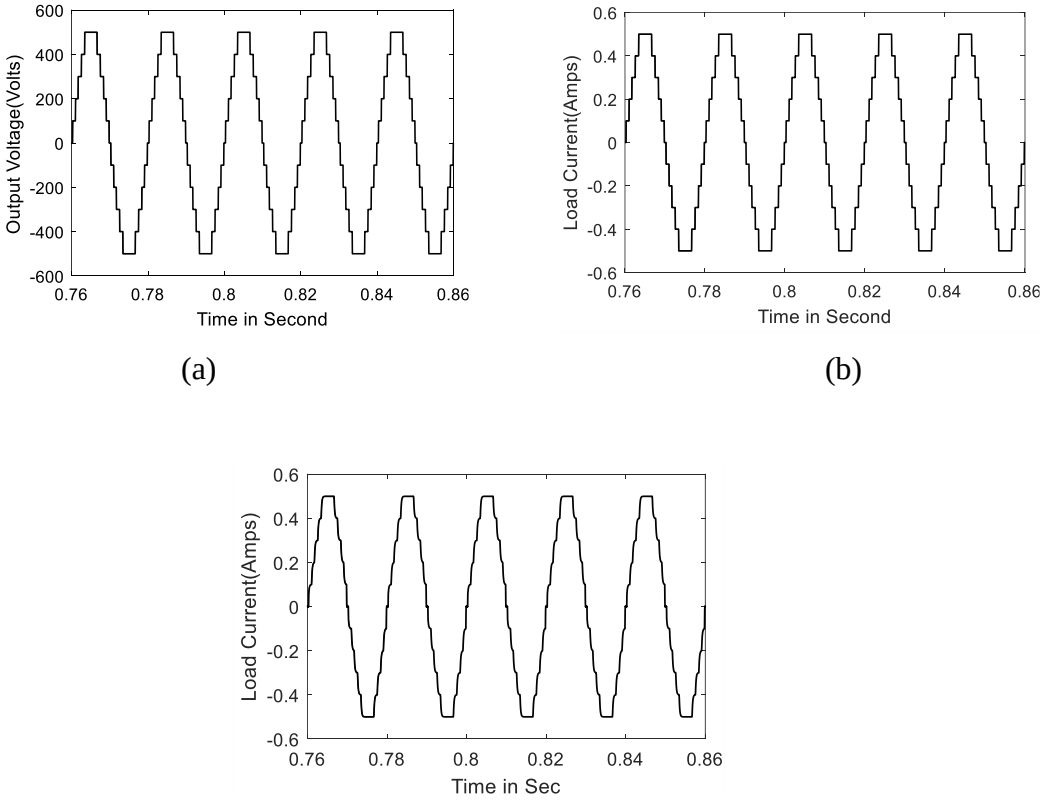


Figure 2.4. Modulation Index vs THD graph

The programming result is verified through MATLAB simulation by developing a single phase 11-level CSMLI with equal voltage sources of 100volts each. The CSMLI is operated by generating the triggering pulse with the help of above switching angles and the output voltage and current are obtained across the RL load of 1000ohm and 150mH. The output voltage waveform, current waveform with pure resistive load of 1000ohm and RL load are shown in figure 2.5.

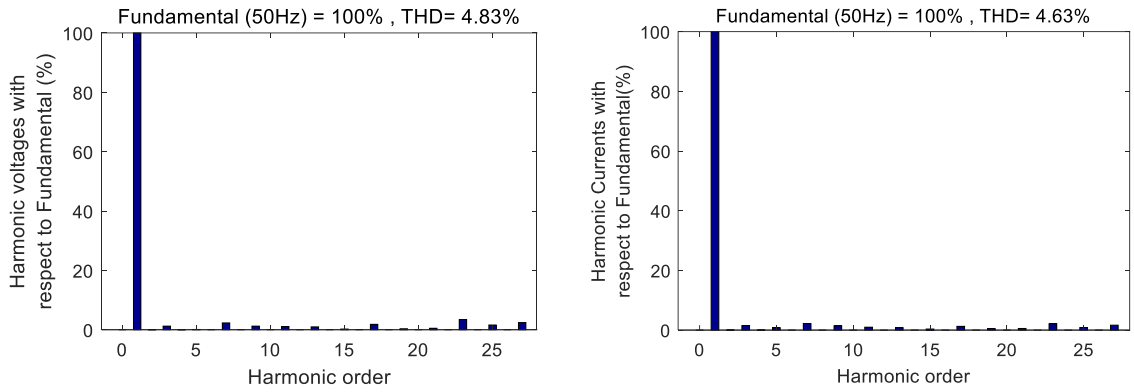


(a) (b)

(c)

Figure 2.5. (a) Output Voltage waveform, Load Current waveform (b) with pure resistive load, (c) with RL load

FFT analysis of the output voltage and load current waveform is performed through MATLAB SIMULINK environment. The load current and voltage harmonic spectrum are shown in figure 2.6.



(a) (b)

Figure 2.6. Harmonic Spectrum (a) Output Voltage (b) Load Current

2.5 SWITCHING LOSS CALCULATION of CSMLI

The power loss across a semiconductor switch is considered during its conduction state and switching state. In this chapter the 11-level CSMLI is studied and simulated with 12 power devices as shown in figure 2.3. In the power devices, on-state resistance can vary with respect to temperature but to simplify the problem, a constant temperature has been considered. The power loss of the device can be calculated as:

$$P_L = P_{conduction} + P_s \tag{2.9}$$

Let V_T is the on state voltage drop of the power device and V_d is the reverse voltage drop of diode, r_T and r_D are the resistance of transistor and diode respectively. The conduction loss of the transistor and reverse conducting diode of a switching device can be determined as:

$$\left.\begin{aligned} P_{LT}(t) &= [V_T + r_T \beta i(t)]i(t) \\ P_{LD}(t) &= [V_d + r_D i(t)]i(t) \end{aligned}\right] \tag{2.10}$$

Here β is assigned as gain constant and *i(t)* is the instantaneous current across the device during conduction. $P_{LT}(t)$, $P_{LD}(t)$ are the instantaneous conduction loss across transistor and reverse conducting diode. The average power loss during conduction depends on the turning on period of a particular switch, so it can be calculated as:

$$\left.\begin{aligned} P_{LT} &= \frac{1}{T}\int_{T1}^{T2}[V_T + r_T\beta i(t]i(t)dt \\ P_{LD} &= \frac{1}{T}\int_{T1}^{T2}[V_d + r_D i(t]i(t)dt \end{aligned}\right] \quad (2.11)$$

Let T1 to T2 is the conduction period of the switch and T is the total time period. Taking the values of V_T, V_d, r_T and r_D from the specification sheet, the power loss for each switch has been calculated as per their conduction by following Table 2.1.β is 1 and current during conduction is 0.4A as load resistance of 1000Ω is used in the simulation model. Putting these values in equation 2.11, the total conduction loss of the reduced MLI is 4.8W.

switching loss for each power switch is calculated at the time of turning on and turning off in the entire cycle. Switching loss is determined by using equation (2.12)

$$P_s = \frac{1}{T}\left[E_{on}N_{on} + E_{off}N_{off}\right] \quad (2.12)$$

Where E_{on} and E_{off} are the on state and off state energy losses respectively of a power switch. N_{on} and N_{off} represent the number of times a power switch is getting on and off respectively over the entire time of operation.

$$\left.\begin{aligned} E_{on} &= \frac{1}{6}[V_{sd}I_s t_{on}] \\ E_{off} &= \frac{1}{6}\left[V_{sd}I_s t_{off}\right] \end{aligned}\right] \quad (2.13)$$

Here V_{sd} is the voltage across a switch before switching on or after switching it off and I_s is the current across switch after switching on or before switching off. The turn on time and turn off time of a particular switching device are represented by t_{on} and t_{off}. Loss during turn

on and turn off for all the switches of CSMLI is calculated to 0.006W. Now the total power loss of the MLI is 4.806W. The output power of the MLI across load is 130W. Considering the output power and total loss of the MLI, the efficiency of the CSMLI is calculated to 96%.

2.6 OBSERVATION

In this chapter, the PSO algorithm has been used to reduce the THD of an 11-level reduced MLI. After determining the optimal switching angles, the findings are validated by MATLAB simulation. The results demonstrate that the inverter's output voltage has been successfully tuned to reduce undesired harmonics up to the 29th order. When applied to a three-phase system, the suggested switching technique cancels out 3rd order harmonics to reduce voltage THD to below 4%. The inverter efficiency required for PV-grid synchronization and other industrial uses is determined by estimating the switching loss of the CSMLI. There are a few small drawbacks to the proposed technique. Higher output voltage levels require a greater number of sources, which can restrict their usefulness. Each switch additionally experiences greater voltage stress in lower switch MLI. These limitations are minimized by developing some new topologies of MLI which are discussed in next chapters.

2.7 PUBLICATION

[1] R.Mohanty, D. Chatterjee, S. Suman and G. Sengupta, "PSO Based Improved Topology for MLI Considering Low THD and Low Switching Loss," 10th International Conference on Computing, Communication and Networking Technologies (ICCVNT), Kanpur,India,2019,pp. 1-5, 2019 doi: 10.1109/ICCCNT45670.2019.8944546.

2.8 REFERENCES

[2.1] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 135–151, 2016, doi: 10.1109/TPEL.2015.2405012.

[2.2] F. Mihalic, M. Milanovic, and A. Hren, "Third harmonic elimination by SPWM for filter reduction in a over-modulated single-phase inverter," *Int. Conf. Electical*

Drives Power Electron., vol. 2017-Octob, pp. 37–45, 2017, doi: 10.1109/EDPE.2017.8123253.

[2.3] K. P. Panda and G. Panda, "Application of swarm optimisation-based modified algorithm for selective harmonic elimination in reduced switch count multilevel inverter," *IET Power Electron.*, vol. 11, no. 8, pp. 1472–1482, 2018, doi: 10.1049/iet-pel.2017.0697.

[2.4] R. N. Ray, D. Chatterjee, and S. K. Goswami, "Harmonics elimination in a multilevel inverter using the particle swarm optimisation technique," *IET Power Electron.*, vol. 2, no. 6, pp. 646–652, 2009, doi: 10.1049/iet-pel.2008.0180.

[2.5] Y. Liu, H. Hong, and A. Q. Huang, "Real-time algorithm for minimizing THD in multilevel inverters with unequal or varying voltage steps under staircase modulation," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2249–2258, 2009, doi: 10.1109/TIE.2009.2015360.

[2.6] M. F. Kangarlu and E. Babaei, "Cross-switched multilevel inverter: An innovative topology," *IET Power Electron.*, vol. 6, no. 4, pp. 642–651, 2013, doi: 10.1049/iet-pel.2012.0265.

[2.7] T. Chaudhuri and A. Rufer, "Modeling and control of the cross-connected intermediate-level voltage source inverter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2597–2604, 2010, doi: 10.1109/TIE.2009.2033486.

[2.8] R. José *et al.*, "Multilevel converters: An enabling technology for high-poer applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, 2009, doi: 10.1109/JPROC.2009.2030235.

[2.9] N. Prabaharan and K. Palanisamy, "Comparative analysis of symmetric and asymmetric reduced switch MLI topologies using unipolar pulse width modulation strategies," *IET Power Electron.*, vol. 9, no. 15, pp. 2808–2823, 2016, doi: 10.1049/iet-pel.2016.0283.

[2.10] M. Hagiwara and H. Akagi, "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, 2009, doi: 10.1109/TPEL.2009.2014236.

Chapter-3

Proposed Single PV-Source based Asymmetrical Cross Switch MLI for grid Integration

This chapter presents an asymmetrical 13-level cross switch MLI for PV-Grid integration. The proposed scheme uses a single PV panel with multi winding flyback converter to energise the inverter. THD minimization of MLI output voltage using Black Widow Optimization algorithm is also discussed. Simulation and experimental analysis are carried out with online control technique using a three phase 13-level reduced CSMLI to validate the proposed concept on a practical system.

PROPOSED SINGLE PV-SOURCE BASED ASYMMETRICAL CROSS SWITCH MLI for GRID INTEGRATION

3.1 INTRODUCTION

One of the most difficult problems in the renewable energy industry is improving the power quality of DC electricity from renewable sources by transforming it into AC power for AC grids or other loads. Research into alternatives to filter circuits for improving power quality has led to the widespread adoption of Multilevel Inverter (MLI) technology for AC power conversion. As discussed in chapter 1, due to the modular design and enhanced output voltage of Cascade H-bridge MLI (CHBMLI), this topology and its modified design are connected to grid without transformer as mentioned in [3.1], [3.2]. But the limitations of CHBMLI motivates researcher to design the MLI with optimum number of switching devices. In order to obtain magnified output voltage waveform with lesser number of switching devices a reduced MLI with symmetrical and asymmetrical input sources is presented in [3.3]. A single phase 53 level MLI is also proposed in [3.4] that uses bidirectional switch to achieve required output voltage with minimum switching loss. A reduced switch asymmetrical voltage source based MLI with low standing voltage has been proposed for PV application [3.5]. A cross switched multilevel inverter with reduced number of power switches is proposed in [3.6] which has already discussed in chapter 2. In this literature the MLI is operated with five equal DC sources to generate 11-level output voltage. To achieve high output voltage level with less number of switching devices and the MLI topologies with unequal DC sources are designed and implemented for grid integration [3.1] and high power application [3.7].When synchronization of PV with grid is considered the primary objective, which needs to achieve is power quality improvement that deals with less harmonic content in grid side and less THD. Some control scheme has been implemented like PWM and modified SPWM for selective harmonic elimination (SHE) to get the appropriate triggering angles, which has achieved the minimum THD as per IEEE standard stated in [3.8],[3.9]. As PWM switching frequency is very high, these techniques lead to increase the switching losses. The above complications are avoided by adopting several population based optimization algorithms which have reduced the output voltage THD using

MLI up to desired level as discussed in [3.10]-[3.12]. Apart from this a modified Grey Wolf Optimization (GWO) algorithm for SHE-PWM has been proposed in [3.13], which has reduced the line voltage THD up to 5.53%, but the higher order harmonics voltages are not reduced properly as viewed in the FFT analysis.

In this chapter a 13-level cross switched MLI(CSMLI) with unequal DC voltage sources generated from single PV module for medium voltage range application is presented. The contribution is pointed below.

1- The performance of the aforementioned MLI in this research, which has a decreased number of switches and DC voltage sources for the purpose of minimising THD, has been thoroughly evaluated, and the results are provided in section 3.4.
2- Rather than using multiple solar panels in each phase for distinct voltage levels, a single solar panel with multiple outputs through a flyback converter has been used in this scheme to provide unequal DC sources to the CSMLI, as discussed in section 3.2.
3- Black Widow Optimisation (BWO) has been adopted to obtain the desired switching angles that would trigger the CSMLI with minimum voltage THD, and to justify its effectiveness of this algorithm, the objective function of the system is calculated in MATLAB's programme environment using GWO and PSO algorithms of the same population size. Section 3.4.1 contains the results of the comparison analysis performed on the aforementioned algorithms.
4- These algorithms have successfully minimized the THD from the line voltage of the system output.
5- The nonlinear change of the triggering angles with the modulation indices is calculated offline and stored in the form of piecewise mixed model equation [3.14] derived from BWO algorithm to achieve minimum voltage THD. In section 3.2.5, all the specifics are laid out for.

3.2 PROPOSED SCHEME

The first objective of this proposed scheme is to implement a newly available metaheuristic search based algorithm for THD minimization of a reduced switch Multilevel Inverter to interface PV energy with medium or high voltage grid. The second objective is usage of a

single PV panel to obtain multiple asymmetrical DC sources for inputs to the MLI, hence making this scheme cheaper and less complicated. Moreover, application of the new optimization algorithm helps to reach lower THD and thereby reducing the interfacing reactor values compared to existing schemes.

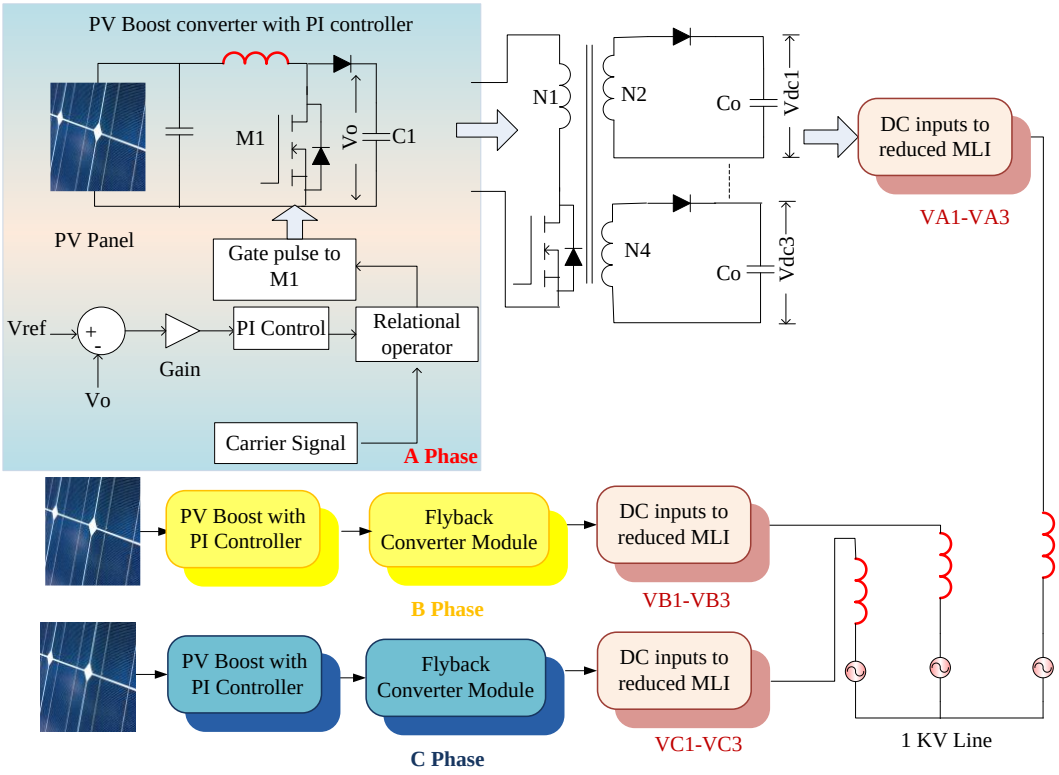


Figure 3.1. PV based CSMLI through proper isolation for grid application

3.2.1 PV Boost Converter Control

In this model, as shown in Figure 3.1, three 260-watt PV panels are utilised for a three-phase system. In each phase, a DC-DC boost converter with a PI controller has been implemented to increase the PV voltage. The PI controller is used to maintain a constant output voltage by adjusting the duty ratio (D) in response to a change in the input voltage. The controller generates a reference signal that is compared to a 20 kHz carrier signal to

generate a trigger pulse for the boost converter, as depicted in the figure above. The relationship between boost output voltage (V_o) and PV input voltage (V_i) is shown below.

$$V_o = \frac{V_i}{1-D} \tag{3.1}$$

3.2.2 Isolation through Flyback Converter

In this chapter, a 13-level reduced MLI is examined for operation with three uneven DC inputs per phase. Furthermore, separation of these sources is necessary to prevent a short circuit from occurring during switching. The proposed method takes into account the use of a PV-boost converter and an isolated multi-output flyback converter to accomplish this. Thus, the proposed scheme reduces the number of input sources compared to existing schemes that typically require 'n' solar panels for 'n' inputs per phase for the MLI [3.1], 3.2]. As a result, the total price of the system might be decreased significantly. The boost converter's output voltage for each of the three phases has been used to power the flyback converter. The 13-level output voltage is generated by feeding the converter's output, V_{dc1} through V_{dc3}, into each phase of the simplified MLI. The output of the flyback converter (V_{out} i.e V_{dc1} of secondary winding N_2) can be expressed as:

$$V_{out} = K1 * \left(\frac{D}{1-D}\right) V_{c1} \tag{3.2}$$

V_{c1}=Input voltage to flyback converter shown in figure 3.1. D=Duty cycle or duty ratio. Here duty ratio ‘D’ and transformation ratio ‘K1’ are set to 0.6 and 2 respectively. Transformation ratios K1, K2 and K3 for the secondary windings bear a ratio of 1:3:2 to generate unequal DC voltages for the MLI inputs.

3.2.3 Reduced 13-level CSMLI

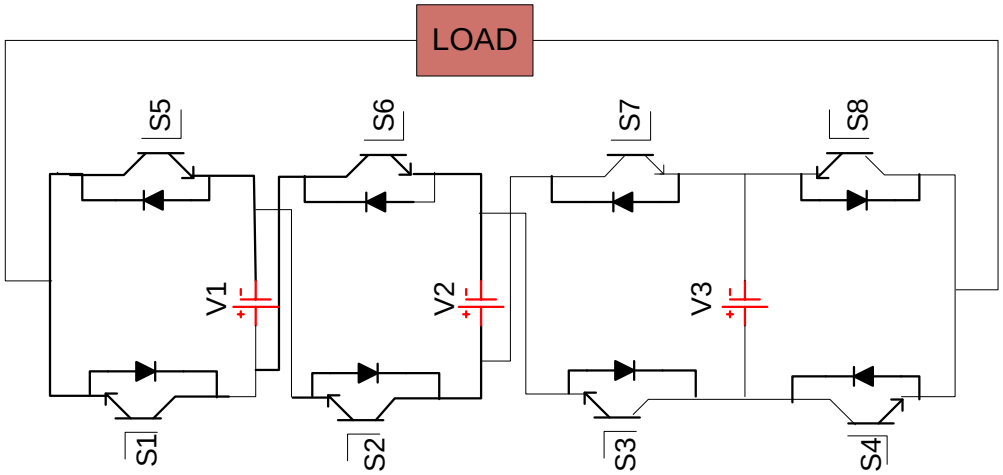


Figure 3.2. Circuit diagram of a single phase 13-level CSMLI

In the previous chapter properties of an 11-level CSMLI has discussed, which operates with equal DC voltage sources and therefore, requires higher number of power switches in order to generate higher output voltage level. Considering this limitation, CSMLI topology with unequal DC voltage sources is introduced in this research. The voltage sources with ratio of 1:3:2 is used to develop 13-level output voltage. Presented reduced MLI required lessen power semiconductor devices in comparison to symmetrical CSMLI and conventional CHBMLI. For developing 13-level output voltage CHBMLI needs 24 numbers of switching devices and symmetrical CSMLI needs 14 switching devices where CSMLI with unequal sources needs 8 switches and three DC sources only. The single phase circuit diagram of 13-level CSMLI is shown in figure 3.2. The relation between number of switches and number of DC voltage sources for both the topologies are:

In case of CHBMLI: $N_{sw} = 4 * N$ (3.3)

In case of CSMLI: $N_{sw} = 2 * (N + 1)$ (3.4)

Presented asymmetrical CSMLI exhibits a relation of output voltage level with number of DC sources is presented in equation (3.5).

$$V_l = 2N(N-2) + 7 \tag{3.5}$$

The optimum switching angles are determined by the help of BWO algorithm using MATLAB program. To obtain the desired staircase output voltage waveform, triggering patterns for the 13-level reduced MLI are designed using Table 3.1. Here asymmetrical DC sources are applied to develop the above-mentioned output voltage level. The input voltages to reduced MLI are performed a relationship which shown in equation (3.6).

$$V1 : V2 : V3 = 1 : 3 : 2 \tag{3.6}$$

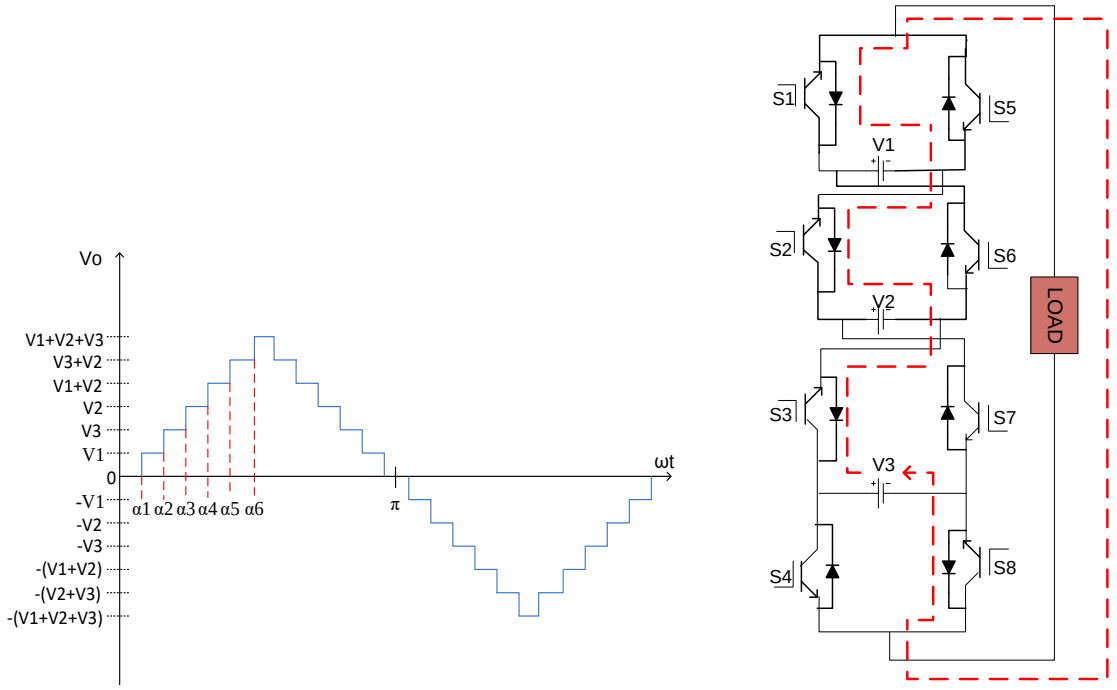
The MLI is operating with unequal DC voltages but results equal step voltage at each level that presented in figure 3.3 (a). The operation of the MLI can be explained as per the switching scheme explained in Table 3.1. As the complete operation of CSMLI has been elaborated in chapter 2, here only the operation of 13-level CSMLI for generating maximum output voltage is explained using a single phase structure of the MLI figure 3.3 (b). The output voltage can vary from V_{max} to $-V_{max}$, which will be accelerated by the triggering angles $\alpha_1, \alpha_2, \ldots \alpha_6$ and V_{max} is expressed in equation (3.7).

$$V_{max} = V1 + V2 + V3 \tag{3.7}$$

Table 3.1. Switching Table of Single Phase 13-Level Reduced Switch MLI

Switching combinations for each voltage level												
switches	V1	V3	V2	V1+V2	V2+V3	V1+V2+V3	-(V1)	-(V3)	-(V2)	-(V1+V2)	-(V2+V3)	-(V1+V2+V3)
S1	1	1	0	1	0	1	0	0	1	0	1	0
S2	1	0	1	1	1	1	0	1	0	0	0	0

S3	0	1	1	1	1	1	1	0	0	0	0	0
S4	0	0	1	1	0	0	1	1	0	0	1	1
S5	0	0	1	0	1	0	1	1	0	1	0	1
S6	0	1	0	0	0	0	1	0	1	1	1	1
S7	1	0	0	0	0	0	0	1	1	1	1	1
S8	1	1	0	0	1	1	0	0	1	1	0	0



(a) (b)

Figure 3.3. (a) Output voltage waveform of a 13- level reduced inverter, (b) Operational diagram of 13- level CSMLI

3.2.4 Mathematical Modelling

The nonlinear equation for MLI output voltage waveform shown in figure 3.3(a) can be represented as:

$$V(\omega t) = \sum_{\alpha=1}^{ai} \frac{4V_D}{n\pi} (\cos(n\alpha_1) + \cos(n\alpha_2) + \cdots + \cos(n\alpha_{ai}))\sin(\omega t) \quad (3.8)$$

V_D is the DC input voltage to the MLI for each level. The nonlinear equation representing the fundamental voltage and harmonic voltages is shown below.

$$\left.\begin{aligned}
&\cos(\alpha_1) + \cos(\alpha_2) + \cdots + \cos(\alpha_6) = KV_1 \\
&\cos(5\alpha_1) + \cos(5\alpha_2) + \cdots + \cos(5\alpha_6) = 0 \\
&\cos(7\alpha_1) + \cos(7\alpha_2) + \cdots + \cos(7\alpha_6) = 0 \\
&\cos(11\alpha_1) + \cos(11\alpha_2) + \cdots + \cos(11\alpha_6) = 0
\end{aligned}\right] \quad (3.9)$$

Where, $K=\pi/4V_D$. The Modulation index (MI) can be represented as:

$$MI = \frac{V_1}{V_{max}} \quad (3.10)$$

Where $V_{max} = (V_l - 1)*V_D/2$. In this chapter THD of output voltage has been minimized through BWO, PSO and GWO algorithms and the optimum switching angles are obtained for the MLI operation. THD of output voltage is minimized considering up to 39^{th} order harmonics, which has been explained through FFT analysis.

3.2.5 Online Control Scheme

During the course of this study, the above control strategy is created for reduced MLI in order to provide minimal harmonic injection when connected to the main grid. The same thing has been validated through the use of the simulation model. Measurements of the grid voltages are taken using voltage sensors, and measurements of the corresponding angles are taken with PLL, so that the control action can be initiated. The inner loop is utilised to achieve control of the current, and the frequency is evaluated in relation to the fundamental. Following the processing of the current error by the PI controller, the modulation index can be derived, as demonstrated in figure 3.4. Here the constants P and I are set to 5 and 10 respectively after tuning so that the output of PI will be within the range of 0.5-0.96. As can be seen in figure 3.5, the ideal switching angles for minimum THD are determined offline by applying the BWO method in conjunction with a variety of modulation indices (MI). The mixed model equation that is proposed in [3.14] can be used to obtain the linear and nonlinear

equations that apply to each portion of the curve. Equations (3.11) and (3.12) contain the identical expressions.

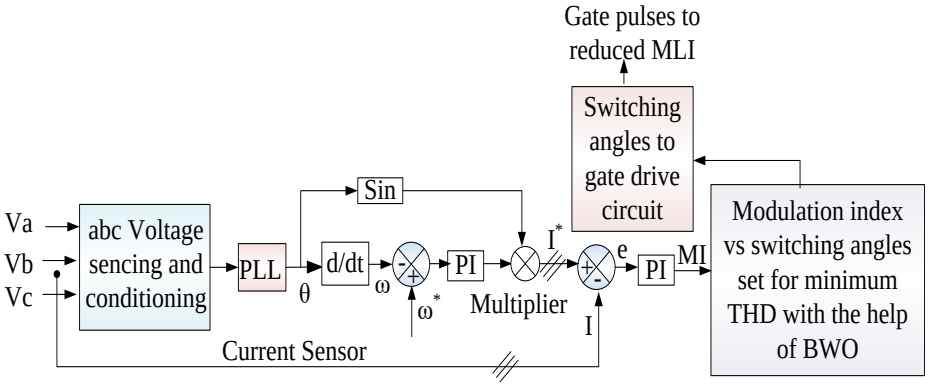


Figure 3.4. Developed Control Scheme

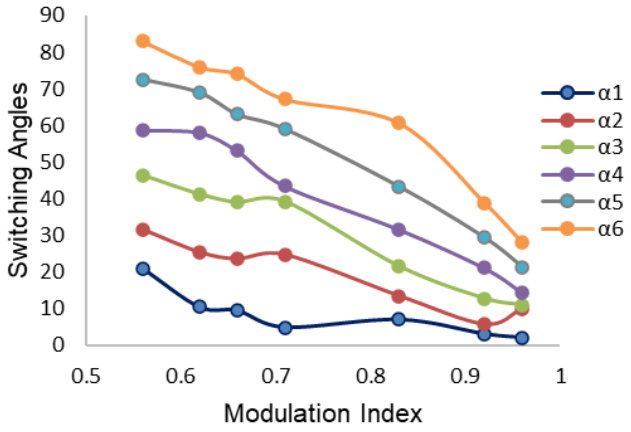


Figure 3.5. Switching angles vs modulation index graph for 13-level CSMLI

For 0.55≤ MI ≤0.71 the switching angles are:

$$\begin{aligned}
\alpha 1 &= -103.4MI + 77.311 \\
\alpha 2 &= -47.644MI + 56.633 \\
\alpha 3 &= -49.282MI + 72.88 \\
\alpha 4 &= -101.16MI + 117.76 \\
\alpha 5 &= -94.147MI + 125.93 \\
\alpha 6 &= -101.97MI + 139.93
\end{aligned} \tag{3.11}$$

and for 0.72≤MI≤0.96 the switching angles are:

$$\begin{aligned}
\alpha 1 &= -343.83MI^2 + 577.56MI - 236.22 \\
\alpha 2 &= 284.02MI^2 - 534.73MI + 259.95 \\
\alpha 3 &= 269.1MI^2 - 611.46MI + 324.84 \\
\alpha 4 &= -87.243MI^2 + 22.843MI + 73.156 \\
\alpha 5 &= -214.51MI^2 + 214.64MI + 13.112 \\
\alpha 6 &= -621.02MI^2 + 859.8MI - 225.69
\end{aligned} \tag{3.12}$$

The modulation indices are varied between 0.55 to 0.96 as this is usually the working range for the converter. For the modulation index below 0.55, the overall THD can become out of the permissible range. These equations are set aside in the processor memory. The gate pulses for MLI are originated as per the stored data in processor memory to attain minimum voltage THD.

3.3 BLACK WIDOW OPTIMIZATION

In the year 2020, V. Hayyolalam and A.P. Kazem suggested a novel metaheuristic algorithm called Black Widow Optimisation (BWO) to address these real-world problems. This method is based on observations of Black widow spider mating and offspring development. According to [3.15], this algorithm has established a new standard for improving the precision with which real-world engineering problems can be solved. When compared to other population-based algorithms, the BWO algorithm has proven to be the most effective at locating global optimum solutions. The widow population has been assigned at random to kick off this method. According to their birth rates, the assigned population is split in two groups of parents. The mating process between the set of parents initiates the reproductive process, and the biological nature of the Black widow spider dictates that the male spider be swallowed by the female spider at some point during or immediately following the mating process. When spiders breed, only the healthiest offspring make it through to adulthood, and

the rest are eaten by the dominant social group. The following equations are formulated to produce offspring.

$$off_1 = a * par_1 + (1 - a) * par_2 \tag{3.13}$$

$$off_2 = a * par_2 + (1 - a) * par_1 \tag{3.14}$$

Where par_1 and par_2 are treated as two group of parents and 'a' is the randomly generated array with same length of parents. In this algorithm the fitness function value decides the stronger population group. After getting the stronger group, mutation is carried out randomly to generate a new solution. The entire process is formulated and an algorithm has been developed to solve the optimization problem.

3.3.1 Proposed Application of BWO Algorithm for CSMLI

For the design of three phase 13-level CSMLI, suitable triggering angles have been evaluated using BWO algorithm that provides minimum THD across output voltage. Here the set of angles are acknowledged as the population size of the spider. The position vector of the spider has been provided as $\alpha_i = [\alpha_{i1}, \alpha_{i1}, \ldots\ldots \alpha_{im}]$. The best population group which provides the optimum result has been obtained using the following steps.

1- Initialize the maximum iteration count, procreating rate, cannibalism rate and mutation rate.

2- The population or triggering angle matrix denoted by 'Trig' of size [k X i] is generated randomly between 0 to π/2 and vector 'a' is initialized randomly of size 'i'.

3- In this step the fitness function is calculated for each set of population (triggering angles) using the following equation.

$$f = min \frac{\sqrt{\sum_{n=3,5\ldots}^{49} V_n^2}}{V_1} \tag{3.15}$$

4- Based on the fitness function values select the stronger population and stored in another matrix say ‘Trig1’

5- The reproduction is started in this step. Two parents’ matrix are selected from matrix ‘Trig1’ and the offspring are generated using equations (3.13) and (3.14). From the new population, the stronger population are obtained based on the minimum fitness function value and rest are destroyed. The best population are now stored in matrix say ‘Trig2’.

6- Mutation is started in this step. From the population matrix ‘Trig1’ position of two randomly selected population vector are exchanged and the new population is stored in ‘Trig3’.

7- Now the population is updated by using the following equation.

$$Trig = Trig2 + Trig3 \tag{3.16}$$

8- The best solution is obtained from the updated population matrix ‘Trig’ and displayed.

9- Termination condition: If maximum iteration is occurred then the entire process is stopped or return to step 3.

3.4 SIMULATION RESULTS and COMPARATIVE STUDY

The simulation has been carried out using grid connected reduced switch 13-level MLI providing low output voltage THD. To get the desired triggering angles MATLAB based program has been used for BWO, GWO and PSO algorithm. The performance and result of these optimization algorithms are compared to verify the usefulness of the proposed BWO technique. Each phase of this inverter has been energized from PV cell with proper isolation. The PV voltage has been boosted up from 32.63 volts to 62.87 volts through boost converter.

To provide multiple unequal DC sources across MLI, flyback converter develops voltages of ratings 122, 245 and 368 volts for MLI operation. The optimum switching angles are calculated for the modulation index (MI) range of 0.55 - 0.96 using all the above algorithms. For a typical

modulation index of 0.92 the calculated angles and corresponding THD values are shown in Table 3.2.

Table 3.2 Triggering Angles Obtained from BWO, GWO and PSO

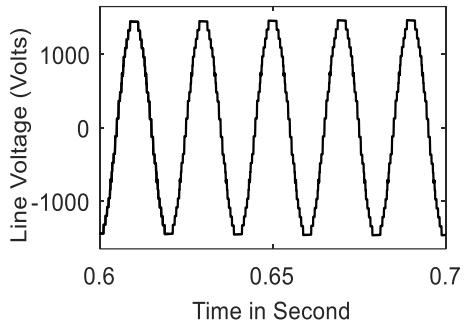
Algorithm	Output Voltage THD	Optimum triggering angles (Degrees)					
		α_1	α_2	α_3	α_4	α_5	$\alpha 6$
BWO	2.27%	3.012	5.62	12.66	21.04	29.3	38.8
GWO	2.63%	2	7.76	12.81	18.61	31.6	35.6
PSO	3.83%	2.45	6.5	12.42	23.51	34.3	39

The boost converter output voltage and the flyback converter output voltages are shown in Figure 3.6 (a) and (b) respectively.

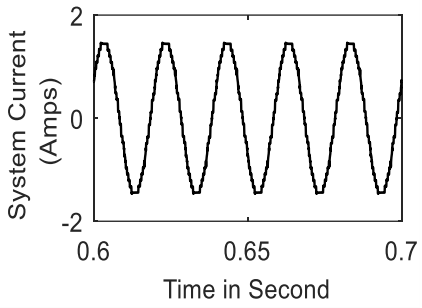
(a) (b)

Figure 3.6. (a) PV output voltage waveform with respect to time, (b) output DC voltage waveforms of flyback converter

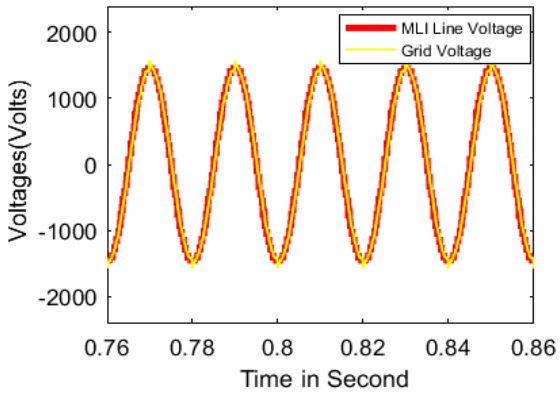
The system is connected to a medium voltage grid of 1KV and 50Hz for verification. The grid connected MLI output voltage, converter current waveforms and synchronized voltage waveforms of MLI and grid output are recorded and displayed in figure 3. 7.



(a)



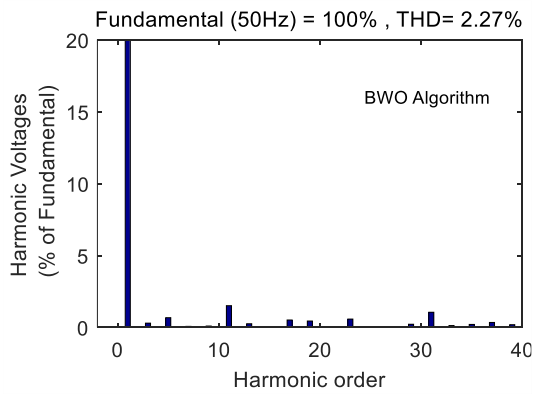
(b)



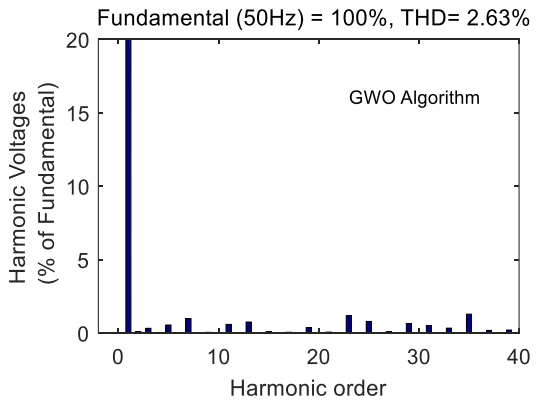
(c)

Figure 3.7. (a) Grid connected Line voltage waveform with respect to time, (b) Converter current waveform with respect to time, (c) Synchronized voltages of MLI and grid

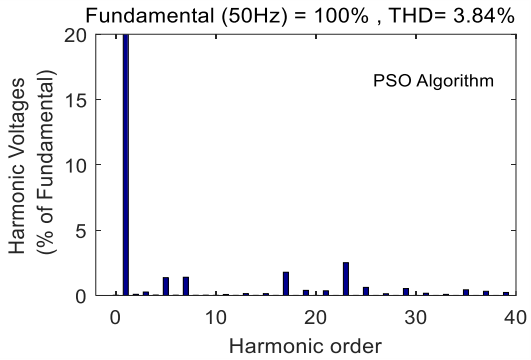
To verify the superiority of BWO algorithm for solving minimum voltage THD, the FFT analysis has been carried out by simulating the proposed scheme using BWO, GWO and, PSO techniques. The FFT graph of output voltage and overall THD has been shown in figure 3.8.



(a)



(b)

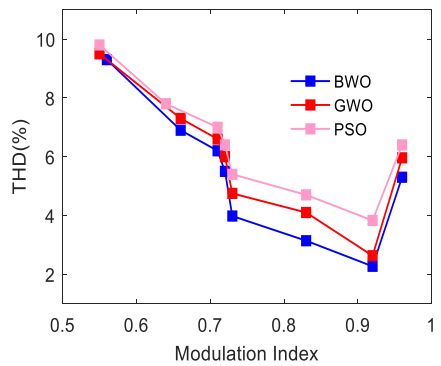


(c)

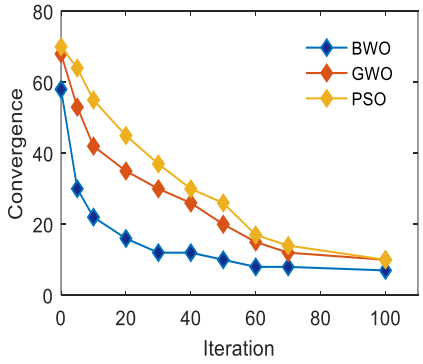
Figure 3.8. Harmonic spectra for output line voltage waveform for modulation index 0.92 using (a) BWO, (b) GWO and (c) PSO algorithm

3.4.1 Comparison Study Between BWO with GWO and PSO Algorithm for The Proposed Application

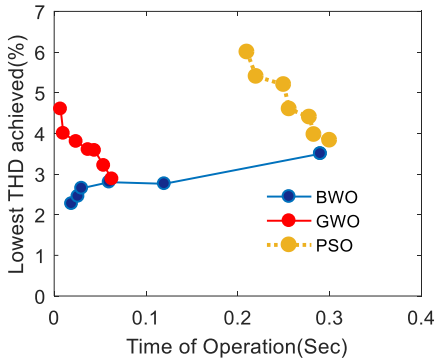
The simulated output voltage THD was measured for different values of modulation indices, which is shown in figure 3.9(a). It shows a gradual decrease with increasing modulation index for all the three methods. However, the THD obtained through BWO is lowest compared to the other two methods. The typical convergence characteristics for the objective function with modulation index 0.92 is shown in figure 3.9(b). Here also the proposed BWO technique shows better performance compared to the other two methods. In figure 3.9(c), the time taken to achieve the minimum voltage THD for all the three methods with same modulation index of 0.92 is shown, which also reflects the superiority of BWO technique over the others.



(a)



(b)



(c)

Figure 3.9. (a) Comparative study of output voltage THD with respect to Modulation Index for BWO, GWO and PSO Algorithm**,** (b) Convergence vs Iteration graph of BWO in comparison with GWO and PSO algorithm, (c) Lowest THD vs Time of operation for BWO, GWO and PSO Algorithm

Different parameters along with lower order harmonic content computed through all the above three methods for typical two modulation indices of 0.6 and 0.92 are shown In Table 3.3. From this table, it is also evident that the proposed BWO technique is more effective compared to GWO and PSO methods for the proposed application. The presented scheme with BWO algorithm has been compared with other available switching schemes used for MLI operation and the results have been presented in Table 3.4.

Table 3.3. Comparison Table for BWO, GWO and PSO Algorithm

Sl NO	BWO Algorithm	PSO Algorithm	GWO Algorithm	Sl NO	BWO Algorithm	PSO Algorithm	GWO Algorithm
At Modulation Index 0.92				At Modulation Index 0.6			
Convergence Time	0.02Sec	0.28Sec	0.063sec	Convergence Time	0.02Sec	0.28Sec	0.063sec
Line voltage THD	2.27%	3.84%	2.63%	Line voltage THD	5.80%	7.10%	6.90%
5^{th} order	0.68%	1.37%	0.54%	5^{th} order	1.00%	3.80%	2.14%
7^{rth} order	0.08%	1.40%	0.98%	7^{rth} order	1.50%	2.00%	1.37%
11^{th} order	0.72%	0.08%	0.59%	11^{th} order	1.17%	0.30%	0.07%
Grid current THD	2.6%	4.40%	3.2%	Grid current THD	6.40%	7.80%	7.50%

Table 3.4. Comparison Study of Proposed BWO Triggering Scheme with Existing Literature

References	MLI voltage level	Triggering scheme	O/P voltage THD
[3.1]	33	NLC	3.81%
[3.3]	9	Unipolar PWM	3.58%
[3.11]	11	Modified PSO	7.45%
[3.13]	11	Modified GWO	5.51%
[3.16]	5	Phase shifted PWM	4.30%
Presented scheme	13	BWO	2.27%

From Table 3.4, the efficiency of BWO algorithm to solve harmonic minimization problem through MLI has been proved. This newly available bio inspired optimization technique provides the optimum result in minimum time.

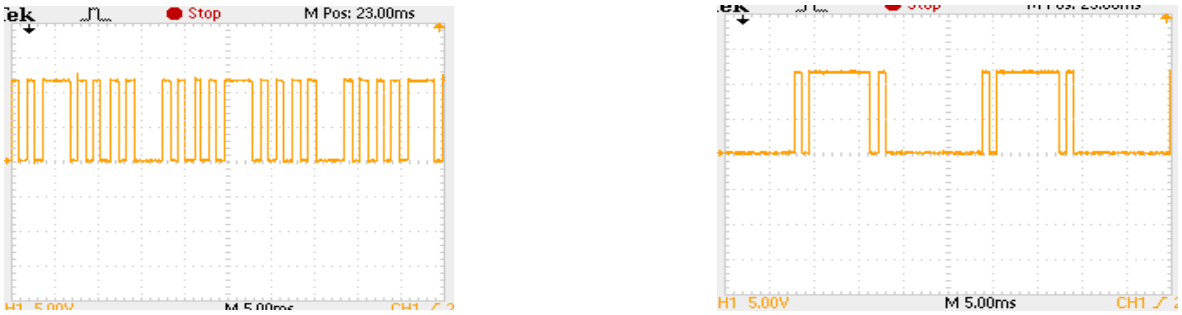
3.5 EXPERIMENTAL RESULTS

To verify the proposed scheme experimentally, a 260-watt solar panel has been used as a DC voltage source for a 13-level CSMLI as per configuration shown in figure 3.1. The inverter has been designed with eight semiconductor switches. The performance of the reduced MLI has been experimented with RL load. For recording the gate pulses load voltage and current waveforms, and voltage harmonic spectrum a DSO model no-TDS 2022B has been used. The component list has been provided in Table 3.5. The typical pulses of s1 and s2 are recorded and shown in figure 3.10.

Table 3.5. Component List

SI NO	**Components**	
1	PV panels	260W
Boost Converter		
2	Series inductor	1.371mH
3	Input capacitance	10μF
4	output capacitance	83.583μF
5	Switching Frequency	25KHz
Isolated Converter		
6	Core	Ferrite E-48, 24AWG
7	Power MOSFET, Power diode	IRF740, BYV26E
8	Switching Frequency	10KHz
Driver Circuit for MLI Switches		
9	Optocoupler	TLP250H
10	Microcontroller	PIC18f452
CSMLI		
11	Power switches (IGBT)	FGA25N120
12	Load	R=100Ω, L=20mH

13	Switching Frequency	50Hz



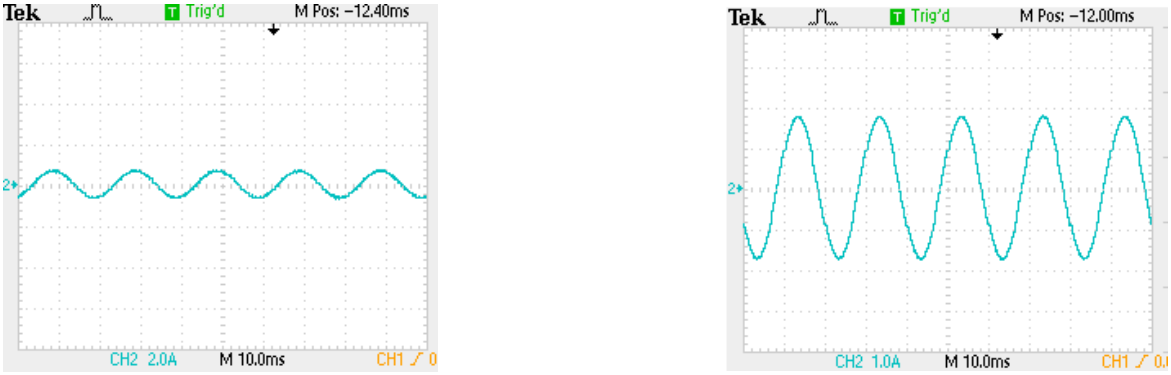
(a) (b)

Figure 3.10. (a)Pulse voltage of switch s1, (b) pulse voltage of switch s2. (scale: -channel1: y axis=5V/div)

Output line voltage and phase voltage are recorded and shown in figure 3.11 (a) and figure 3.11 (b) respectively. Dynamic characteristics of the MLI is recorded and the current waveforms at a constant load and at 50% increase of load are shown in figure 3.12 (a) and figure 3. 12 (b) respectively. The frequency spectrum of the output voltage wavefomrm at two different Modulation indices of 0.92 and 0.6 are shown in figure 3.13 (a) and (b) respectively. From the FFT analysis graph, of figure 3.13, it can be observed that almost all the lower order harmonics up to 39th has been removed from the line voltage waveform for MI of 0.92 with the help of the proposed algorithm however for the MI of 0.6 some of the higher order harmonics are having larger magnitude which increases the THD.

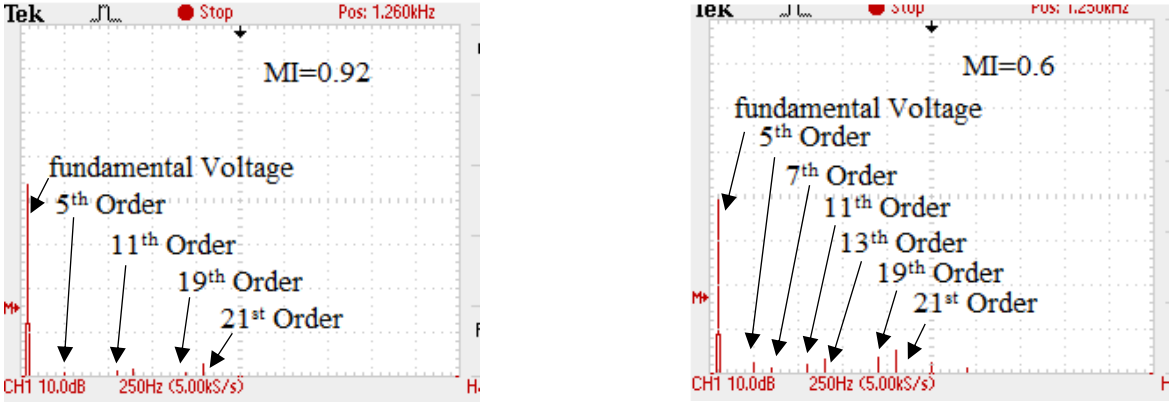
(a) (b)

Figure 3.11. Output voltage waveform (a) Line voltage (scale: - channel1: y axis=50V/div), (b) Phase voltage (scale: - channel1: y axis=20V/div)



(a) (b)

Figure 3.12. Current waveform at power factor 0.98 (a) At normal loading (scale: -channel1: y axis=2A/div), (b) At 50% increase of load (scale: -channel1: y axis=1A/div)



(a) (b)

Figure 3.13. Output Voltage harmonic spectrum (a) at modulation index 0.92, (b**)** at modulation index 0.6

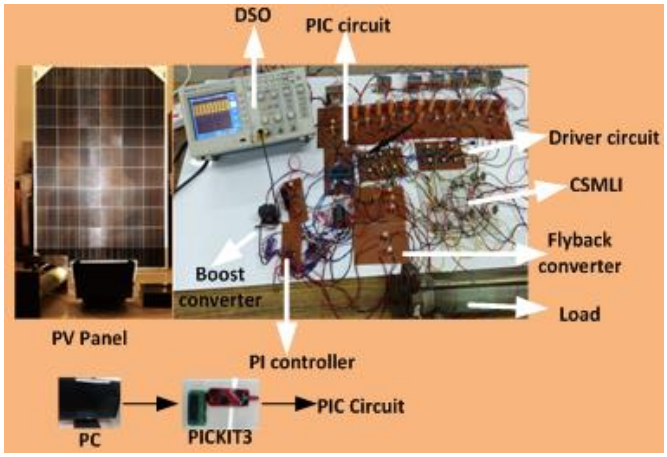


Figure 3.14. Developed prototype in the laboratory

The experimental verification of the proposed scheme in a small scale is carried out in the laboratory. The picture of the laboratory set up is shown in figure 3.14.

3.6 OBSERVATION

In this chapter a PV based scheme with cross switched multilevel inverter suitable for grid interconnection has been studied. The proposed scheme reduces the number of sources for developing desired output voltage level with low output voltage THD in comparison to other existing techniques. Three different metaheuristic algorithms have been tried for the proposed application, out of which BWO algorithm proved to be more accurate compared to the others. Thus, the BWO algorithm is used to obtain optimum switching angles for lowest output voltage THD at different modulation indices. The calculated angles are stored in micro controller memory in the form of mixed model equations for online application. To verify the capability of this MLI a 13-level CSMLI has been simulated for three phase system and experimental set up has been developed. It has been observed that both simulation and experimental results corroborate with theoretical model developed. The proposed technique is simple and can be easily implemented for a practical system.

3.7 PUBLICATION

[1] R. Mohanty et.al., "Lower Output Voltage Harmonics with Optimum Switching Angles of Single PV-Source Based Reduced Switch Isolated Multilevel Inverter using BWO Algorithm," IEEE Access (Under Review).

3.8 REFERENCES

[3.1] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4399–4406, 2009, doi: 10.1109/TIE.2009.2029579.

[3.2] F. Wu, X. Li, F. Feng, and H. B. Gooi, “Modified cascaded multilevel grid-connected inverter to enhance European efficiency and several extended topologies,” *IEEE Trans. Ind. Informatics*, vol. 11, no. 6, pp. 1358–1365, 2015, doi: 10.1109/TII.2015.2486623.

[3.3] N. Prabaharan and K. Palanisamy, “Comparative analysis of symmetric and asymmetric reduced switch MLI topologies using unipolar pulse width modulation strategies,” *IET Power Electron.*, vol. 9, no. 15, pp. 2808–2823, 2016, doi: 10.1049/iet-pel.2016.0283.

[3.4] E. Babaei, “A cascade multilevel converter topology with reduced number of switches,” *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2657–2664, 2008, doi: 10.1109/TPEL.2008.2005192.

[3.5] P. R. Bana, K. P. Panda, and G. Panda, “Power Quality Performance Evaluation of Multilevel Inverter with Reduced Switching Devices and Minimum Standing Voltage,” *IEEE Trans. Ind. Informatics*, vol. 16, no. 8, pp. 5009–5022, 2020, doi: 10.1109/TII.2019.2953071.

[3.6] M. F. Kangarlu and E. Babaei, “Cross-switched multilevel inverter: An innovative topology,” *IET Power Electron.*, vol. 6, no. 4, pp. 642–651, 2013, doi: 10.1049/iet-pel.2012.0265.

[3.7] M. D. Siddique, M. Rawa, S. Mekhilef, and N. M. Shah, “A new cascaded asymmetrical multilevel inverter based on switched dc voltage sources,” *Int. J. Electr. Power Energy Syst.*, vol. 128, no. August 2020, p. 106730, 2021, doi: 10.1016/j.ijepes.2020.106730.

[3.8] N. A. Rahim, K. Chaniago, and J. Selvaraj, “Single-phase seven-level grid-connected inverter for photovoltaic system,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2435–2443, 2011, doi: 10.1109/TIE.2010.2064278.

[3.9] S. Luo, F. Wu, and K. Zhao, “Modified Single-Carrier Multilevel SPWM and Online Efficiency Enhancement for Single-Phase Asymmetrical NPC Grid-Connected Inverter,” *IEEE Trans. Ind. Informatics*, vol. 16, no. 5, pp. 3157–3167, 2020, doi: 10.1109/TII.2019.2906248.

[3.10] R. N. Ray, D. Chatterjee, and S. K. Goswami, “Harmonics elimination in a multilevel inverter using the particle swarm optimisation technique,” *IET Power Electron.*, vol. 2, no. 6, pp. 646–652, 2009, doi: 10.1049/iet-pel.2008.0180.

[3.11] A. Routray, R. K. Singh, and R. Mahanty, “Modified Particle Swarm Optimization Based Harmonic Minimization in Hybrid Cascaded Multilevel Inverter,” *2018 IEEE Energy Convers. Congr. Expo. ECCE 2018*, vol. 15, no. 8, pp. 5573–5578, 2018, doi: 10.1109/ECCE.2018.8558021.

[3.12] M. H. Etesami, N. Farokhnia, and S. Hamid Fathi, “Colonial competitive algorithm development toward harmonic minimization in multilevel inverters,” *IEEE Trans. Ind. Informatics*, vol. 11, no. 2, pp. 459–466, 2015, doi: 10.1109/TII.2015.2402615.

[3.13] A. Routray, R. K. Singh, and R. Mahanty, “Harmonic Reduction in Hybrid Cascaded Multilevel Inverter Using Modified Grey Wolf Optimization,” *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 1827–1838, 2020, doi: 10.1109/TIA.2019.2957252.

[3.14] D. Chatterjee, “A novel magnetizing-curve identification and computer storage technique for induction machines suitable for online application,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 12, pp. 5336–5343, 2011, doi: 10.1109/TIE.2011.2126539.

[3.15] V. Hayyolalam and A. A. Pourhaji Kazem, “Black Widow Optimization Algorithm: A novel meta-heuristic approach for solving engineering optimization problems,” *Eng. Appl. Artif. Intell.*, vol. 87, no. September 2019, p. 103249, 2020, doi: 10.1016/j.engappai.2019.103249.

[3.16] Y. Shi, R. Li, Y. Xue, and H. Li, “High-frequency-link-based grid-tied PV system with small DC-link capacitor and low-frequency ripple-free maximum power point tracking,” *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 328–339, 2016, doi: 10.1109/TPEL.2015.2411858.

Chapter-4

Proposed Hybrid Model Optimum Switched Multilevel Inverter for PV Standalone System

This chapter introduces a hybrid Multilevel Inverter with reduced switch count. The operation of this MLI and its efficiency is discussed in this chapter. The reduced MLI output voltage is set to minimal Total Harmonic Distortion by the help of Modified JAYA algorithm. The competence of the proposed algorithm is verified and discussed. The proposed MLI topology for PV standalone system is studied and discussed.

PROPOSED HYBRID MODEL OPTIMUM SWITCHED MULTILEVEL INVERTER for PV STANDALONE SYSTEM

4.1 INTRODUCTION

Surge of energy demand has extended the research area towards harnessing the maximum energy from inexhaustible resources that keeps the environment pollution free. The PV energy can be successfully utilized in the places of high solar irradiation and nonexistence of AC grid through high voltage DC substation as discussed in [4.1]. But there is a major concern of power conversion with improved power quality when PV energy sources are interfaced with AC loads or grids without the use of passive filter circuit and transformer. The conventional Cascade H-bridge MLI (CHBMLI) with different control algorithms and control schemes are implemented successfully to solve the selective harmonic elimination problem and optimizing the Total Harmonic Distortion (THD) at grid or load side [4.2] and [4.3]. But due to the limitations of CHBMLI, MLIs with reduced number power switches are developed for high voltage application. In [4.4], a new topology of reduced MLI has been developed and utilized for PV-grid synchronization. Another topology of reduced MLI with switched-diode configuration, generating 31 output voltage level is demonstrated in [4.5] and the switching pulses for the proposed MLI are developed by staircase modulation techniques. But this MLI topology uses additional H-bridge to develop positive and negative cycle voltage, which leads to use of higher number of switching devices. In order to reduce the number of power devices another topology of reduced MLI has been developed without the use of H-bridge for low/ high voltage grid integration [4.6]. In this literature number of DC sources is reduced by implementing voltage divider with two series capacitors. The MLIs with reduced number of power devices make the system concise and efficient by minimizing the switching losses. Instead of symmetrical voltage sources, asymmetrical voltage sources for MLIs are preferred to procure higher level of output voltage with reduced number of DC sources and components [4.7,4.8]) which would able to reduce the system cost.

In this chapter, a 15-level reduced MLI with asymmetrical DC voltage sources has been proposed. This reduced MLI is suitable for medium or high voltage PV standalone system with minimum output THD. The contributions of this chapter are as follows:

a. The proposed topology is developed by hybridizing cross switched MLI (CSMLI) [4.9] and Packed U-cells (PUC) MLI [4.10]. The presented design of reduced MLI uses lower number of switching devices and DC sources for developing higher output voltage level and avoids the use of extra diodes and capacitors as discussed in [4.5], [4.6].

b. The proposed topology uses unequal voltage sources resulting in equivalent voltage level with lower voltage THD in comparison to the existing techniques.

c. The ideal switching angles for the proposed MLI are determined with the help of modified JAYA algorithm that uses less controlling parameter, less equations to achieve lowest voltage THD in comparison to other bio inspired algorithm based switching techniques [4.11] and [4.12]. This presented algorithm requires a single variable and less time of operation to converge.

The efficiency of the proposed algorithm has been verified by optimizing the output voltage THD of proposed 15-level MLI with conventional JAYA and modified PSO algorithm. The performance analysis of the proposed MLI is carried out by simulating a three phase 15-level reduced Hybrid Multilevel Inverter (HybMLI) for PV standalone system. To substantiate the simulation result, a small-scale prototype has been experimented in laboratory and discussed in section 4.7.

4.2 OPERATION of HYBRID MULTILEVEL INVERTER

The topology of HybMLI is influenced from CSMLI and PUCMLI as discussed in the introduction section. The CSMLI topology has been developed by cross arrangement of power devices with a DC source for each level and in PUCMLI topology each unit exhibits an ‘U’ structure with two power devices and one DC voltage source. This presented topology has a crossed power switches structure and ‘U’ shaped power switches structure in

alternative step. This reduced MLI is specially designed for asymmetrical DC voltage sources with minimum number of semiconductor switches to provide higher level of output voltage that leads to lower distortion. The reduced MLI is studied for a three-phase system that can be successfully implemented for a PV standalone system with improved power quality. The single phase structure of the proposed MLI is shown in figure 4.1. HybMLI is energized with a combination of positive and negative polarity of unequal DC sources with varying ratio. Here a single phase 15-level reduced MLI has been represented with three DC sources and eight switching devices to explain the operation with suitable switching pattern. In order to acquire a 15-level output voltage the input voltage ratio has been set to (1:2:5). The switching pattern for each voltage level is shown in Table 4.1.

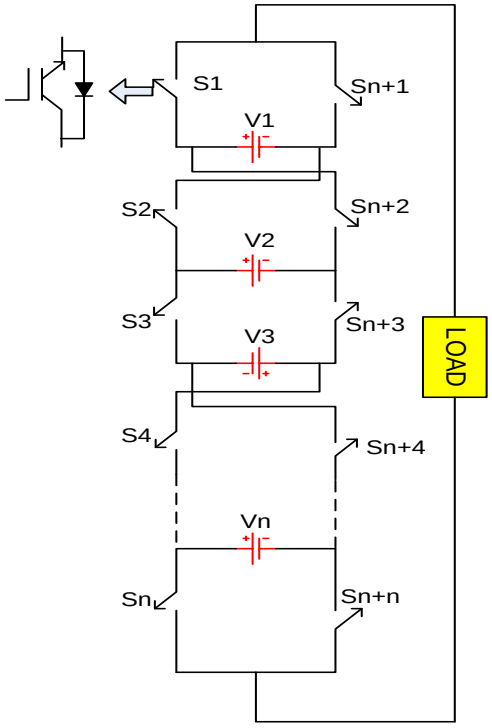


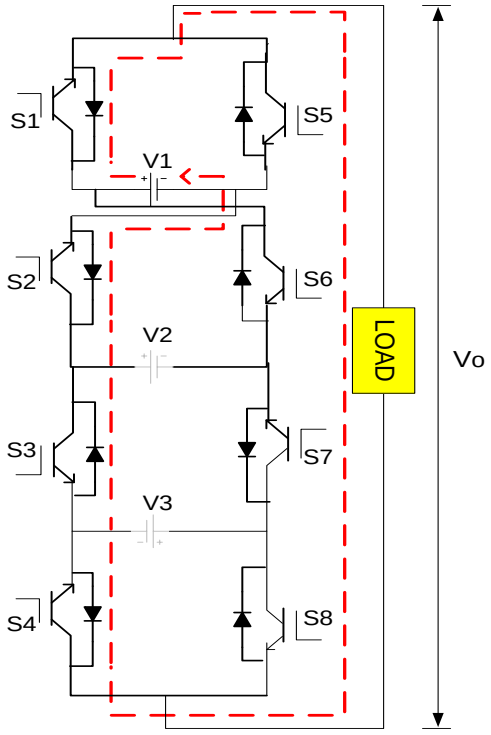
Figure 4.1. Circuit diagram of a single phase HybMLI

Table 4.1. Switching pattern of each device for HybMLI

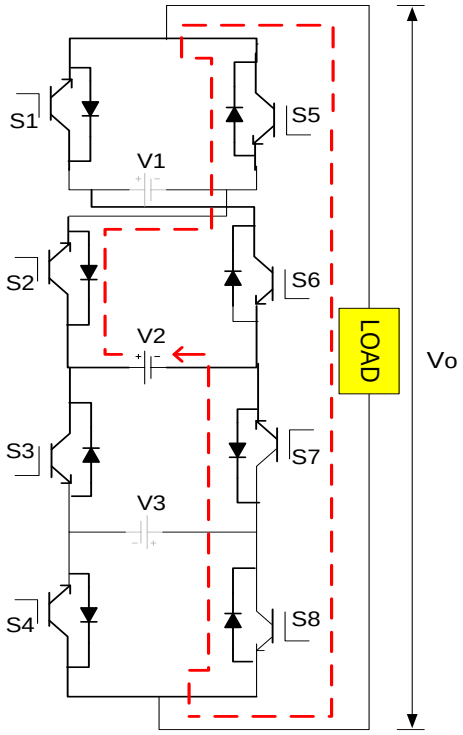
Operational Status of each switch for different voltage level														
SWITCH	V1	V2	V1+V2	V3-V1	V3	V3+V2	V1+V2+V3	-V1	-V2	-(V1+V2)	-(V3-V1)	-V3	-(V3+V2)	-(V1+V2+V3)
S1	1	0	1	0	1	0	1	0	1	0	1	0	1	0
S2	1	1	1	0	0	1	1	0	0	0	1	1	0	0
S3	1	0	0	0	0	0	0	0	1	1	1	1	1	1
S4	1	0	0	1	1	1	1	0	1	1	0	0	0	0

S5	0	1	0	1	0	1	0	1	0	1	0	1	0	1
S6	0	0	0	1	1	0	0	1	1	1	0	0	1	1
S7	0	1	1	1	1	1	1	1	0	0	0	0	0	0
S8	0	1	1	0	0	0	0	1	0	0	1	1	1	1

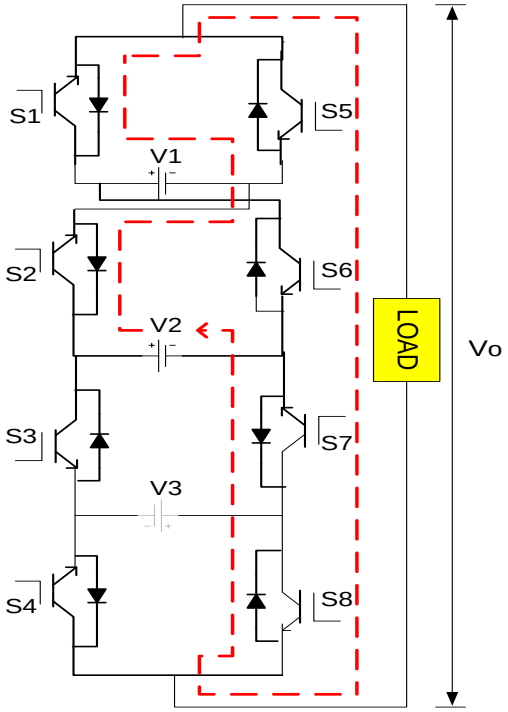
The three voltage sources V1, V2 and V3 are connected with the power devices in such a manner that by performing a decorous switching pattern with synthesizing these sources differently an expected output voltage can be achieved. For each voltage level there are four switches operating at a time. Operation of this proposed topology has been explained in seven different modes for positive half cycle with the suitable switching combination shown in Table 4.1.



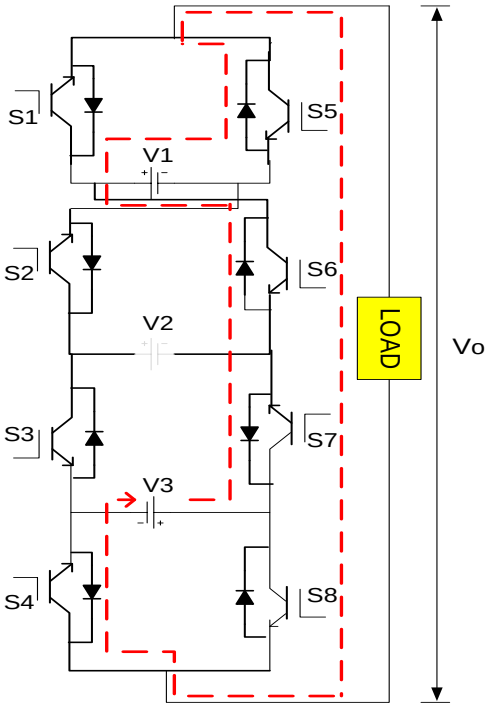
(a)



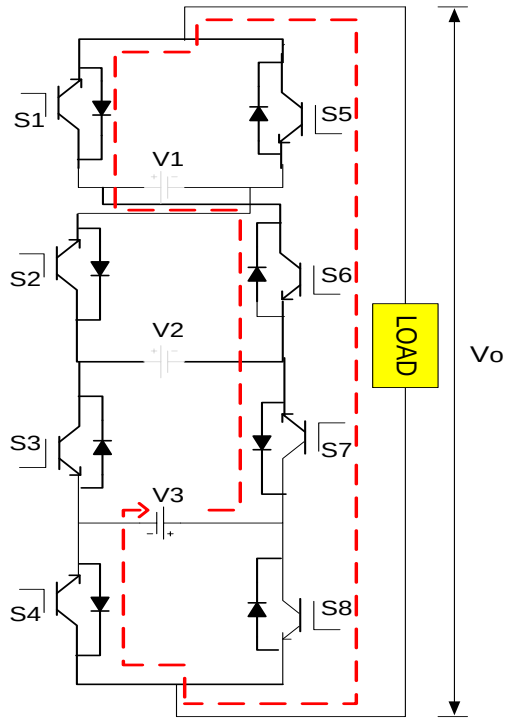
(b)


S1
S5
V1
S2
S6
V2
LOAD
Vo
S3
S7
V3
S4
S8

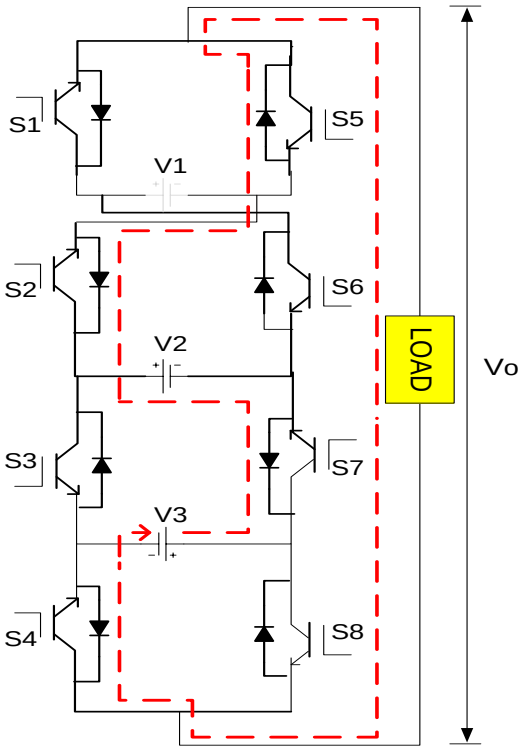
(c)


S1
S5
V1
S2
S6
V2
LOAD
Vo
S3
S7
V3
S4
S8

(d)


S1
S5
V1
S2
S6
V2
LOAD
Vo
S3
S7
V3
S4
S8

(e)


S1
S5
V1
S2
S6
V2
LOAD
Vo
S3
S7
V3
S4
S8

(f)

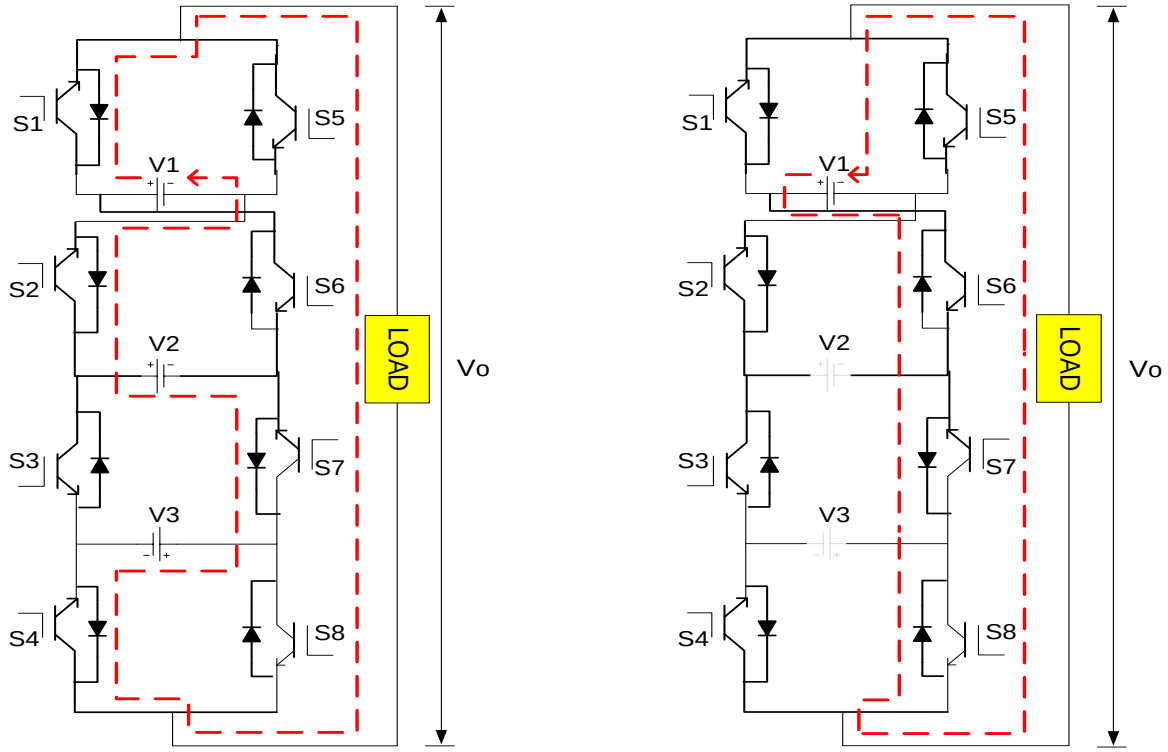


Figure 4.2. HybMLI Operation (a) mode 1, (b) mode 2, (c) mode 3, (d) mode 4, (e) mode 5 (f) mode 6, (g) mode 7, (h) mode 1 of negative half cycle

Figure 4.2(a) describes mode 1 operation of HybMLI to appear only V1 voltage across output, the 4 switches (S1, S2, S3 and S4) are getting turned on and the direction of current through load is shown by arrow. Figure 4.2(b) describes mode 2 operation to get V2 voltage, 4.2(c) explains mode 3 where output voltage is (V1+V2), 4.2(d) explains mode 4 of the reduced MLI to obtain (V3-V1) output voltage, 4.2(e) and 4.2(f) represent mode 5 and mode 6 respectively and result V3 and (V3+V2) voltage across output. Mode 7 is explained by figure 4.2(g) that gives maximum positive output voltage (V1+V2+V3). Similarly, the negative cycle of output voltage has been determined by operating the different switches as per Table 4.1. Mode 1 operation of negative half cycle is explained in figure 4.2(h). Number of switching devices for multilevel inverter design depend on output voltage level and input DC sources. In the proposed design of MLI, the number of switching devices and the output voltage level is derived as follows:

$$N_{sw} = 2 * (N + 1) \tag{4.1}$$

$$V_l = 2^{(N+1)} - 1 \tag{4.2}$$

Output voltage level of this reduced MLI can be varied by arranging the ratio of input voltage sources with different combination. This arrangement shrinks the need of DC voltage sources to result higher level of output voltage. The recommended design of reduced MLI makes the system compact and cost effective due to the use of reduced number of switching devices and provides lower voltage THD.

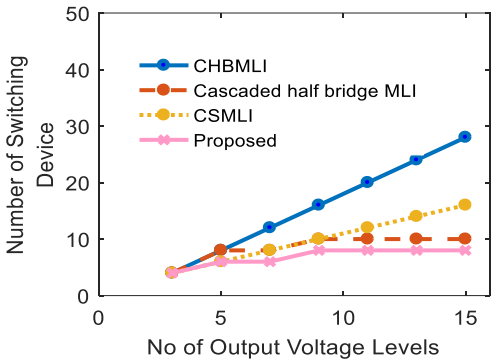


Figure 4.3. Required number of switching devices with respect to output voltage level for different topologies

Figure 4.3 shows the requirement of switching devices with respect to output voltage level by different topologies. Table 4.2 has classified the need of equipment with respect to output voltage level by other MLI topologies.

Table 4.2. Requirement of equipment with respect to output voltage level

MLI Topology	**For 15-level MLIs**			
	No of Sources	No of switches	No of diodes	No of capacitors
CHB MLI (Symmetrical)	7	28	0	0
Cascaded half bridge MLI(Asymmetrical)	3	10	0	0
[4.5] (Asymmetrical)	4	8	4	0
[4.6] (Asymmetrical)	3	10	0	2
[4.9] (Asymmetrical)	4	10	0	0
[4.10] (Asymmetrical)	1	8	0	2
Proposed (Symmetrical)	7	16	0	0
Proposed (Asymmetrical)	3	8	0	0

4.3 PROPOSED HYBRID MLI TOPOLOGY for PV STANDALONE SYSTEM

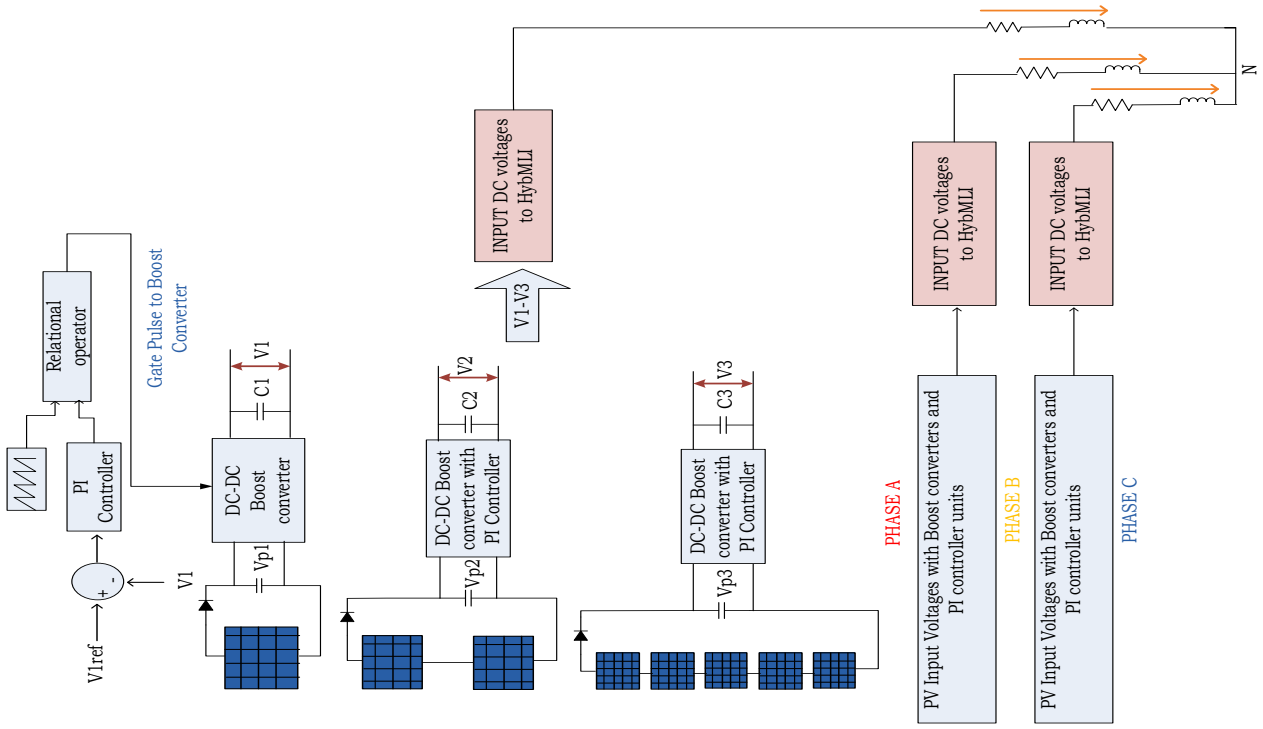


Figure 4.4. Circuit arrangement of power conversion through 15 level HybMLI for a PV standalone system

The schematic connection diagram of three-phase system for the proposed HybMLI is shown in figure 4.4. In section 4.2, it has been discussed that the input voltages should maintain a ratio of 1:2:5 to operate the proposed MLI for developing 15 level output voltage. As per the switching pattern shown in Table 4.1 and corresponding figure 4.2, it can be shown that the individual three PV sources per phase are not loaded equally. The approximate ratio of loading can be calculated as 1:3:10 for sources 1,2 and 3 respectively. Therefore, the power ratings of the PV sources are chosen as 50W, 150W and 500W for the proposed scheme. Voltage V1 is obtained from a 50W, 12V PV panel which is boosted up from Vp1 as shown in figure 4.4. For getting V2 voltage which is 2*V1, two PV panels of 75W of same voltage are connected in series and via boost converter the voltage is stepped up from Vp2 to V2. Likewise, voltage V3, which is 5 times greater than V1, is derived from a PV array of five PV panels each of 100W and same voltage in series. For the proposed scheme the per phase peak output voltage can be calculated as,

$$V_{max} = V1 + V2 + V3 \quad (4.3)$$

or

$$V_{max} = V1 + 2 * V1 + 5 * V1 \quad (4.4)$$

or

$$V_{max} = 8 * V1 \quad (4.5)$$

And the negative maximum voltage value is -8V1.

4.3.1 Mathematical Modelling

Output voltage of a Multilevel Inverter can be determined with the help of Fourier series analysis and MLI with asymmetrical voltage sources has the voltage expression of,

$$V(\omega t) = \sum_{\alpha=1}^{i} \frac{4V_D}{n\pi} ((k1 * \cos(n\alpha_1) + (k2 * \cos(n\alpha_2) + \cdots + (ki * \cos(n\alpha_i)))\sin(n\omega t) \quad (4.6)$$

Where V_D is the standard voltage at each step, k1, k2……. ki are the input voltage ratios to a standard set voltage and 'i' is treated as desired switching angles. The proposed reduced MLI has been designed with asymmetrical voltage sources but its output voltage level has not varied accordingly to satisfy equation (4.6). According to Table 4.1, the output voltage waveform is displayed in figure 4.5. From this voltage waveform it can be observed that, voltage magnitude at each step is same but at α_6 the voltage is two times greater than the others, which define the input voltage ratios $K_1 = K_2 = K_3 = K_4 = K_5 = K_7 = 1$ and $K_6 = 2$. Therefore, the expression of output voltage of the proposed MLI can be derived as follow.

$$V(\omega t) = \frac{4V_D}{n\pi} (cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3) + \cos(n\alpha_4) + \cos(n\alpha_5) + (2 * \cos(n\alpha_6)) + \cos(n\alpha_7))sin(n\omega t) \quad (4.7)$$

Here 'n' describes nth order harmonics present in the system and the nth order harmonic voltages are affected with the change of triggering angles α_1 to α_7 as displayed in equation (4.7). These angles lie between 0 to $\pi/2$ and bear a relation of:

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \pi/2 \quad (4.8)$$

Objective function or fitness function in this research that needs to optimise, which improves the power quality of the proposed system is stated as:

$$F = \frac{\sqrt{\sum_{n=3,5,\ldots}^{39} V_n^2}}{V_1} \tag{4.9}$$

In this research, the nonlinear equations that are solved using Modified JAYA algorithm to generate the optimum switching angles for getting lower output voltage THD are given below.

$$\left.\begin{aligned} &cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cdots + (2 * \cos(\alpha_6)) + \cos(\alpha_7) = C * V_1 \\ &cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \cdots + (2 * \cos(5\alpha_6)) + \cos(5\alpha_7) = 0 \\ &cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \cdots + (2 * \cos(7\alpha_6)) + \cos(7\alpha_7) = 0 \\ &cos(11\alpha_1) + \cos(11\alpha_2) + \cos(11\alpha_3) + \cdots + (2 * \cos(11\alpha_6)) + \cos(11\alpha_7) = 0 \end{aligned}\right\} \tag{4.10}$$

Here $C=\pi/4V_D$. Modulation index is defined by $MI=V_1/V_{max}$ as discussed in the previous chapter.

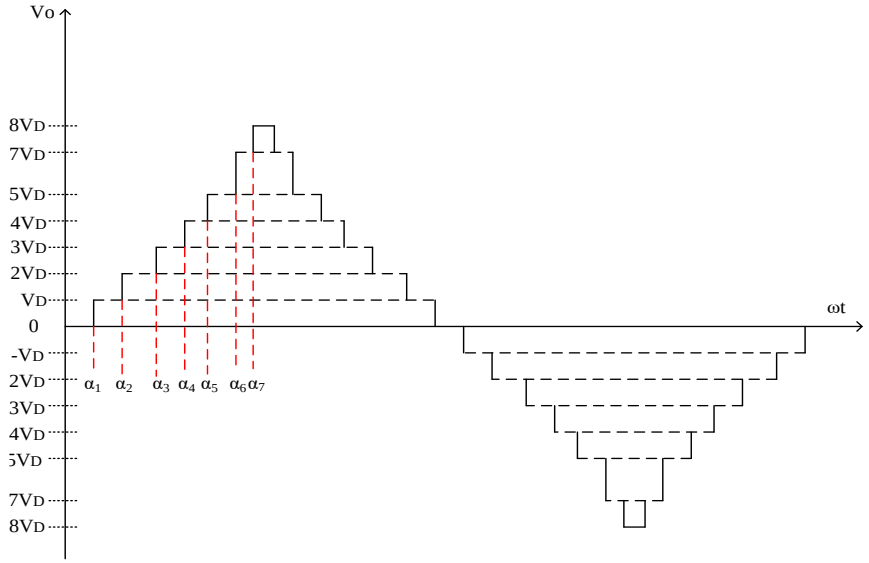


Figure 4.5. Output voltage waveform of 15 level HybMLI

4.4 PROPOSED MODIFIED JAYA ALGORITHM

Conventional JAYA algorithm was developed by V. Rao [4.13] in 2016 influenced by swarm behaviour of different organism. The Sanskrit meaning of victory has motivated the author to name the algorithm as "JAYA". The superiority of this algorithm is, it can solve the complex problems with smaller number of equations and less controlling parameter. It can be said that this algorithm has a potential to achieve the global optima with minimum computational attempt as discussed in [4.14]. The conviction of this algorithm that making it efficient among other metaheuristic algorithm is, it converges faster by avoiding the worst solution and getting closer towards the best solution in each iteration. A transformation of population has been carried out by the following equation after getting the best and worst population from the fitness function.

$$P_i(itr+1) = P_i(itr) + r_1\left(P_{ibest} - P_i(itr)\right) - r_2\left(P_{iworst} - P_i(itr)\right) \quad (4.11)$$

Where 'itr' stands for current iteration, P_{ibest} and P_{iworst} are the best and worst population obtained from their past experience respectively. r_1 and r_2 are the random numbers varied between 0 to 1.

In this proposed scheme to achieve the best solution by optimizing the fitness function, the algorithm is modified with an additional tuning variable. For enhancing the computational effort, an accelerating factor has been introduced to rationalize the population as represented in equation (4.12).

$$P_i(itr+1) = A * P_i(itr) + r_1\left(P_{ibest} - P_i(itr)\right) - r_2\left(P_{iworst} - P_i(itr)\right) \quad (4.12)$$

'A' is the acceleration factor given by:

$$A = (A_{max} - A_{min}) + \left(\left(\frac{itr_m - itr}{itr_m}\right) + A_{min}\right) \quad (4.13)$$

Where:

$$(A_{max} + A_{min}) \leq 1 \quad (4.14)$$

itr_m and itr are the maximum iteration count and current iteration value in the algorithm.

This modified JAYA algorithm has been designed with initializing ith population (switching angles) in random search space to minimize the THD of inverter output voltage. The equations (4.9) and (4.10) are solved using the proposed algorithm to achieve minimum voltage THD with optimized switching angles. Application of the modified algorithm to determine the appropriate switching angles is demystified by the following steps.

4.4.1 Application of modified JAYA algorithm in Hybrid MLI

Let's 'j' sets of 'i' numbers of population are initiated to optimize the fitness function which is the Total Harmonic Distortion (THD) of the output voltage. The switching angles set for inverter is considered as the population that is needed to calculate the fitness function and updated in each iteration from their experience.

Steps:

1- Maximum iteration count, maximum and minimum value of acceleration factor are initiated.

2- The population (switching angles) are randomly set up between 0 to π/2.

3- Fitness function or THD is calculated using equation (4.15).

$$F = \%THD = \frac{\sqrt{\sum_{n=3,5,\ldots}^{49} V_n^2}}{V_1} * 100 \qquad (4.15)$$

4- The best and worst value of the fitness function is recorded with their corresponding population.

5- The set of population are updated using equation (4.12) and the solution is getting modified by the following condition:

If $P_i(itr+1)$ has generated a better solution than $P_i(itr)$ then it is replaced with the former one or it is kept as it is.

6- If maximum iteration count has been reached, the steps are aborted or it will continue from step 3.

7- At the end optimum result is revealed.

4.5 SIMULATION RESULTS and COMPARATIVE EVALUATION

A three phase HybMLI is simulated in MATLAB/Simulink environment for a PV standalone system with optimized output voltage THD. The input voltage sources per phase for the MLI are arranged as per Fig.4 with PV panels of 50W,75W and 100W of 12V. This has maintained the desirable voltage ratio (1:2:5) to reach the required output. The PV voltages are stepped up using boost converter with PI controller to settle the converter output voltage by varying the duty cycle. As explained in figure 4.4, first voltage source for HybMLI is boosted from 12V to 37V, second voltage source is boosted from 24V to 73V and the third voltage source is boosted to 189V from 60V. The preferable triggering angles for operating the HybMLI with minimum THD is evolved by programming the modified JAYA optimization algorithm.

The minimum THD that has been obtained with modulation index 0.91 using the above algorithm is 2.23% and the corresponding triggering angles are:

$\alpha_1 = 3.238^0$, $\alpha_2 = 7.760^0$, $\alpha_3 = 19.973^0$, $\alpha_4 = 23.426^0$, $\alpha_5 = 30.31^0$, $\alpha_6 = 46.378^0$, $\alpha_7 = 71.92^0$.

The tunning constants for the above algorithm are set to,

$A_{min} = 0.25$ and $A_{max} = 0.6$.

The performance and expertise of this proposed algorithm is endorsed by developing this optimization program through standard JAYA and modified PSO(MPSO) algorithm with comparative evaluation. JAYA algorithm has resulted the output voltage THD to 2.5% with the suitable triggering angles,

$\alpha_1 = 1.40^0$, $\alpha_2 = 6.32^0$, $\alpha_3 = 10.73^0$, $\alpha_4 = 14.90^0$, $\alpha_5 = 22.19^0$, $\alpha_6 = 27.42^0$, $\alpha_7 = 41.90^0$.

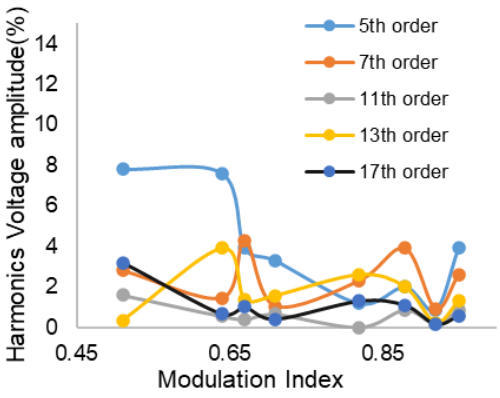
The THD that has derived from MPSO is 2.58% and the respective switching angles are: $\alpha_1 = 0.18^0$, $\alpha_2 = 5.127^0$, $\alpha_3 = 9.10^0$, $\alpha_4 = 13.76^0$, $\alpha_5 = 19.91^0$, $\alpha_6 = 26.12^0$, $\alpha_7 = 42.13^0$.

The tunning parameters for MPSO are set to:

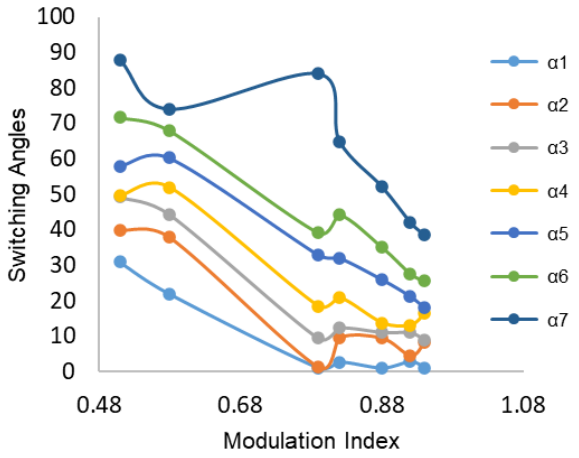
C1 = 2.0, C2 = 1.9, C3 = 2.1, C4 = 1.7, Wmin = 0.4, Wmax = 0.6.

The optimized angles are obtained from JAYA and MPSO algorithm at the same modulation index 0.91.

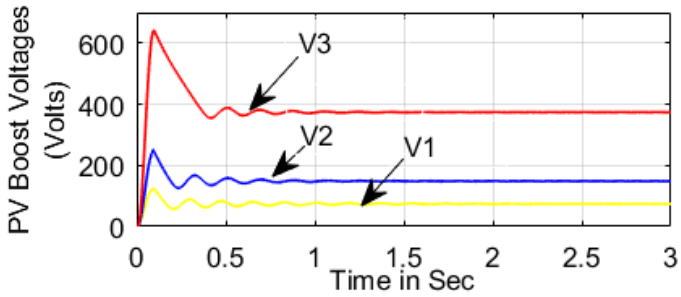
From the above result it is verified that Modified JAYA has attended the minimum THD for the proposed MLI. The voltage THD is obtained for different values of modulation indices. The harmonic voltages behaviour with respect to modulation index and switching angles variation with respect to the same are described in figure 4.6(a) and 4.6(b) respectively. The PV boost voltages waveform to the reduced MLI is cited in figure 4.6(c). The proposed MLI is simulated for a three-phase medium voltage PV standalone system. To obtain the desired voltage range, a balanced three phase RL load is connected across output of the MLI. The line voltage and load current are 850volts (RMS), 0.5mA (RMS) respectively. The line voltage, phase voltages and load current waveforms are displayed in figure 4.7. FFT analysis graph for modulation index 0.91 from simulation is also shown in figure 4.7(d) that presented the minimum THD of output voltage up to 39th harmonics order.



(a)



(b)



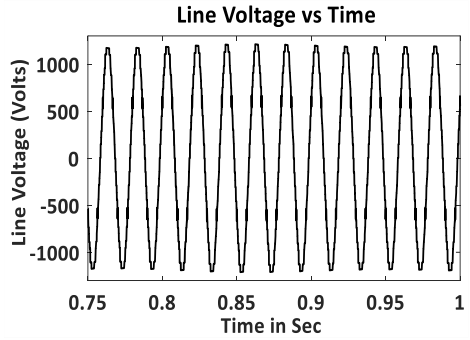
(c)

Figure 4.6. (a)Harmonic voltages amplitude (% of fundamental) with respect to modulation index, (b) Switching angles vs Modulation Index, (c) PV Boost voltages (in Volts) with respect to Time

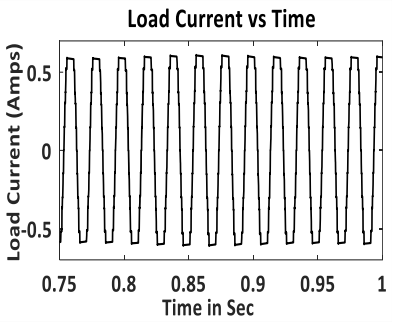
The calculated voltage THD and the voltage THD from simulation for several modulation indices are shown in Table 4.3.

Table 4.3. Evaluation of output voltage THD with different modulation indices derived from Modified JAYA algorithm

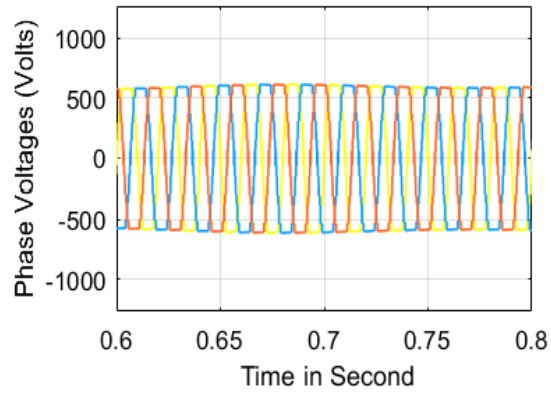
Modulation Index	**Calculated Voltage THD (%)**	**Voltage THD from simulation (%)**
0.6	5.78	6.1
0.7	5.4	5.56
0.8	2.4	2.48
0.86	2.6	2.66
0.91	2.17	2.23
0.92	2.42	2.53
0.94	6.3	6.6



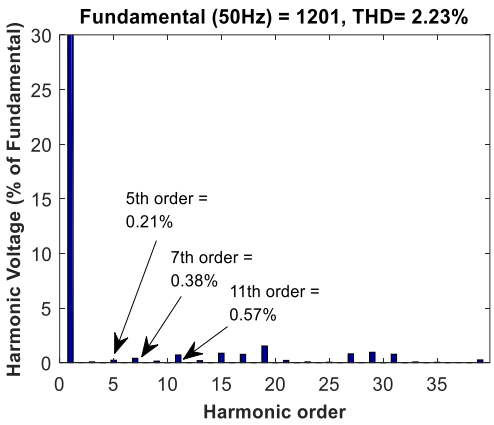
(a)



(b)



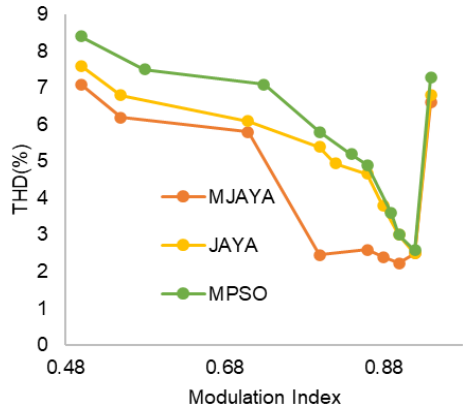
(c)



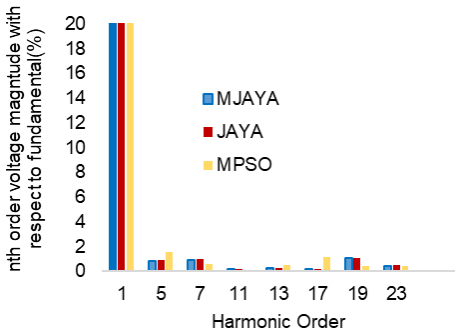
(d)

Figure 4.7. (a) Line Voltage vs Time, (b) Load current vs Time, (c) phase voltages with respect to time and (d) FFT analysis of inverter output voltage

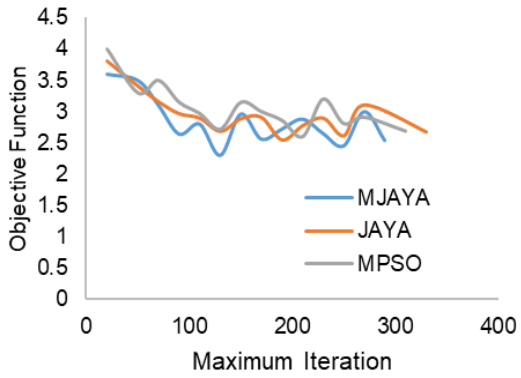
The effectiveness of modified JAYA (MJAYA) algorithm over conventional JAYA and modified PSO in different aspects has been demonstrated with the help of Figure 4.8 and Table 4.4.



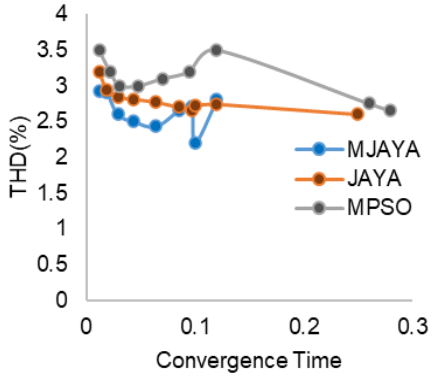
(a)



(b)



(c)



(d)

Figure 4.8. (a) Modulation index vs THD, (b) FFT analysis graph, (c) Maximum Iteration vs Objective function, (d) Convergence Time vs THD (for MJAYA, JAYA and MPSO algorithm)

From figure 4.8 (a) it has been observed that MJAYA has obtained the lower voltage THD at each modulation index than other two algorithms. In figure 4.8(b) the FFT analysis has been shown for three applied algorithms. Here, it can be observed that MJAYA has suppressed the lower as well as higher order harmonic voltages effectively in comparison to JAYA and MPSO. Figures 4.8 (c) and 4.8 (d) show a faster convergence rate of MJAYA algorithm than JAYA and MPSO.

Table 4.4. Comparative Evaluation Among Modified JAYA, JAYA and MPSO Algorithm

Sl NO	Modified JAYA	JAYA	MPSO
Maximum Iteration to Converge	130	190	210
Convergence Time	0.08Sec	0.25Sec	0.28Sec
Tunning Parameters	1	0	2
Line voltage THD (with modulation index 0.91)	2.23%	2.50%	2.58%
5^{th} harmonic voltage amplitude	0.21%	1.35%	1.53%
7^{rth} harmonic voltage amplitude	0.38%	1.11%	0.60%
11^{th} harmonic voltage amplitude	0.57%	0.23%	0.13%

4.6 LOSS CALCULATION of HYBRID MLI

In order to determine the efficiency of the proposed MLI, the loss calculation for a single phase 15-level HybMLI is derived. The total loss of a semiconductor switch is determined by conduction loss and switching loss.

4.6.1 Conduction Loss

Conduction loss of a switch is determined by:

$$P_{conduction} = P_{LT} + P_{LD} \tag{4.16}$$

Here P_{LT} is the conduction loss of transistor and P_{LD} is the reverse conduction loss of antiparallel diode in each MOSFET. The reduced MLI consists of 8 power switches and the total loss are calculated using following equations.

$$P_{LT} = \frac{1}{T}\int_{t_1}^{t_2}[V_T + r_T\beta I(t)]I(t)dt \tag{4.17}$$

$$P_{LD} = \frac{1}{T}\int_{t_1}^{t_2}[V_d + r_D\beta I(t)]I(t)dt \tag{4.18}$$

Where t_1 and t_2 are the time interval of a switch to conduct and T is the total time of operation. The on state voltage drop across transistor is given by V_T and reverse voltage drop across diode is given by V_d. r_T and r_D are the resistances of transistor and diode respectively, β is gain constant and the instantaneous current across switch during conduction is denoted as I(t). With the help of these equations the total conduction loss for 8 switches of HybMLI is calculated and it is 2.07watt.

4.6.2 Switching Loss

Switching loss for each power switch is calculated at the time of turning on and turning off in the entire cycle. Switching loss is determined by using equation (4.19)

$$P_s = \frac{1}{T}\left[E_{on}N_{on} + E_{off}N_{off}\right] \quad (4.19)$$

Where E_{on} and E_{off} are the on state and off state energy losses respectively of a power switch. N_{on} and N_{off} represent the number of times a power switch is getting on and off respectively over the entire time of operation.

$$E_{on} = \frac{1}{6}[V_{sd}I_s t_{on}] \quad (4.20)$$

$$E_{off} = \frac{1}{6}\left[V_{sd}I_s t_{off}\right] \quad (4.21)$$

Here V_{sd} is the voltage across a switch before switching on or after switching it off and I_s is the current across switch after switching on or before switching off. The turn on time and turn off time of a particular switching device are represented by t_{on} and t_{off}. Loss during turn on and turn off for all the switches of reduced MLI is calculated to 0.0038watts. Now the total power loss of the MLI is 2.0738watt. The output power of the single phase HybMLI is 58watt. The overall efficiency of the proposed MLI exhibits an efficiency of 96.74%.

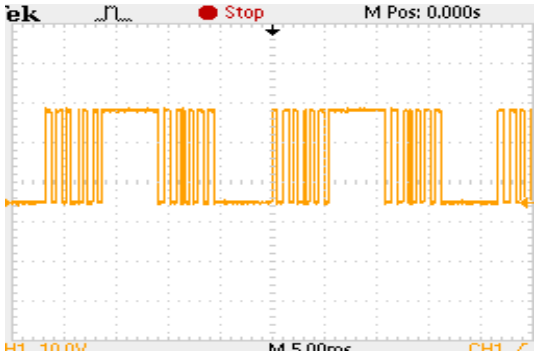
4.7 EXPERIMENTAL VERIFICATION

The performance of the proposed MLI is demonstrated by developing a 15-level prototype. The MLI is designed with eight IGBTs and the gate pulses to the switches are provided using

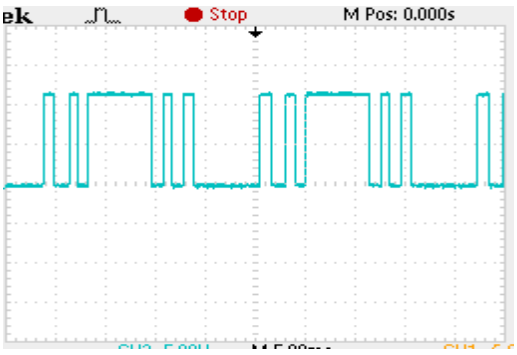
18F452 microcontroller and TLP250H driver circuit. The output voltage, current waveforms in different loading condition and harmonic spectrum are recorded by the help of DSO model no-TDS 2022B. The DC voltages of 12Volts, 24Volts and 60Volts (with the ratio 1:2:5) are provided to operate the MLI for achieving required output voltage level. Component list for hardware setup is provided in Table 4.5 with their specification. The gate pulses to the reduced switch MLI are recorded and cited in figure 4.9 that satisfies the switching arrangement demonstrated by Table 4.1. The output voltage and current waveforms for RL load with power factor 0.86 and current waveforms with R load are displayed in figure 4.10. The FFT voltage and current spectrum with a modulation index 0.91 with same load are shown by figure 4.11.

Table 4.5. List of Components

SI NO	Components	
1	optocoupler (Driver Circuit)	TLP250H
2	Microcontroller	PIC18f452
3	IGBT	IE15AB
4	Load	R= 100Ω, L= 0.19H



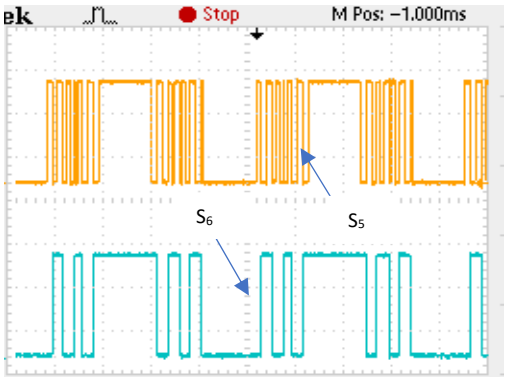
(a)



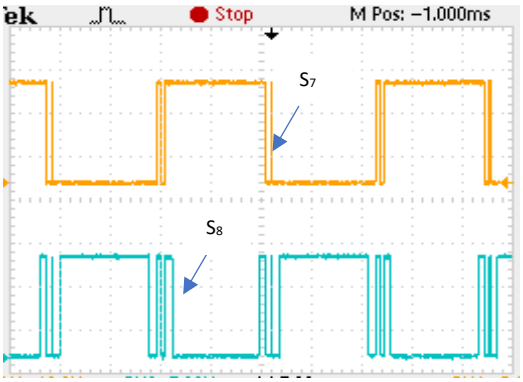
(b)

(c)

(d)

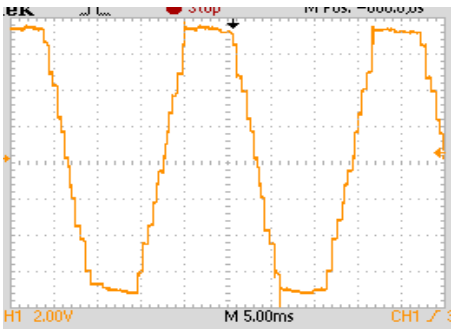


(e)

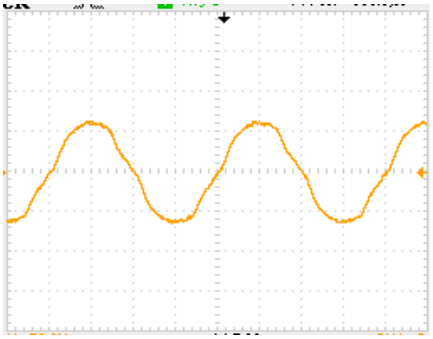


(f)

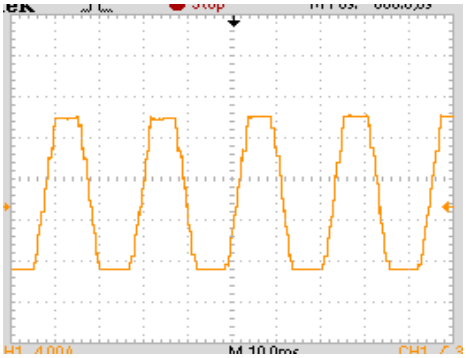
Figure 4.9. (a) gate pulse to S_1, (b) gate pulse to S_2, (c) gate pulse to S_3, (d) gate pulse to S_4, (e) gate pulses to S_5 and S_6, (f) gate pulses to S_7 and S_8 (Scale: Y axis=5volts/div)



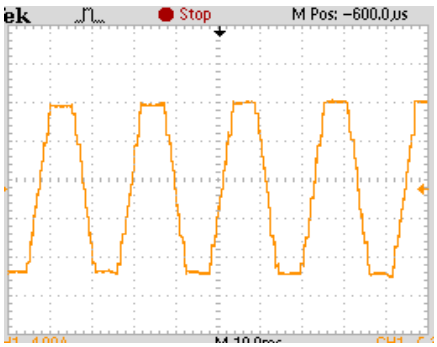
(a)



(b)

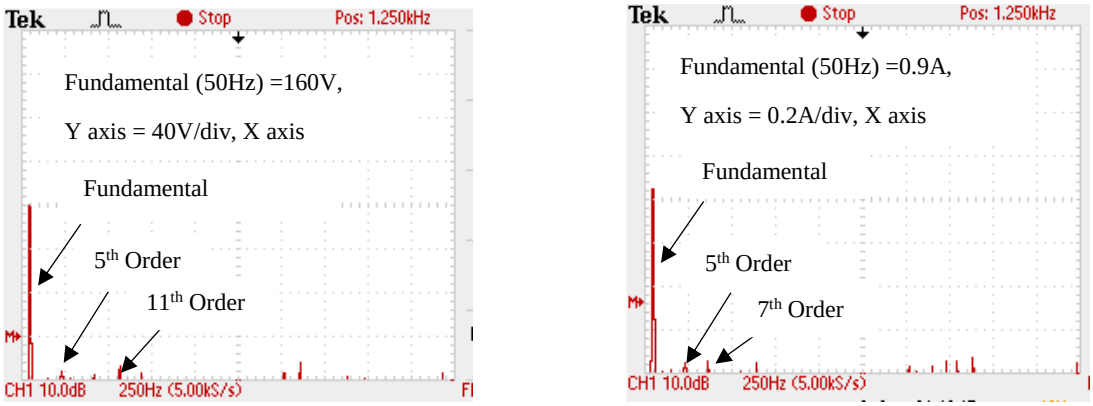


(c)



(d)

Figure 4.10. (a) Output Voltage waveform with RL Load, (b)Current waveform with RL load at 0.86pf, (c) current waveform with R Load, (d) current waveform with R load when load resistance reduced to 50% [(scale: - for figure (a) channel1: y axis=40v/div), (scale: - for figure (b) channel1: y axis=0.5A/div), (scale: - for figure (c), (d) channel1: y axis=1A/div]



(a) (b)

Figure 4.11. (a) Harmonic spectrum of Output Voltage, (b) Harmonic spectrum of load current

From the harmonic spectrum it is shown that the lower order harmonics are supressed successfully. The experimental setup photograph is cited in figure 4.12.

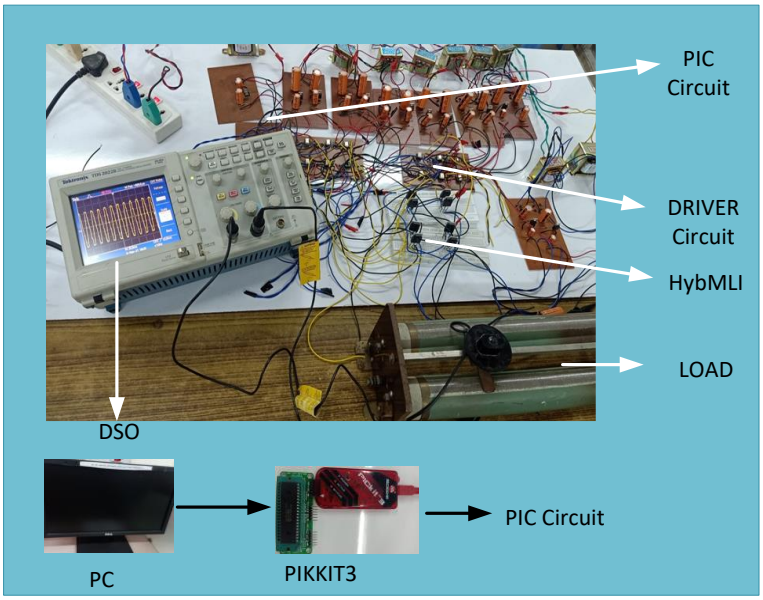


Figure 4.12. Experimental setups for 15-level HybMLI operation

4.8 OBSERVATION

This chapter offered a Hybrid design of reduced MLI capable of providing 15-levels of output voltage with the fewest possible power switches. The comparison analysis revealed that the proposed MLI does not make use of any additional diodes or capacitors, in contrast

to the other MLIs that were provided. The ideal switching angles are calculated with a modified version of the JAYA algorithm in order to get the lowest possible output voltage THD. In comparison to the various population-based algorithms that have been presented, the suggested approach has produced the lowest voltage THD while requiring the fewest possible tuning variables. The efficacy of the modified JAYA algorithm applied to the reduced MLI is demonstrated and validated by experimental investigation. It has been determined, based on the findings of the simulation as well as the experiments, that the inverter design works well for use in PV-based standalone applications.

4.9 PUBLICATION

[1] R. Mohanty, D. Chatterjee, S. Suman and M. Anand, "A Reduced Switch Count Multilevel Inverter for PV Standalone System using Modified JAYA Algorithm," International Journal of Electronics, Taylor and Francis, 2022 DOI: 10.1080/00207217.2022.2164073.

4.10 REFERENCES

[4.1] A. K. Singh, S. Kumar, and B. Singh, "Solar PV Energy Generation System Interfaced to Three Phase Grid with Improved Power Quality," *IEEE Trans. Ind. Electron.*, vol. 67, no. 5, pp. 3798–3808, 2020, doi: 10.1109/TIE.2019.2921278.

[4.2] M. Easley, M. B. Shadmand, and H. Abu-Rub, "Hierarchical Model Predictive Control of Grid-Connected Cascaded Multilevel Inverter," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 3, pp. 3137–3149, 2021, doi: 10.1109/JESTPE.2020.3015128.

[4.3] S. S. Letha, T. Thakur, and J. Kumar, "Hardware Implementation of Power Quality Improvement in Photo-Voltaic Fed Cascaded H-Bridge Multilevel Inverter," *IEEE Int. Symp. Ind. Electron.*, vol. 2018-June, pp. 401–406, 2018, doi: 10.1109/ISIE.2018.8433752.

[4.4] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 135–151, 2016, doi: 10.1109/TPEL.2015.2405012.

[4.5] M. A. Hosseinzadeh, M. Sarebanzadeh, M. Rivera, E. Babaei, and P. Wheeler, "A

Reduced Single-Phase Switched-Diode Cascaded Multilevel Inverter," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 3, pp. 3556–3569, 2021, doi: 10.1109/JESTPE.2020.3010793.

[4.6] R. Agrawal and S. Jain, "Multilevel inverter for interfacing renewable energy sources with low/medium- and highvoltage grids," *IET Renew. Power Gener.*, vol. 11, no. 14, pp. 1822–1831, 2017, doi: 10.1049/iet-rpg.2016.1034.

[4.7] H. Vahedi, S. Member, M. Sharifzadeh, and S. Member, "Modified Seven-Level Pack U-Cell Inverter for Photovoltaic Applications," vol. 6, no. 3, pp. 1508–1516, 2018.

[4.8] I. A. Harbi, H. Z. Azazi, A. E. Lashine, and A. E. Elsabbe, "A higher levels multilevel inverter with reduced number of switches," *Int. J. Electron.*, vol. 105, no. 8, pp. 1286–1299, 2018, doi: 10.1080/00207217.2018.1440429.

[4.9] M. F. Kangarlu and E. Babaei, "Cross-switched multilevel inverter: An innovative topology," *IET Power Electron.*, vol. 6, no. 4, pp. 642–651, 2013, doi: 10.1049/iet-pel.2012.0265.

[4.10] Y. Ounejjar, K. Al-Haddad, and L. A. Grégoire, "Packed U cells multilevel converter topology: Theoretical study and experimental validation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1294–1306, 2011, doi: 10.1109/TIE.2010.2050412.

[4.11] K. P. Panda and G. Panda, "Application of swarm optimisation-based modified algorithm for selective harmonic elimination in reduced switch count multilevel inverter," *IET Power Electron.*, vol. 11, no. 8, pp. 1472–1482, 2018, doi: 10.1049/iet-pel.2017.0697.

[4.12] A. Routray, R. K. Singh, and R. Mahanty, "Harmonic Reduction in Hybrid Cascaded Multilevel Inverter Using Modified Grey Wolf Optimization," *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 1827–1838, 2020, doi: 10.1109/TIA.2019.2957252.

[4.13] R. Venkata Rao, "Jaya: A simple and new optimization algorithm for solving constrained and unconstrained optimization problems," *Int. J. Ind. Eng. Comput.*, vol. 7, no. 1, pp. 19–34, 2016, doi: 10.5267/j.ijiec.2015.8.004.

[4.14] S. Mishra and P. K. Ray, "Power Quality Improvement Using Photovoltaic Fed DSTATCOM Based on JAYA Optimization," *IEEE Trans. Sustain. Energy*, vol. 7, no. 4, pp. 1672–1680, 2016, doi: 10.1109/TSTE.2016.2570256.

Chapter-5

Proposed Single PV Source Based Grid Interactive Asymmetrical Reduced Switch MLI using Red Deer Optimization

An asymmetrical reduced switch MLI for grid integration is presented with single active voltage source. The performance of the MLI and its operation is discussed. Scheme for integrating the PV source with grid and the control technique has been discussed. Harmonic reduction using Red Deer Optimization algorithm is presented. The potential of the algorithm is proved by comparative study and presented.

PROPOSED SINGLE PV SOURCE BASED GRID INTERACTIVE ASYMMETRICAL REDUCED SWITCH MLI USING RED DEER OPTIMIZATION

5.1 INTRODUCTION

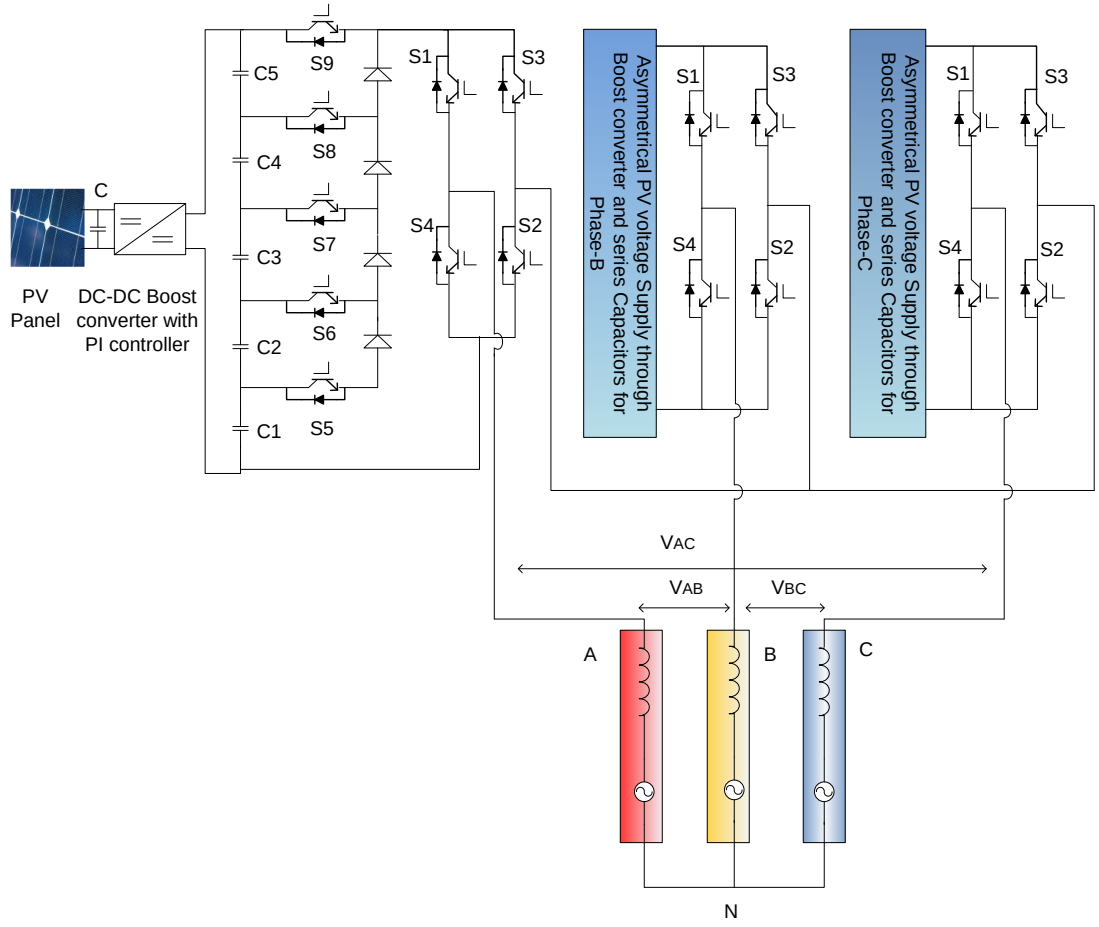
Conversion of lower capacity solar energy to higher one and integration with low, medium and high voltage grid with proper control technique is the biggest challenge. In order to avoid the bulky step-up transformer along with power conversion stage in PV-grid interconnection a new medium voltage dc collection grid method with an interleaved modular dc-dc converter is introduced in [5.1] for MPPT tracking. As per the review status [5.2], there are several possibilities of harmonic distortion in low power network that powered by solar energy and the factors influencing for rise of total harmonics distortion (THD) in a real time micro grid application. Multilevel inverter was introduced in different articles for its modular nature and simplicity as it does not need reactive components for filter circuit to eliminate undesirable harmonics from the system which have already discussed in previous chapters. Due to higher number of power switches for generating higher voltage level, reduced MLIs of different topology with their switching techniques have been introduced in different research articles [5.3] - [5.8]. To operate the MLI with fundamental frequency for minimizing the switching stress, fundamental switching frequency modulation in [5.9] and optimal direct current control method in [5.10] are proposed. But a larger number of equations are solved to generate suitable switching pulses for harmonic control in the above literatures. Despite of this, nature inspired optimization algorithms are shown their efficiency in solving different complex problems in different aspects. Particle swarm optimization (PSO) in [5.11], [5.12] is implemented for harmonics elimination using MLI. A modified species PSO in [5.13] and modified PSO in [5.14] are implemented in CHBMLI and reduced MLI respectively to optimize the THD across output. Modified Grey Wolf Optimization in [5.15] has also been implemented in hybrid cascaded MLI for harmonic reduction.

In this chapter an 11-level series capacitor based reduced H- bridge MLI topology is proposed to integrate the PV voltage with low voltage grid which is energized by asymmetrical voltages. The proposed design is an improvement of the existing topology as discussed in [5.16]. This reduced MLI is operated with single PV panel in each phase to

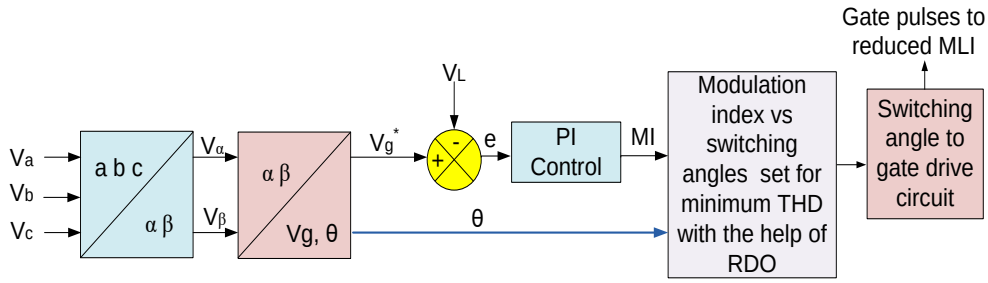
reduce the total cost of the system. Asymmetrical reduced switch MLI and asymmetrical H-bridge MLI are discussed in [5.17] and [5.18] along the comparison with symmetrical topologies. In this research an asymmetrical H-bridge reduced MLI is used to prune the voltage THD near grid side with the help of a new population-based algorithm called Red Deer Optimization (RDO) algorithm proposed in [5.19]. To prove the effectiveness of this algorithm, the reduced MLI is designed with the optimum switching angles derived from PSO and GWO algorithm and the comparative analysis is described in section 5.4. The PV energy is synchronized with grid through reduced MLI by implementing piecewise mixed model discussed in [5.20] for online control. A set of linear and nonlinear equations of switching angles with different modulation indices are developed to find optimum switching angles using RDO considering least voltage THD. The angles are stored in the processor memory for online application. To verify the entire concept of the proposed scheme, simulation and experimental analysis are performed on a three phase system with efficient power conversion through 11-level capacitor based asymmetrical reduced MLI.

5.2 PROPOSED SCHEME

The motive of designing this scheme is to implement an upgraded reduced multilevel inverter which would use a single source to get the staircase voltage waveform with optimum THD. Instead of using similar voltage at each level, here unequal voltages are provided through series capacitances that result different grading of voltage across output to make the system less distorted with lower and higher order of harmonics.



(a)



(b)

Figure 5.1. (a) Three phase circuit arrangement of 11-level reduced Multilevel Inverter energized with single PV supply, (b) Control arrangement of the system

5.2.1 PV Boost converter control

The developed system is energized from three 260 watts PV panels. For each phase only one panel is used to provide the multi-input voltages to the reduced MLI through series capacitors that appeared in figure 5.1(a). The PV output voltage is boosted up with the help of DC-DC

power converter and the duty cycle of the converter has been controlled through PI controller to set a constant step-up voltage across series capacitances. The boost converter is operated in high frequency of 20KHz. With the help of PI controller, the gate pulse has been induced by comparing the reference signal of above-mentioned frequency with carrier signal for boost converter switch. The block diagram for PI control has been illustrated in figure 5.2.

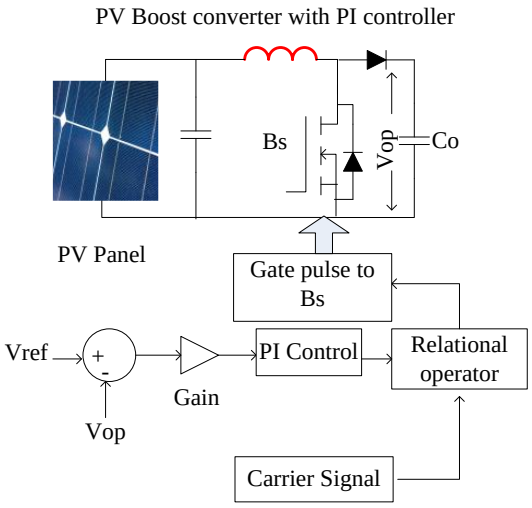


Figure 5.2. Block Diagram of PI control for Boost Converter

In the above figure V_{op} is the PV output voltage, which compared with the reference output voltage and the error signal is processed through PI controller and the output signal has been compared with carrier signal through relational operator. The generated signal or pulse has been fed to boost converter switch for its operation. The expression of boost output voltage is given by,

$$V_{op} = \frac{V_i}{1-D} \tag{5.1}$$

Where, V_i is input to the boost converter and D is the duty cycle of boost converter.

5.2.2 Series Capacitor based reduced MLI

This proposed MLI uses only single source with series capacitances to generate multilevel output voltage. This topology also requires lower number of switching devices with few numbers of diodes for developing higher level and higher rating of output voltage. With the comparison of conventional cascade H-bridge MLI (CHBMLI), It has been observed that

this reduced MLI uses half the number of switching devices for generating same level of output voltage. The number of semiconductor switches required for the operation of proposed reduced MLI for generating V_l output voltage is:

$$N_{sw} = 4 + N \tag{5.2}$$

The circuit arrangement and operation of the proposed MLI has been described below with RL load.

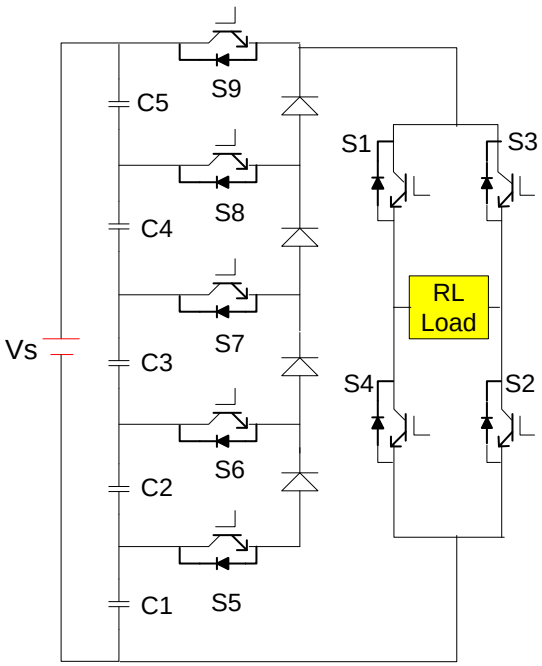


Figure 5.3. Circuit arrangement of 11-level reduced H-bridge MLI

Operation of this MLI has been carried out by the suitable switching scheme. The switching pattern of these nine semiconductor switches for the entire cycle are described in Table 5.1. Status of a switch '0' is treated as turn off condition and '1' is treated as turn on condition. As this reduced MLI has been designed for asymmetrical voltage supply to reduce the THD across output voltage, capacitors C1-C5 are different in values. These capacitors are treated as the voltage divider, which shares the source voltage unequally after getting charged as per their capacitance values. Here the voltage relation across capacitors can be given by equation (5.3). The voltages V1-V5 are treated as the voltages across C1-C5.

$$V1 \neq V2 \neq V3 \neq V4 \neq V5 \tag{5.3}$$

Table 5.1. Switching pattern for reduced H-bridge MLI

	Voltage level											
Switches	0	V1	V1+V2	V1+V2+V3	V1+V2+V3+V4	V1+V2+V3+V4+V5	0	-(V1)	-(V1+V2)	-(V1+V2+V3)	-(V1+V2+V3+V4)	-(V1+V2+V3+V4+V5)
S1	0	1	1	1	1	1	0	0	0	0	0	0
S2	0	1	1	1	1	1	0	0	0	0	0	0
S3	0	0	0	0	0	0	0	1	1	1	1	1
S4	0	0	0	0	0	0	0	1	1	1	1	1
S5	0	1	0	0	0	0	0	1	0	0	0	0
S6	0	0	1	0	0	0	0	0	1	0	0	0
S7	0	0	0	1	0	0	0	0	0	1	0	0
S8	0	0	0	0	1	0	0	0	0	0	1	0
S9	0	0	0	0	0	1	0	0	0	0	0	1

Referring Table 5.1, the operation of reduced MLI to result V1 across output is explained in figure 5.4 (a)

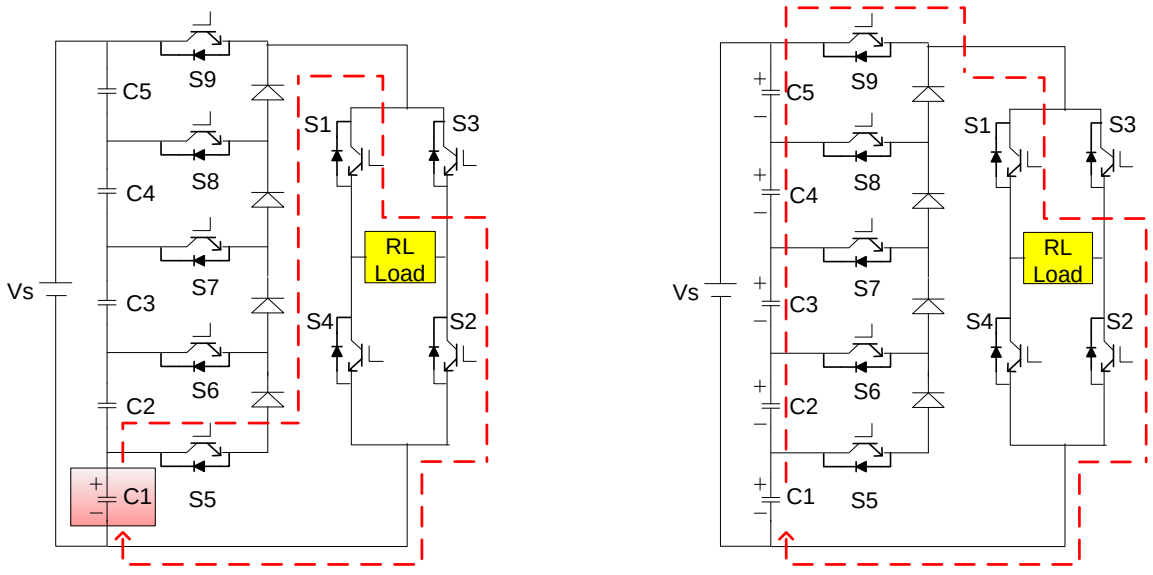


Figure 5.4. (a) Circuit operation of 11-level MLI to get 'V1', (b) Circuit operation of 11-level MLI to get maximum positive output voltage

To obtain V1 voltage across output, switches S5, S1, S2 are turned on and the rest six switches are turned off completely. In the above figure the current direction from source

(capacitive voltage c1) to load is conveyed through the arrow. To achieve the maximum positive voltage i.e., V1+V2+V3+V4+V5, the switches S9, S1, S2 will be operated for the positive half cycle and the circuit operation is explained through figure 5.4(b). in the same way the rest of the voltage level can be achieved by operating the power switches according to the Table 5.1.

5.2.3 Mathematical Modelling

The output voltage expression of MLIs with equal voltage sources can be derived by,

$$V(\omega t) = \sum_{\alpha=1}^{ai} \frac{4V_D}{n\pi} (\cos(n\alpha_1) + \cos(n\alpha_2) + \cdots + \cos(n\alpha_{ai}))\sin(\omega t) \quad (5.4)$$

From equation (5.4) it is cleared that the output voltage and the nth order harmonic voltages are affected by the switching angles of MLIs. These switching angles exhibits a relation which is stated as:

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \cdots < \alpha_{ai} < \pi/2 \quad (5.5)$$

The objective function which needs to minimize by the application of MLIs from system voltage is the Total Harmonics Distortion (THD).

$$THD = \frac{\sqrt{\sum_{n=3,5,7}^{49} V_n^2}}{V_1} \quad (5.6)$$

Where V_1 is the fundamental output voltage. From equation (5.6) it can be stated that the minimum value of THD can be obtained by selecting suitable switching angles for MLI operation.

Now considering the MLIs that are operating with unequal voltage sources, the output voltage waveform, and the expression of the same are designated in figure 5.5 and equation (5.8) respectively. Here each voltage source exhibits a relation of some fraction with the common or nominal voltage 'V_D'. In this case the output voltage is driven between +k5V_D to -k5V_D. k1-k5 are the fraction of five DC source voltages and the relationship among these that are set here is:

$$k1 < k2 < k3 < k4 < k5 \tag{5.7}$$

In this scheme the series capacitors used across a source voltage are unequally chosen with the above fractions. Here the common capacitance is taken as 2200µF for simulation and C1 value is k1*2200µF. Similarly, all the other capacitances are chosen. From figure 5.5, it can be clearly observed that the uneven staircase waveform is closer to fundamental waveform which leads to minimum voltage THD than symmetrical sources of MLIs. The expression of output voltage waveform with Fourier analysis is determined by equation (5.8).

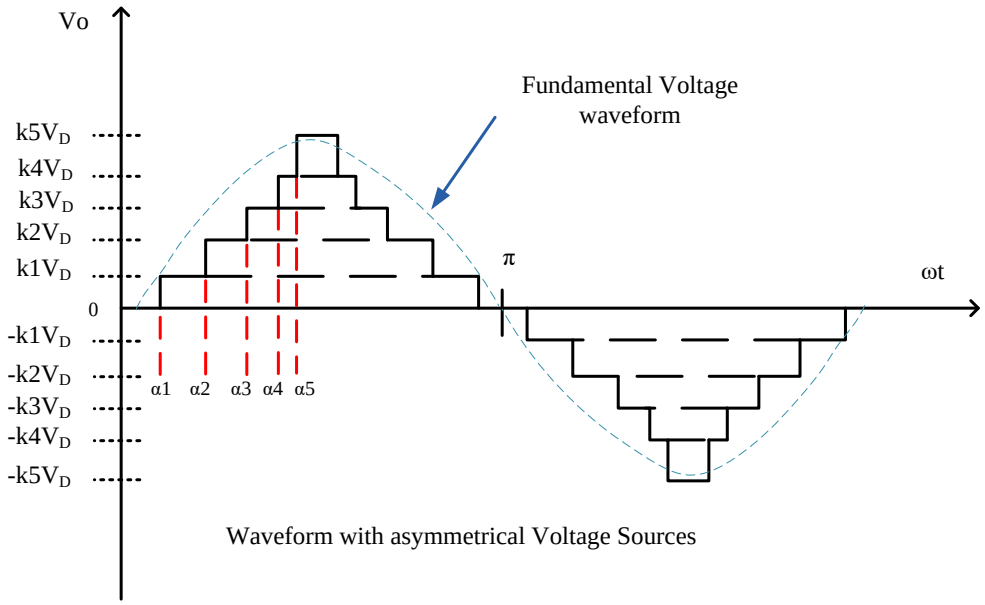


Figure 5.5. 11-level output voltage with unequal voltage sources

$$V(\omega t) = \sum_{\alpha=1}^{ai} \frac{4V_D}{n\pi}\left(k1 * cos(n\alpha_1) + k2 * cos(n\alpha_2) + \cdots + kai * cos(n\alpha_{ai})\right) sin(n\omega t) \tag{5.8}$$

From the above expression the output voltage and the nth harmonic voltages are not only depend on the switching angles but also on the DC voltages fraction. From equation (5.6) and equation (5.8), to obtain a minimum output voltage THD from the reduced MLI, it is necessary to get the proper values of input voltages fraction (k1-k5) with the optimum switching angles. In this chapter to procure the minimum THD or to reduce the nth order harmonic voltages from the output, Red Deer Optimization (RDO) algorithm with a modified

version is employed to get the suitable switching angles and capacitors fractional values for the operation of above proposed MLI.

5.3 RED DEER OPTIMIZATION ALGORITHM (RDO)

This new meta-heuristic algorithm is proposed by Amir Mohammad Fathollahi-Fard et.al in 2020. This is a nature influenced algorithm that emulates the mating behaviour of Scottish red deer in breading season to get new offspring. The convergence of this evolutionary algorithm has been achieved by competition among two groups of male red deer to get mate with hinds or female red deer by performing their roaring capacity. The superiority of this new optimization algorithm has proved in comparison with different existing metaheuristic algorithm by solving some multi-objective optimization problem as mentioned in [5.19].

This algorithm is also initiated by randomly initializing the population that is red deer. The best red deer are treated as male red deer and the rest are known as hinds. Among the male red deer, commanders are selected based on their roaring power (a). The number of male commanders is calculated as:

$$R_{com} = round\{a * R_{male}\} \tag{5.9}$$

Remaining male red deer are known as stag which are determined by,

$$R_{stag} = R_{male} - R_{com} \tag{5.10}$$

To mate with the hinds the best commander is selected from the fighting process among commander deer and stag. When these two groups confront each other two new solutions are found and the commander are replaced by their best solution. From the fighting process the two new solutions are determined from the given formula.

$$R_{new1} = \frac{(R_{com} - R_{stag})}{2} + (b1 * \big((UB - LB) * b2\big) + LB) \tag{5.11}$$

$$R_{new2} = \frac{(R_{com} - R_{stag})}{2} - (b1 * \big((UB - LB) * b2\big) + LB) \tag{5.12}$$

Where UB and LB are the upper limit and lower limit of population in search space. b1 and b2 are the random number between 0 and 1.

In the next stage the hinds are distributed among the commanders proportionally as per their power. Here the hinds that are selected for mating are computed by,

$$R_{Hind}^{mate} = round\{a * R_{harem}\} \quad (5.13)$$

Where:

$$R_{harem} = round\{P_n * R_{Hind}\} \quad (5.14)$$

P_n is the normalized power of male commander that can possess a portion of hinds.

Now the new offspring is developed or taken birth by the mating process using the following equation.

$$offspring = \frac{(R_{com}+R_{Hind})}{2} + (UB - LB) * c \quad (5.15)$$

C is the random number that uniformly distributed between 0 and 1.

The entire process is modelled in to algorithm to achieve the best optimized result from the best value of population or red deer.

5.3.1 Approach of RDO towards proposed scheme

RDO has been implemented in the above scheme to determine the optimum switching angels and capacitance fractions for 11-level reduced MLI which has resulted minimum voltage THD at grid side. Here the algorithm has been limited up to finding the new solution from fighting process instead of elongating it to generate the new offspring from mating process as discussed in section 5.3. The solution that has been achieved from the new population

after equation (5.11) and (5.122) and its comparison, has fulfilled the motive of using the optimization techniques. The flowchart diagram that explains the algorithm to get the strongest population or optimum switching angles is shown in figure 5.6.

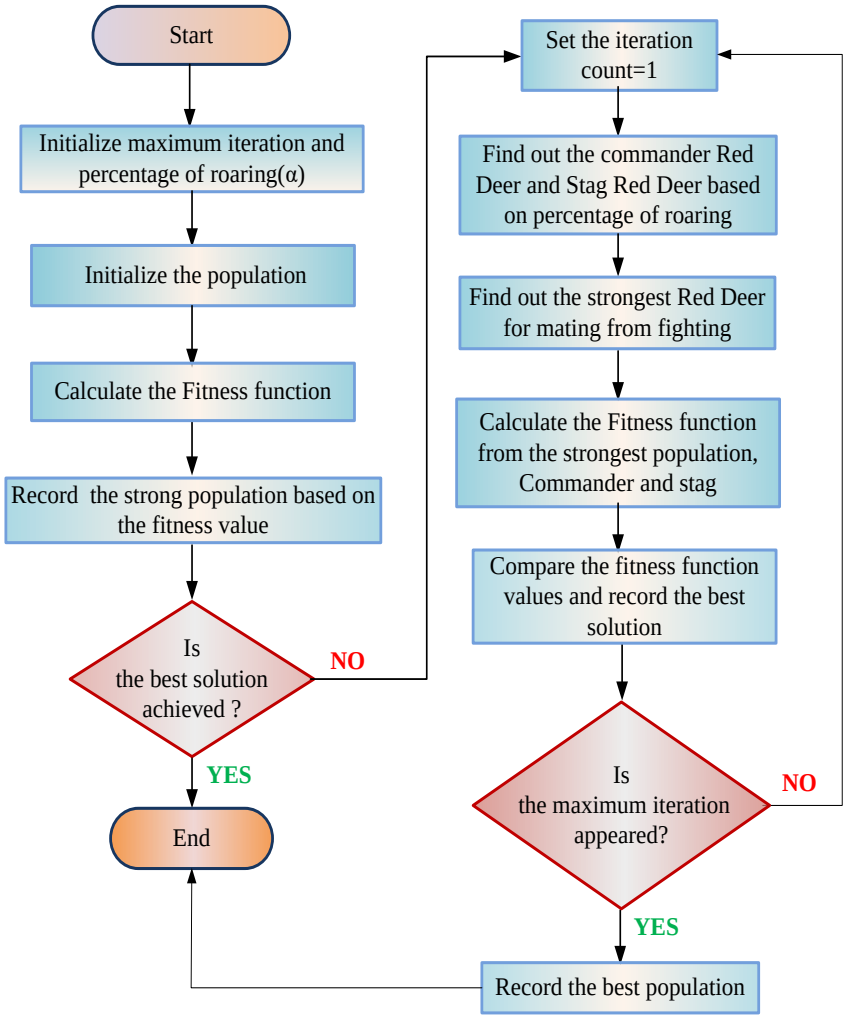


Figure 5.6. Flowchart diagram of RDO Algorithm

Here to design an 11-level reduced MLI for three phase system the following steps are carried out for RDO to get the suitable firing angles i.e., α_1, α_2 ……α_{ai} and capacitance fractions i.e., k1, k2 ……..kai.

STEPS:

i. Set the maximum iteration count, percentage of roaring (a), and the boundaries conditions for population vector.

ii. Randomly initiate the population from 0-π/2 for firing angles and 0.1-2 for fractions of capacitors.

iii. Calculate the fitness function value using equations (5.6) and (5.8) from the initiated populations.

iv. Start iteration count: Roar the male deer using ‘a’ percentage and form the commander and stag male deer using equations (5.9) and (5.10).

v. Generate the new solutions of population from the fighting process through equation (5.11) and (5.12).

vi. Calculate the fitness function from new population and record the best value. Update the population with the former one if the new population gives the best result.

vii. Check the maximum iteration count: If maximum iteration arrived with best solution, terminate the algorithm, or go back to step (iv).

Percentage of roaring of red deer affects the fitness value to a greater extend. At different roaring percentage (a), respective voltage THD is recorded and the suitable ‘a’ value is set for the program. The relation is graphically represented in figure 5.7.

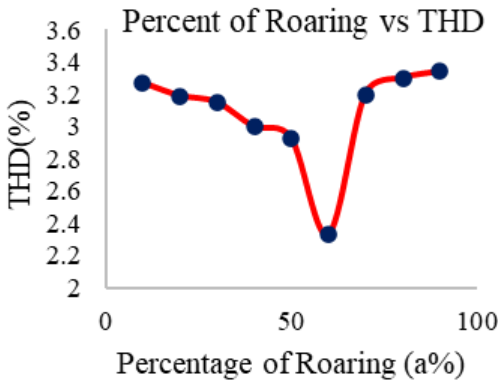


Figure 5.7. Percentage of Roaring to select Commander Red Deer vs THD

From the above figure it has been perceived that the minimum THD has been achieved at 60% of roaring strength of the red deer.

5.4 SIMULATION RESULTS

The performance of the reduced H-bridge inverter and its efficiency are justified by developing a three phase 11-level reduced MLI integrating with PV-grid system through simulation. In each phase the MLI is energized from a single PV panel of 260watts and its voltage is boosted up by means of boost converter as explained in section 5.2.1. The asymmetrical voltage supplies are provided through series capacitances. To diminish the THD across grid side the suitable switching angels and capacitance fraction values are determined by performing three different optimization algorithm and the most efficient one is selected for further demonstration.

The minimum voltage THD that has been resulted through GWO up to 39^{th} order is 3.8% and the corresponding switching angles and fractions of capacitors are:
$\alpha_1 = 1.37^0$, $\alpha_2 = 8.51^0$, $\alpha_3 = 14.41^0$, $\alpha_4 = 20.32^0$, $\alpha_5 = 32.81^0$.
k1= 0.28, k2 = 0.32, k3 = 0.35, k4 = 0.37, k5 = 0.38.

The minimum voltage THD that has been resulted through PSO up to 39^{th} order is 4.1% and the corresponding switching angles and fractions of capacitors are:
$\alpha_1 = 4.25^0$, $\alpha_2 = 6.40^0$, $\alpha_3 = 12.82^0$, $\alpha_4 = 21.07^0$, $\alpha_5 = 33.43^0$.
k1= 0.29, k2 = 0.357, k3 = 0.426, k4 = 0.487, k5 = 0.543.
The preferable switching angles and fractions value using RDO algorithm are:
$\alpha_1 = 3.532^0$, $\alpha_2 = 6.767^0$, $\alpha_3 = 12.308^0$, $\alpha_4 = 24.769^0$, $\alpha_5 = 39.973^0$.
k1 = 0.542, k2 = 0.609, k3 = 0.83, k4 = 0.9, k5 = 0.98.

The above set of angles and fractions are minimized the voltage THD to 2.33% at grid side and 3.52% at load side which is reduced to a greater extend in comparison to GWO and PSO algorithm.

Using the above data, the proposed scheme was simulated with the help of MATLAB16b. The reduced MLI line voltage and system current are recorded before connecting the grid

across three phase RL load, the THD values at different load conditions are shown through FFT analysis.

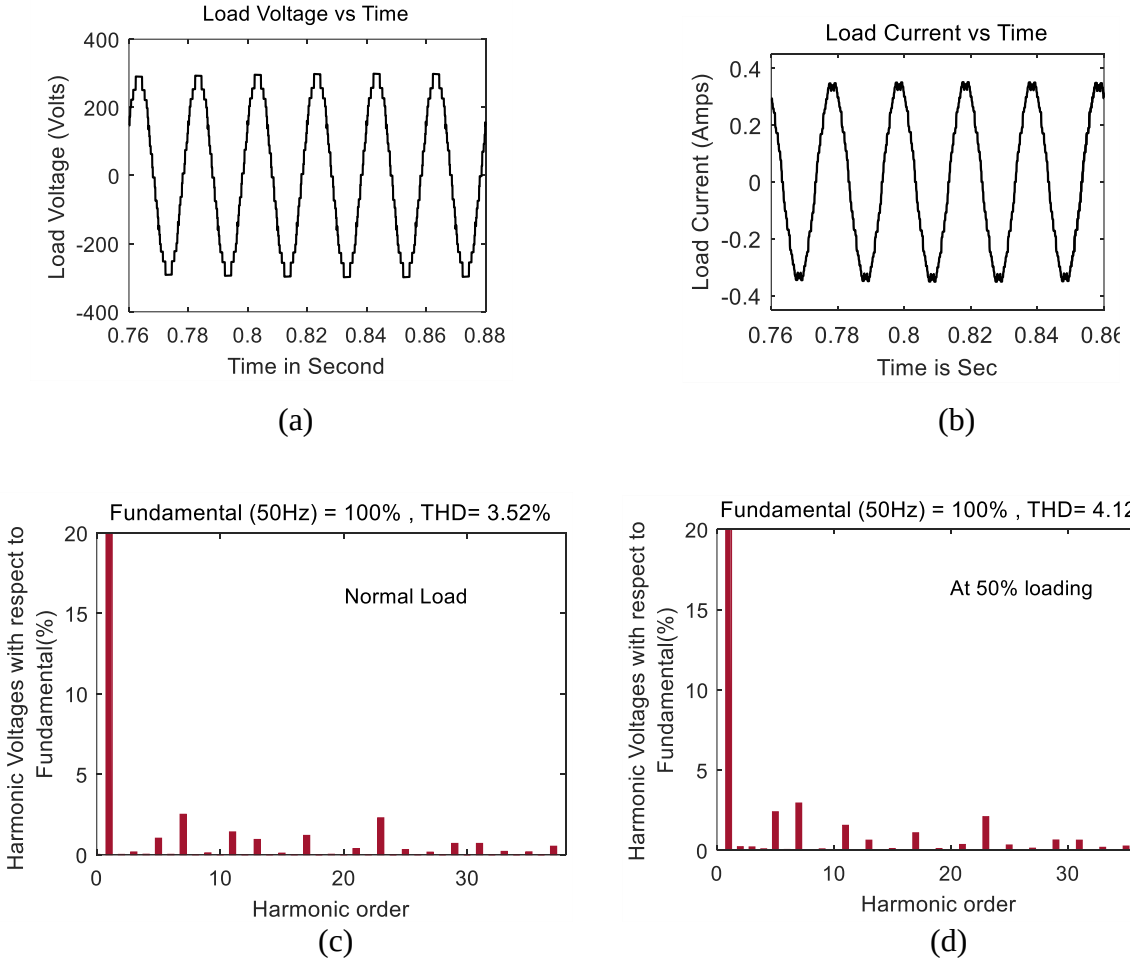


Figure 5. 8. (a) Line Voltage in Volts with respect to Time across load, (b) Load Current in Amps with respect to Time, (c) FFT analysis of line voltage at normal load, (d) FFT analysis at 50% load

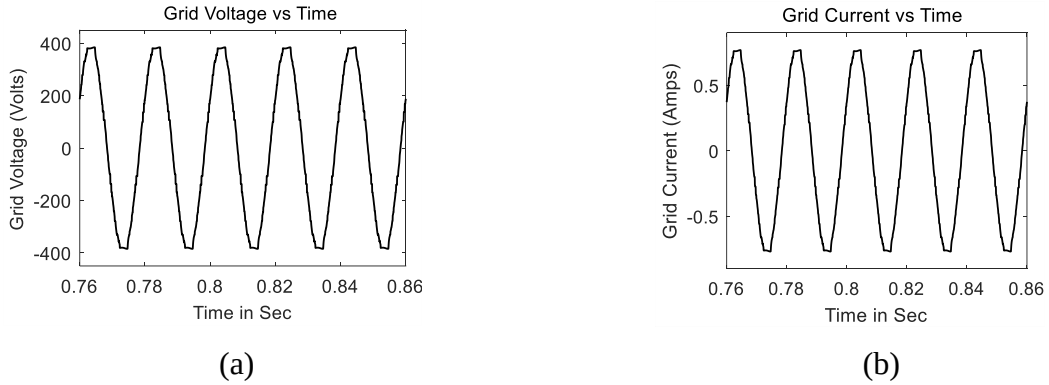


Figure 5.9. (a) Grid line voltage in Volts with respect to Time, (b) Grid current in Amps with respect to Time

The converter output is synchronized with a low voltage grid of 240 volt after satisfying the prior condition and FFT analysis are done to check the system efficiency towards power quality. The line voltage at grid side and the current waveforms are shown in figure 5.9. The FFT analysis result for RDO and comparison with GWO and PSO are cited in figure 5.10, which shows the overall voltage THD and distortion due to harmonics voltage.

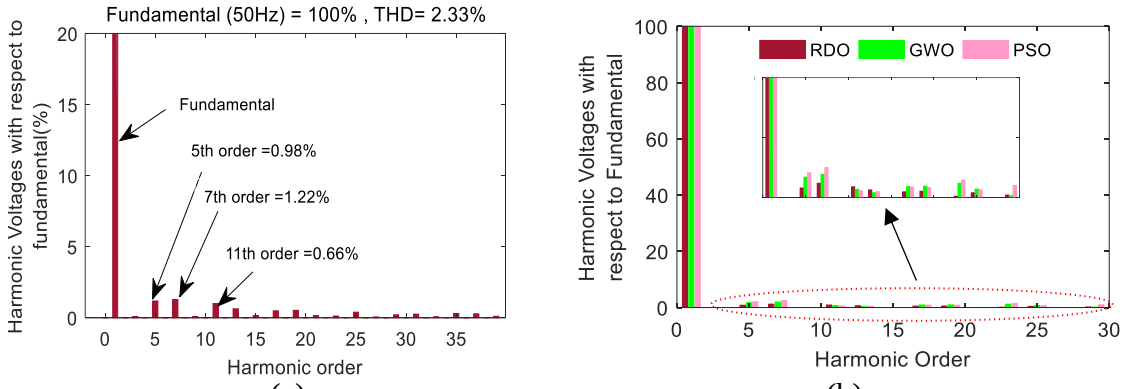


Figure 5.10. (a) FFT analysis of line voltage using RDO, (b FFT analysis comparison for RDO, GWO and PSO

5.4.1 Comparative study of proposed switching scheme

To prove the efficiency of RDO in the proposed scheme, its performance is compared with two swarm-based algorithms like GWO and PSO. The comparison is done in several aspect to measure the superiority of this new optimize algorithm. The program output has tested in the three-phase model developed through simulation. The comparison analysis of proposed reduced MLI with RDO algorithm has been carried out with some references taken for literature review to verify the productiveness.

Table 5.2. Comparison of Voltage THD with respect to existing topology with their switching scheme

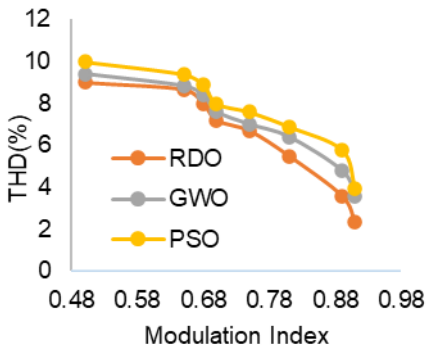
Sl No	Literature	Output Voltage level of MLI	Adopted switching control technique	Voltage THD (%)
1	[5.3]	17	Sigma Delta Modulation	4.05%
2	[5.5]	7	ANFIS	9.17%

3	[5.6]	21	Fundamental sine quantized technique	3.67%
6	[5.9]	13	Fundamental switching frequency Modulation	6.60%
7	[5.11]	11	PSO	5.42%
8	[5.14]	7	Modified PSO	11.55%
9	[5.15]	11	Modified GWO	5.53%
4	[5.21]	19	PWM technique	2.08%
5	[5.22]	29	NLC Modulation	4.14%
10	Proposed	11	RDO	2.33%

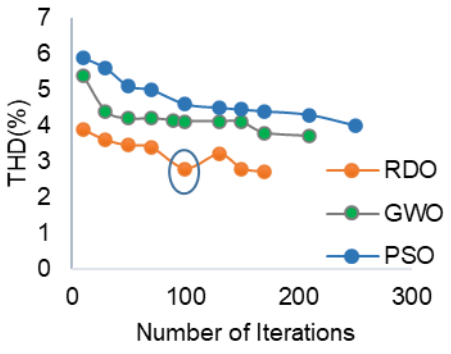
This above table describes the proficiency of proposed reduced MLI using RDO algorithm over the other existing topology with their switching scheme.

For getting the fair comparison, minimum THD for each algorithm is determined with a modulation index of 0.91. The relation of Total Harmonics Distortion with corresponding modulation index is presented below and the fractional value of capacitance with different value of modulation indices are determined which represented graphically. The modulation index is formulated as:

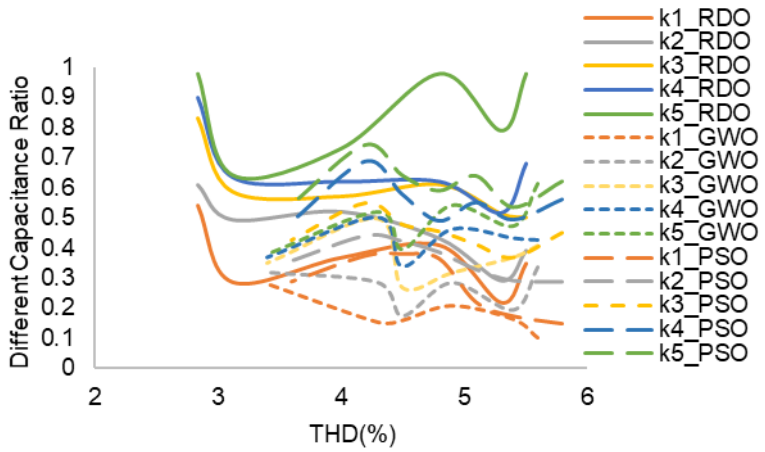
$$MI = \frac{V_1}{V_{max}} = \frac{Fundamental\ Voltage}{Maximum\ Voltage} \tag{5.16}$$



(a)



(b)



(c)

Figure 5.11. (a) Voltage THD resulted from RDO, GWO and PSO with different Modulation Index. (b) Graphical representation of THD with Number of Iteration using Modified RDO, GWO and PSO (c) Capacitance Fractions set for different voltage THD resulted from RDO, GWO, PSO

From figure 5.11(b) It is detectable that RDO requires less iteration count to converge the goal in comparison to GWO and PSO. From FFT analysis graph it is observed that the lower order and higher order harmonics voltages are suppressed effectively with the help of modified RDO and the comparison is also demonstrated for GWO and PSO algorithm.

5.4.2 Power loss calculation of proposed MLI

The efficiency of this proposed MLI is demonstrated by calculating the power loss which has compared with conventional CHBMLI of same level. The above reduced MLI has simulated for single phase 11-level with RL load to calculate the losses. The losses of any switching device are categorized in to conduction loss and switching loss which is discussed in chapter 2 and 4 precisely. By using the loss calculation formulae, total loss of the reduced MLI is found to 1.501w and for CHBMLI it is found to 3.012w. The converter efficiency of the reduced MLI is calculated to 95% with 9 switching devices whereas for CHBMLI it is 90% with 20 switching devices.

5.4.3 Control scheme for the proposed model

To achieve better transient response across grid side after synchronization with PV cell through reduced MLI, online control of switching angles has been done by implementing piecewise mix model equations. This control technique needs linear and nonlinear set of equations which has been calculated offline using RDO and stored in the processor memory for online operation.

In this scheme the variation of triggering angles with different modulation indices has shown in figure 5.12. From this graph the set of linear and nonlinear equations of triggering angle as a function of modulation index 'MI' has developed for storing purpose.

The equations are: for 0.61≤MI≤0.81

$$\left.\begin{aligned}\alpha_1 &= 4.2347MI + 5.6036\\ \alpha_2 &= -76.54MI + 73.423\\ \alpha_3 &= -100.6MI + 102.48\\ \alpha_4 &= -126.03MI + 129.93\\ \alpha_5 &= -100.88MI + 136.73\end{aligned}\right] \quad (5.17)$$

for 0.81≤MI≤0.92

$$\left.\begin{aligned}\alpha_1 &= 6203.3MI^2 - 1130.1MI + 5150.4\\ \alpha_2 &= -1716.7MI^2 + 3084.7MI - 1378.7\\ \alpha_3 &= -13877MI^2 - 25775MI + 11521\\ \alpha_4 &= -17022MI^2 + 30963MI - 14056\\ \alpha_5 &= 6655MI^2 - 12348MI + 5765.5\end{aligned}\right] \quad (5.18)$$

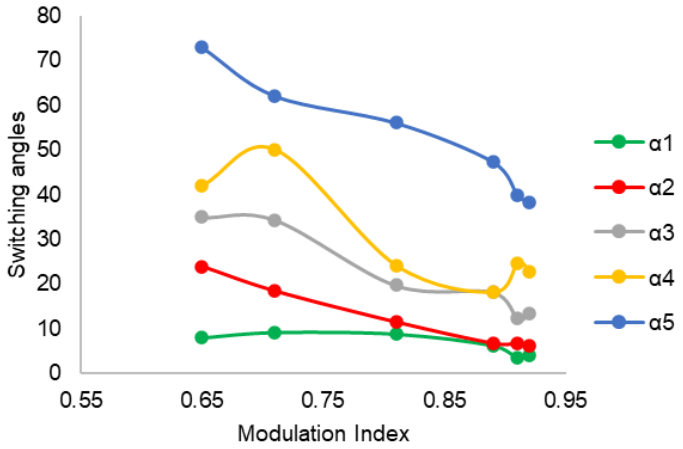


Figure 5.12. Switching angles at different modulation index derived from modified RDO

As presented in figure 5.1(b), the grid voltage is compared with the reference output voltage and the error is processed via PI controller. The output of PI controller is treated as modulation index and for different value of modulation indices the set of triggering angles in form of equations are stored in processor memory, which drive the reduced MLI through driver circuits.

5.5 EXPERIMENTAL OUTCOMES

The effectiveness of the proposed MLI is verified through a hardware design of 11-level reduced MLI with RL load, which is powered by a single PV panel of 260 watts for each phase. The MLI is designed with 9 IGBTs (FGA25N120) and 4 power diodes. The component details are given in Table 5.3. The gate pulses are stored in microcontroller 18F452 and flashed through PICKIT3 which are driven by TLP250H driver circuit with 50Hz frequency to operate the MLI. The line voltage, phase voltage, load current waveforms and harmonic contents in the output voltage is recorded with the help of DSO model no-TDS 2022B. The PV boost voltage waveform and the series capacitors voltages are shown in figure 5.13. The experimental outputs and voltage harmonic spectrum with different modulation indices and different loading are cited in figure 5.14.

Table 5.3. Component List

SI NO	**Components**	
1	PV panels	260W, 24V
2	Series Capacitors	1200µF,1500 µF,1800 µF,2000 µF,2200 µF
Boost Converter		
2	Series inductor	1.371mH
3	Input capacitance	10µF

4	output capacitance	83.583µF
5	Switching Frequency	25kHz
Inverter		
6	IGBT (9)	FGA25N120
7	Load	R=200Ω, L=20mH
8	Switching Frequency	50Hz
Driver Circuit		
8	Optocoupler	TLP250H
9	Microcontroller	PIC18f452

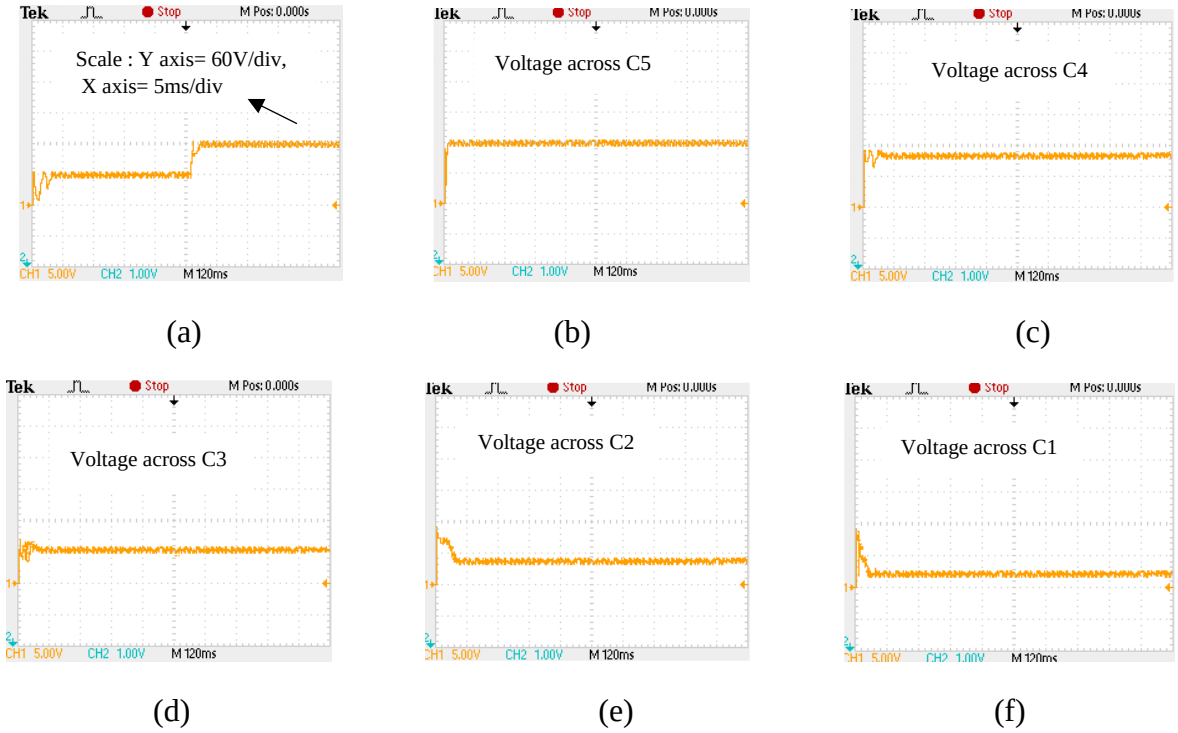
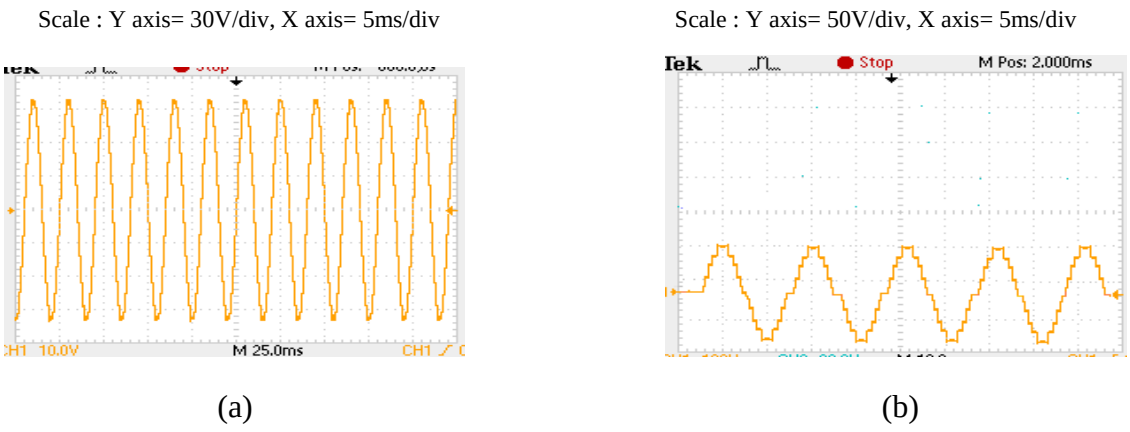


Figure 5.13. DC input voltages (a) PV Boost voltage, (b), (c), (d), (e) and (f) are the series capacitor voltages



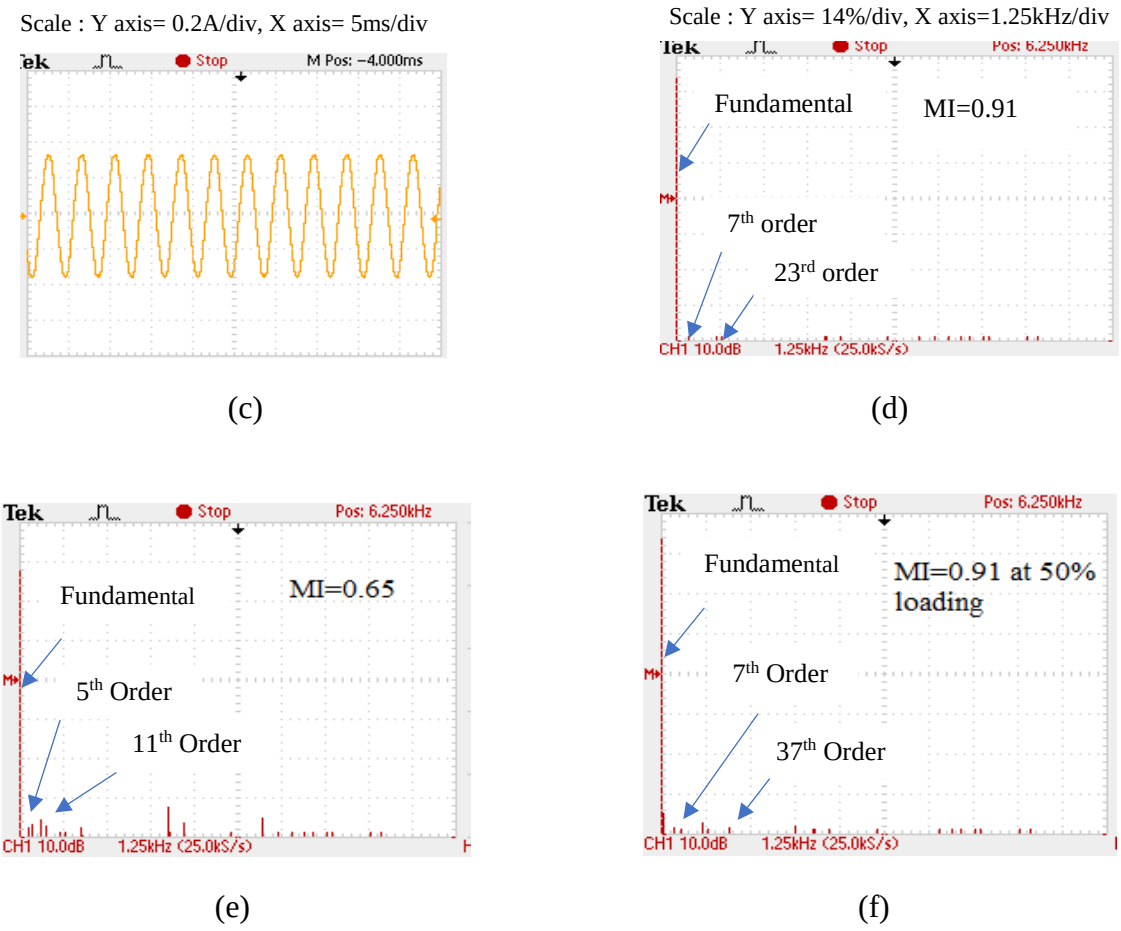


Figure 5.14. (a) Line voltage waveform (Vab), (b) Phase Voltage waveform, (c) Load current waveform, (d) Harmonic voltages spectrum of line voltage

The picture of experimental setup is shown in figure 5.15.

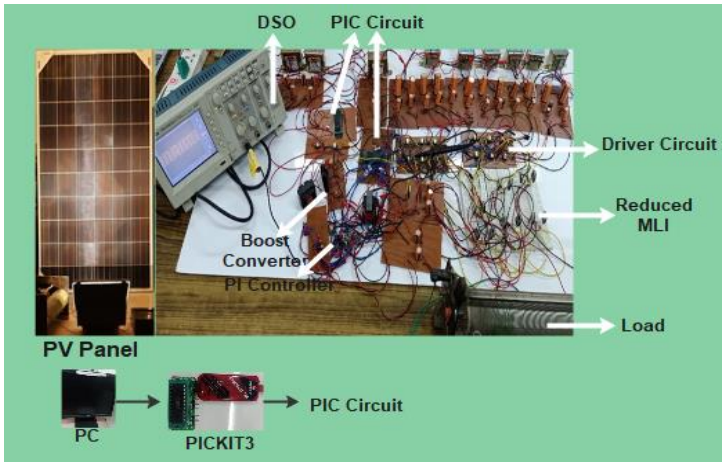


Figure 5.15. Experimental Setup for the proposed MLI energized with PV input

5.6 OBSERVATION

In this chapter a single source-based capacitor charged reduced topology of MLI has been demonstrated for a low voltage grid. The reduced MLI has efficiently converted the PV energy with minimum output voltage THD. The output voltage THD has been reduced at grid side through online control by piecewise mixed model equations. Implementation of RDO algorithm with some modification enables to converge the objective function faster with less complication compared to other population-based algorithms. The simulation and experimental observations justify the motive behind origination of the scheme. This can be applicable for medium or high voltage system with enhanced power quality using solar array.

5.7 PUBLICATION

[1] R. Mohanty, D. Chatterjee, S. Suman, "Red Deer Optimization based Asymmetrical Reduced Switch MLI with Low Switching Loss and Minimum Voltage Harmonics," International journal of Power Electronics, Inderscience. DOI:10. 1504/IJPELEC.2024.10056817.

5.8 REFERENCES

[5.1] Fahad M. Alhuwaishe et.al., A Medium-Voltage DC-Collection Grid for Large-Scale PV Power Plants with Interleaved Modular Multilevel Converter, *IEEE Journal of Emerging and Selected Topics in Power Electronics*. 8 (2020) 3434-3443.

[5.2] A. Vinayagam et.al., Harmonics assessment and mitigation in a photovoltaic integrated network, *Journal of Sustainable Energy, Grids and Networks*. 20 (2019) 100264.

[5.3] Tefan M. Goetz et al., Concept of a distributed photovoltaic multilevel inverter with cascaded double H-bridge topology, *International Journal of Electrical Power & Energy Systems*. 110 (2019) 667-678.

[5.4] T.R. Sumithira and A. Nirmal Kumar, Elimination of Harmonics in Multilevel Inverters Connected to Solar Photovoltaic Systems Using ANFIS: An Experimental Case Study, *Journal of Applied Research and Technology*. 11 (2013) 124-132.

[5.5] G. Nageswara Rao, P. Sangameswara Raju, K. Chandra Sekhar, Harmonic elimination of cascaded H-bridge multilevel inverter based active power filter controlled by intelligent techniques, *International Journal of Electrical Power & Energy Systems*. 61 (2014) 56-63.

[5.6] P. K Kar, A. Priyadarshi, S.B Karanki, Development of an enhanced multilevel converter using an efficient fundamental switching technique, *International Journal of Electrical Power & Energy Systems*. 119 (2020) 105960.

[5.7] S. R. Raman et. al., Family of Multiport Switched-Capacitor Multilevel Inverters for High-Frequency AC Power Distribution, *IEEE Transactions on Power Electronics*. 34 (2019) 4407-4422.

[5.8] E. Samadaei, M. Kaviani and K. Bertilsson, A 13-Levels Module (K-Type) With Two DC Sources for Multilevel Inverters, *IEEE Transactions on Industrial Electronics.* 66 (2019) 5186-5196.

[5.9] Y. Naderi et.al., An optimized direct control method applied to multilevel inverter for microgrid power quality enhancement, *International Journal of Electrical Power & Energy Systems*. 127 (2019) 496-506.

[5.10] H. Taghizadeh and M. Tarafdar Hagh, Harmonic Elimination of Cascade Multilevel Inverters with Nonequal DC Sources Using Particle Swarm Optimization, *IEEE Transactions on Industrial Electronics*. 57 (2010) 3678-3684.

[5.11] R.N. Ray, D. Chatterjee and S.K. Goswami, Harmonics elimination in a multilevel inverter using the particle swarm optimization technique, *IET Power Electron*. 9 (2009) 646-652.

[5.12] M. Tarafdar Hagh, H. Taghizadeh and K. Razi, Harmonic Minimization in Multilevel Inverters Using Modified Species-Based Particle Swarm Optimization, *IEEE Transactions on Power Electronics*. 24 (2009) 2259-2267.

[5.13] K.P. Panda and G. Panda, Application of swarm optimization-based modified algorithm for selective harmonic elimination in reduced switch count multilevel inverter, *IET Power Electronics*. 11 (2018) 1472-1482.

[5.14] S. Mohanty, B. Subudhi and P. K. Ray, A New MPPT Design Using Grey Wolf Optimization Technique for Photovoltaic System Under Partial Shading Conditions, *IEEE Trans. Sustainable Energy*. 7 (2016) 181-188.

[5.15] A. Routray, R. K. Singh and R. Mahanty, Harmonic Reduction in Hybrid Cascaded Multilevel Inverter Using Modified Grey Wolf Optimization, *IEEE Trans. Industry Applications*. 56 (2020) 1827-1838.

[5.16] K. K. Gupta et.al., Multilevel Inverter Topologies with Reduced Device Count: A Review, *IEEE Transactions on Power Electronics.* 31 (2016)135-151.

[5.17] N. Prabaharan & K. Palanisamy, Comparative analysis of symmetric and asymmetric reduced switch MLI topologies using unipolar pulse width modulation strategies, *IET Power Electronics*. 9 (2016) 2808-2823.

[5.18] K. Yang, X. Lan, Q. Zhang and X. Tang, Unified Selective Harmonic Elimination for Cascaded H-Bridge Asymmetric Multilevel Inverter, *IEEE Journal of Emerging and Selected Topics in Power Electronics*. 6 (2018) 2138-2146.

[5.19] A.M. Fathollahi-Fard, M. Hajiaghaei-Keshteli and R. Tavakkoli-Moghaddam, Red deer algorithm (RDA): a new nature-inspired meta-heuristic, *Journal of Soft Computing by Springer*. 24 (2020)14637-14665.

[5.20] D. Chatterjee, A Novel Magnetic-curve Identification and Computer Storage Technique for Induction Machines Suitable for Online Application, *IEEE Trans. Ind. Electron*. 58 (2011) 5336-5343.

[5.21] Ahmed Ismail M. Ali, Mahmoud A. Sayed and T.Takeshita, Isolated single-phase single-stage DC-AC cascaded transformer-based multilevel inverter for stand-alone and grid-tied applications, *International Journal of Electrical Power and Energy Systems.* 125 (2021) 106534.

[5.22] R. Agrawal, S. Jain, Multilevel inverter for interfacing renewable energy sources with low/medium- and high voltage grids, *IET Renewable Power Generation*. 11 (2017) 1822-1831.

Chapter-6

GRID INTERACTIVE ASYMMETRICAL CASCADED MLI with MINIMUM VOLTAGE DISTORTION

This Chapter presents a grid connected asymmetrical cascaded Multilevel Inverter with minimum voltage distortion. The optimum switching angles of the MLI is found out using an efficient search based algorithm, known as Honey Badger Optimization Algorithm. The control scheme for getting minimum distortion during grid interconnection is presented here. Statistical significance of the proposed algorithm with existing nature-based algorithm is also presented.

GRID INTERACTIVE ASYMMETRICAL CASCADED MLI with MINIMUM VOLTAGE DISTORTION

6.1 INTRODUCTION

The development of power electronic devices and converter applications makes the system for power conversion in several fields more compact and efficient. The development of Multilevel Inverter is motivated by the desire to convert AC power from DC sources without filter circuits. Due to its modular construction, dependability, and capacity to operate under defective situations, cascaded MLI is the most ideal topology for industrial applications or grid integration [6.1],[6.2]. In contrast, symmetrical DC sources based cascaded MLI requires a greater number of DC sources and switching devices to produce higher output voltage levels. Utilizing unequal DC sources of variable ratios for MLI operation has eliminated the flaw and made the converter economical. [6.3] proposed an asymmetrical binary MLI for shunt active power filter to reduce the unwanted current harmonics with a minimum amount of energy sources. Various switching strategies are used to establish the optimal triggering angles for the MLI in order to produce higher power quality, voltage, and current waveforms with minimal distortion. The application of differential evolution to tackle the harmonic removal issue in cascade MLI employing PWM switching technique has been presented [6.4]. In this literature to eliminate a higher number of harmonics with a seven-level MLI, 18 switching angles must be established, which makes the computation difficult. [6.5] developed an improved PWM approach to minimize the THD of a modular MLI for PV-integrated systems. However, this switching method needs an extra filter circuit in order to lower the THD value below the standard threshold. THD optimization with MLI is also handled using sinusoidal PWM [6.6]and staircase PWM [6.7] to achieve reduced distortion of output voltage. In the previously stated PWM approaches, the switching frequency is in the kHz range, which increases the switching loss of the MLI. The switching loss due to higher frequency has been ignored by implementing different SHE modulation techniques with fundamental frequency to obtain the optimum switching angles for MLI [6.8], [6.9]. Artificial intelligence-based adaptive neuro fuzzy interference system is proposed in [6.10] and fuzzy logic controller for multi carrier phase shifted PWM is proposed in [6.11] in order to achieve minimum THD via voltage variation control and current error

control respectively. In order to achieve the least amount of voltage distortion, the appropriate switching angles are computed using Genetic Algorithm (GA) in the newly established 9-level MLI that has been detailed in [6.12]. The Newton Raphson technique and the GA have been used to resolve the harmonic reduction issue of the cascade H-bridge MLI employing SHEPWM switching control [6.13]. However, this procedure becomes more difficult due to the conversion of the GA optimization process from decimal to binary during crossover. For achieving the appropriate switching angles of cascaded MLI, PSO has been employed in [6.14],[6.15] in order to shorten the computing time of operation. By improving the searching method of traditional PSO and Grey wolf Optimization (GWO) algorithms, better convergence has also been obtained in [6.16], [6.17], and [6.18]. The works of literature have suggested the use of hybrid asynchronous PSO - GA [6.19], generalized pattern search [6.20], and opposition-based quantum bat algorithm [6.21] as optimization methods to remove the undesirable harmonic voltages from the output voltage of cascade H-bridge MLI and to lower the computational cost. To achieve high efficiency and minimal THD, the best design of CHBMLI has been carried out for drives using Pareto optimization [6.22].

This chapter presents the use of a newly developed Honey Badger optimization algorithm (HBA) to produce the minimal voltage distortion of cascaded reduced switch MLI suited for grid connections.

The primary contributions of this research are:

a. Due to the usage of asymmetrical DC sources in the proposed scheme, the required number of switching devices are greatly reduced for generation of same output voltage level compared to the existing MLI topologies.

b. The optimum switching angles are obtained using HBA to obtain lowest possible voltage THD compared to existing switching methods.

c. The employment of HBA in the proposed scheme has shown better convergence rate and lower computational time compared to similar bio inspired algorithms.

Competence of HBA has been verified by developing both single phase and three phase model of a 9-level cascaded MLI in MATLAB simulation tool and the results are compared with the literatures that are shown in section 6.4.1. The simulation results are endorsed through a hardware model for off-grid condition and through real time simulator OPALRT-5650 for grid integration in the laboratory which has been discussed in section 6.5.

6.2 PROPOSED SCHEME

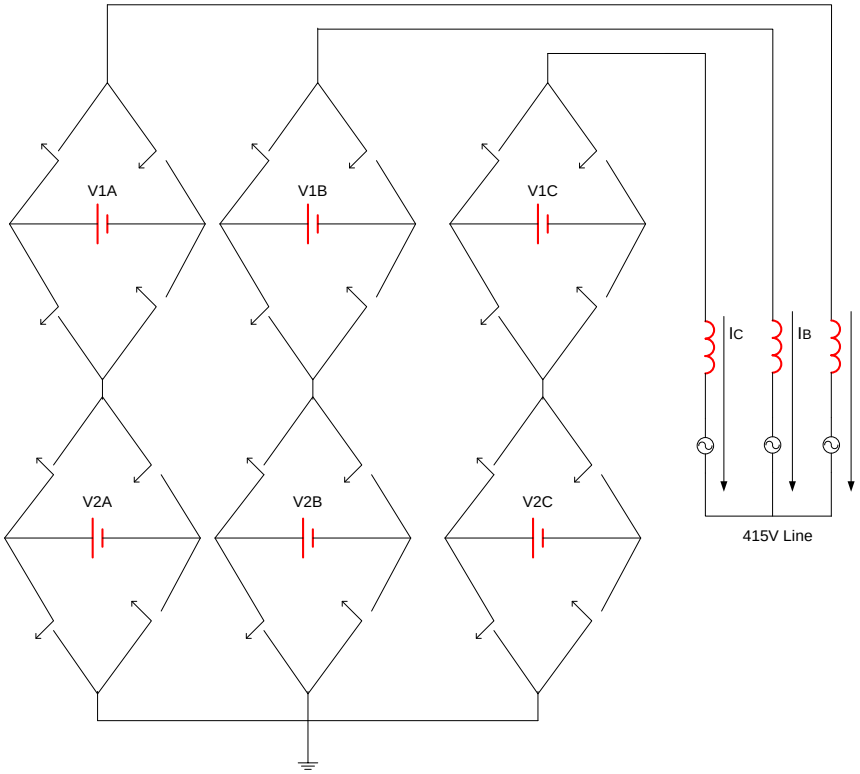


Figure 6.1 Grid integrated asymmetrical cascaded MLI

In this research the MLI with minimum number of voltage sources and switching devices is efficiently integrated with grid using HBA optimization technique. The HBA algorithm uses an efficient search approach that avoids confinement in the local region, resulting in faster convergence. The asymmetrical 9-level cascaded MLI integrating with 415volts grid is shown in the above figure. The feature and single-phase structure of a 9-level cascaded MLI has been discussed in the next section.

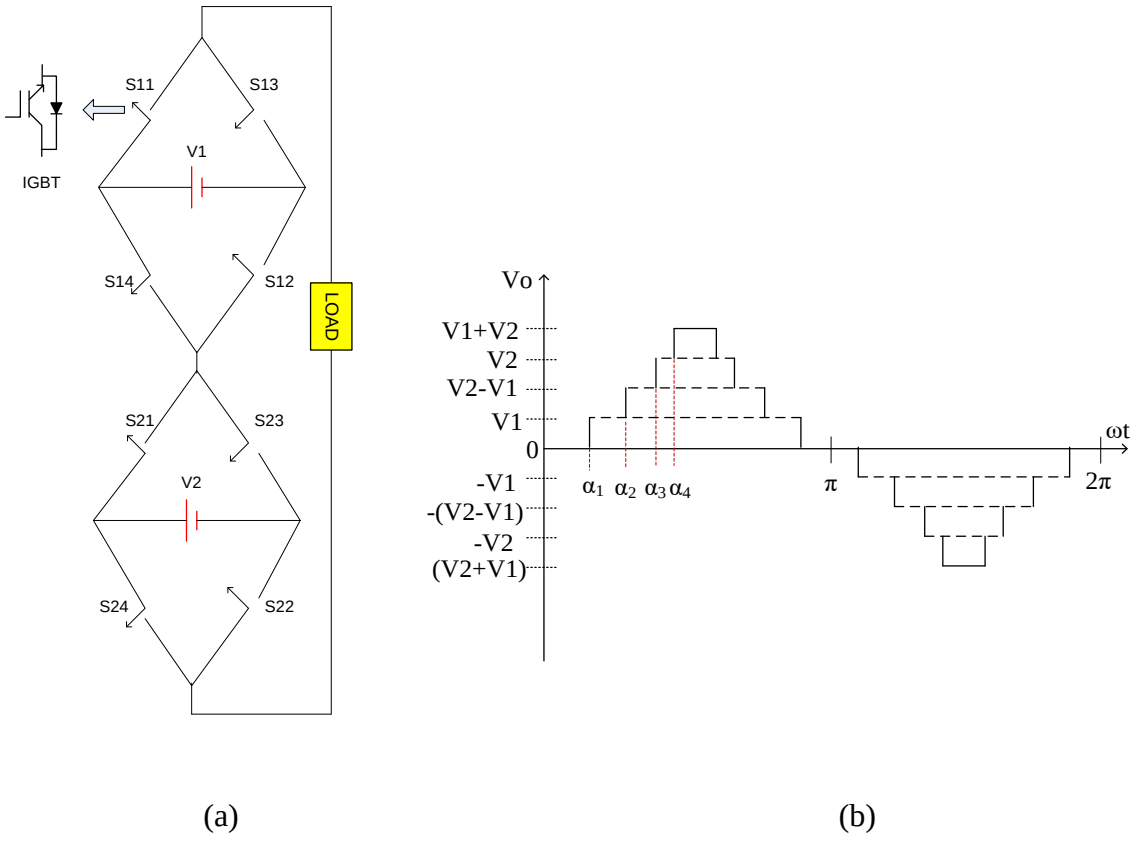
6.2.1 Asymmetrical Cascaded MLI

Cascaded MLI with unequal DC sources can develop higher output voltage level in comparison to an equal one with same number of power devices. The maximum output voltage level for cascaded MLI can be developed using 'N' number of asymmetrical DC sources is given by,

$$V_{lmax} = 3^N \tag{6.1}$$

In this research, a 9-level cascaded MLI is developed with two DC sources of voltage ratio 1:3 and eight power switches and the topology is shown in figure 6.2 (a). The output voltage waveform with different levels of voltage is shown in figure 6.2(b). The maximum output voltage of MLI is determined by equation (6.2).

$$V1 + V2 = 4V_D \tag{6.2}$$



(a) (b)

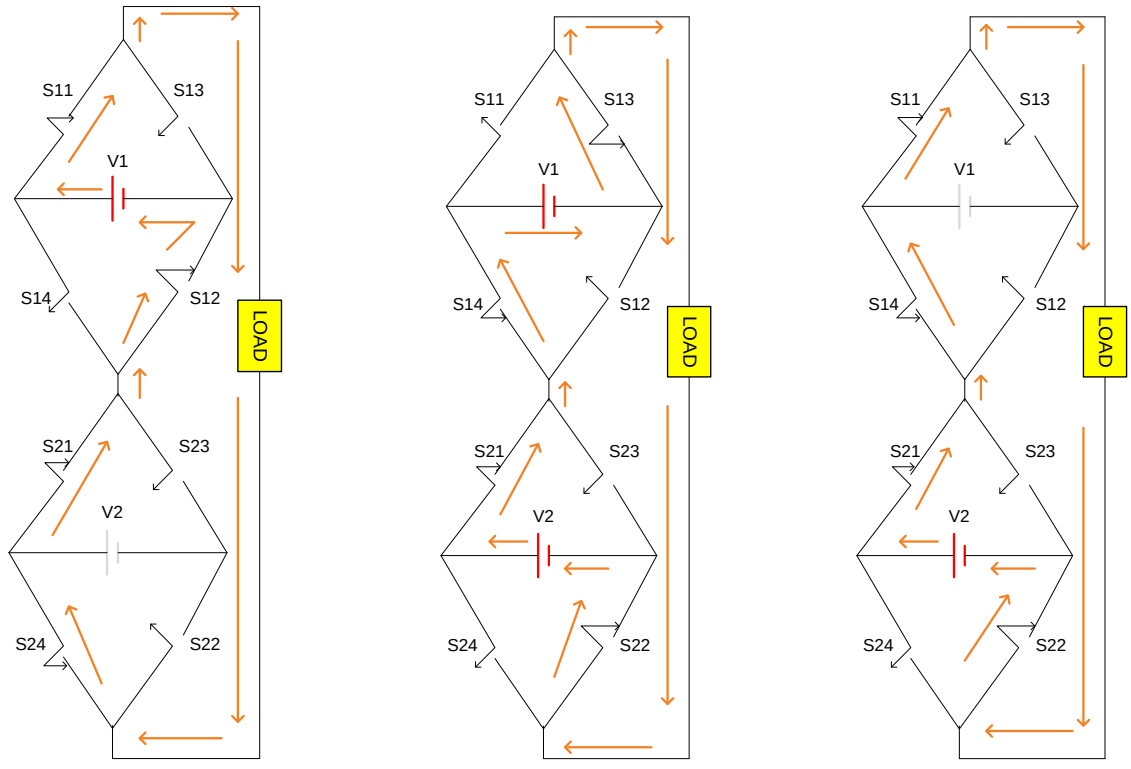
Figure 6.2. 9-level Asymmetrical MLI (a) Single phase circuit diagram, (b) Output Voltage waveform

The operation of power switches for generating 9-level output voltage is shown in Table 6.1.

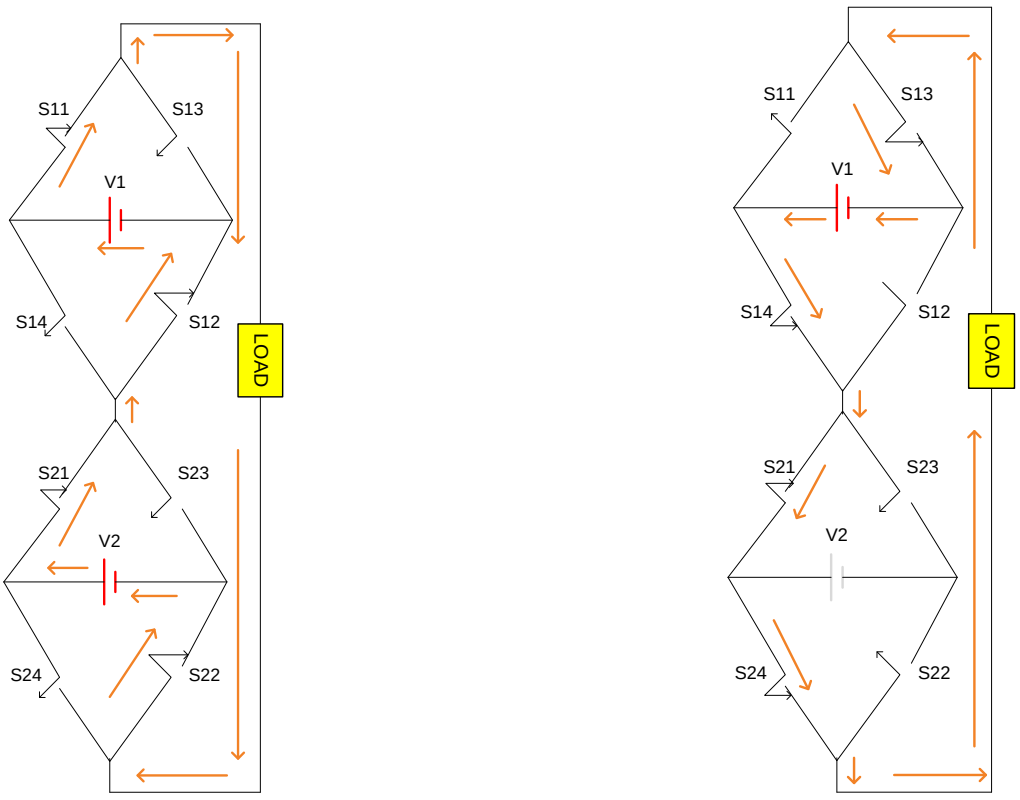
Table 6.1. Switching Scheme of 9-level MLI

Switching pattern for 9-level MLI(Asymmetrical)								
Switches	V1	V2-V1	V2	V2+V1	(-V1)	-(V2-V1)	-(V2)	-(V2+V1)
S11	1	0	1	1	0	1	1	0
S12	1	0	0	1	0	1	0	0
S13	0	1	0	0	1	0	0	1
S14	0	1	1	0	1	0	1	1
S21	1	1	1	1	1	0	0	0
S22	0	1	1	1	0	0	0	0
S23	0	0	0	0	0	1	1	1
S24	1	0	0	0	1	1	1	1

In the above table, switch on for the device is denoted by state '1', and switch off for the device is denoted by state '0' for each voltage level. The operation of 9-level MLI is explained in four different modes, which is shown in figure 6.3.



(a) (b) (c)



(d) (e)

Figure 6.3 Operational diagram of single phase MLI. (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 1 operation of negative half cycle

Figure 6.3 (a) describes mode 1 operation of the MLI. As per the switching states of 9 power devices shown in Table 6.1, to generate $V1=V_D$ voltage across output, S11, S24, S21 and S12 circulates the current in the circuit. In mode 2, $V2-V1=2V_D$ voltage appears across the output and the circuit operation is explained by figure 6.3 (b). Figure 6.3 (c) describes mode 3 operation to develop $V2=3V_D$ voltage across output. The maximum output voltage, $V1+V2=4V_D$ is developed across output in mode 4 and the circuit operation is cited in figure 6.3(d). In the same way the four different modes of operation are carried out for negative half cycle by following the switching pattern of Table 6.1. Mode 1 operation of negative half cycle is explained by figure 6.3(e). Here in each mode four power switches are turned on and rest four switches are remained off.

6.2.2 Control Scheme

The optimum switching angles obtained from HBA have reduced the distortion of MLI output voltage. To achieve the minimum voltage distortion at grid side after integrating with

MLI voltage, the simultaneous voltage and frequency control technique has been adopted in this research. The block diagram of the control technique is shown in figure 6.4. The grid voltage frequency is compared with the fundamental frequency and the error is fed to the set of angles developed by HBA. The magnitude of grid voltage is controlled by the outer loop and the error is processed through PI controller. Output of the PI controller is treated as the modulation index. Switching angles set for different modulation index are calculated offline and provided through a lookup table for online applications.

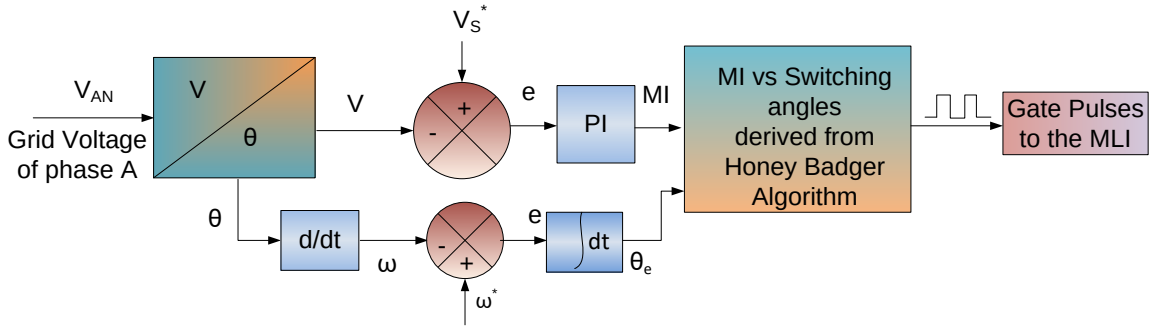


Figure 6.4. Control scheme for grid connected MLI

6.2.3 Mathematical Modelling

In section 6.2, it has been discussed that to generate 9-level output voltage the two input DC voltages exhibit the following relationship.

$$V1:V2 = 1:3 \tag{6.3}$$

As discussed in the previous chapters, the voltage waveform of MLI is quarter wave symmetry in nature. The expression of output voltage waveform using Fourier series analysis is determined by,

$$V(\omega t) = \sum_{\alpha=1}^{ai} \frac{4V_D}{n\pi} (\cos(n\alpha_1) + \cos(n\alpha_2) + \cdots + \cos(n\alpha_{ai}))\sin(\omega t) \tag{6.4}$$

For developing 9-level output voltage '*ai*' is taken as 4 which describes the switching angles for MLI. The output voltage THD is expressed in equation (6.5).

$$THD = \frac{\sqrt{\sum_{n=3,5,\ldots}^{21} V_n^2}}{V_1} \tag{6.5}$$

In this chapter, the lower and higher order harmonic voltages are suppressed with the optimum switching angles derived from HBA and these angles are perceived using equations (6.4) and (6.5). The lower limit and upper limit set for the switching angles are 0 and π/2 respectively.

6.3 HONEY BADGER OPTIMIZATION ALGORITHM

By Fatma A. Hashim et al. in 2021, the Honey Badger Algorithm is proposed. This algorithm's performance is influenced by how honey badger graze. The honey badger, a mammal native to Africa, Southwest Asia, and the Indian subcontinent, lives in semi-deserts and rainforests. The researcher's technique for solving the difficult optimisation problem mentioned in [6.23] was inspired by the honey badger's daring and astute foraging habit. There are multiple steps in the algorithm that lead to convergence of the objective function. These include setting an initial population size, determining smell intensity, updating the density factor, avoiding getting stuck in local optima, and setting an initial population location. The honey badger's rate of movement in the direction of its prey is determined by the strength of the odours it detects. Figure 6.5 and equation (6.6) are used to use the inverse square law to calculate the smell intensity, which focuses on the idea that increased distance from the source decreases the intensity.

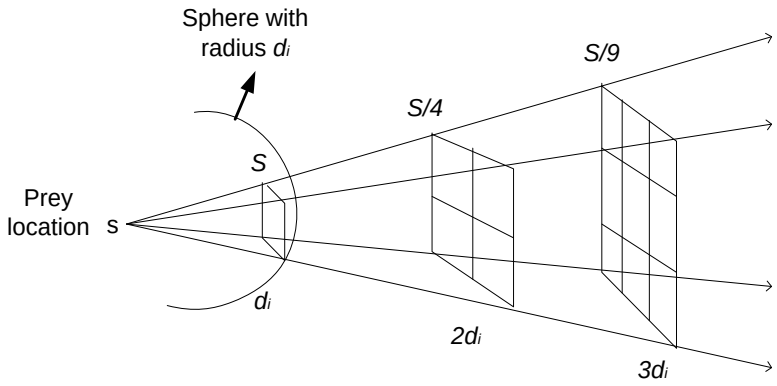


Figure 6.5 Determination of smell intensity by Inverse square law

$$S_i = r_1 * \frac{s}{4\pi d_i^2} \tag{6.6}$$

's' is the concentration strength of the honey badger and it is expressed by,

$$s = (p_i - p_{i+1})^2 \tag{6.7}$$

d_i can be determined with the help of equation (6.8).

$$d_i = p_{prey} - p_i \tag{6.8}$$

The density factor controls transition of exploration to exploitation smoothly. This factor depends on the constant 'C' and number of iterations. Density factor is updated using the following equation.

$$D_f = C * exp\left(\frac{-itr}{itr_m}\right) \tag{6.9}$$

Where $C \geq 1$; it has been set to 2 in the literature to attain the optimum fitness value.

The honey badger position is updated in two ways after getting the global best position (location of prey). The position is first updated in digging phase which depends on the smell intensity of honey badger to get the location of prey. The honey badger reaches to the prey location by cardioid motion as shown in figure 6.6. Therefore, the honey badger position is updated by following the equation of cardioid motion which has derived in equation (6.10).

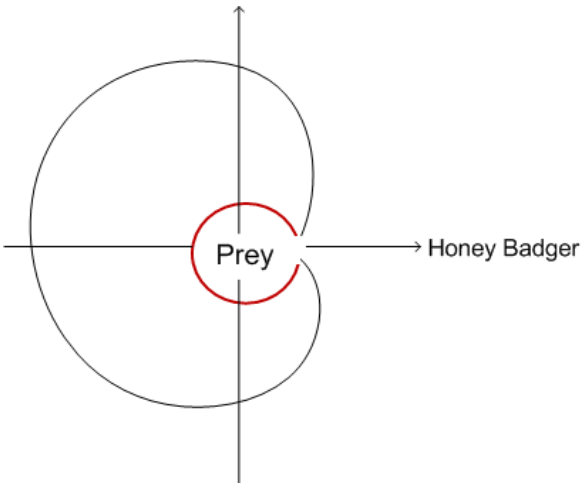


Figure 6.6 Cardioid motion of honey badger

$$p_{new} = p_{prey} + \left(Fl * B * S_i * p_{prey}\right) + \left(Fl * r_2 * D_f * d_i\right) * |\cos(2\pi r_3) * [1 - \cos(2\pi r_4]| \quad (6.10)$$

p_{new} is the new position of the population. p_{prey} is the best position of prey that searched yet. $B \geq 1$, it is the random number which is treated as the potential of honey badger to get food and in literature [6.23] it is set to 7 for achieving better result. *'Fl'* is treated as a flag that changes the search direction alternatively. *Fl* is taken as 1, if $r_5 \leq 5$ else *F* is taken as -1. Second phase is known as honey phase, where the honey badger follows honey guide to reach the beehive. In this phase the population is updated by the following equation.

$$p_{new} = p_{prey} + (F * r_6 * D_f * d_i) \quad (6.11)$$

d_i and D_f are determined from equations (6.8) and (6.9) respectively.

The switching angles of the MLI are treated as the population which are randomly initialized between 0 to π/2. In this chapter the position vector for the x^{th} particle is expressed in y dimension space.

$\alpha_x = [\alpha_{x1}, \alpha_{x2}, \ldots\ldots \alpha_{xy}]$. Where, y=4 for 9-level MLI.

6.3.1 Implementation of HBA for optimizing voltage THD of cascaded MLI

In order to achieve the minimum output voltage THD of MLI, the desired switching angles are determined using the flowchart shown in figure 6.7. The fitness function (percentage of THD) can be determined as:

$$F = \frac{\sqrt{\sum_{n=3,5,\ldots}^{21} V_n^2}}{V_1} * 100 \qquad (6.12)$$

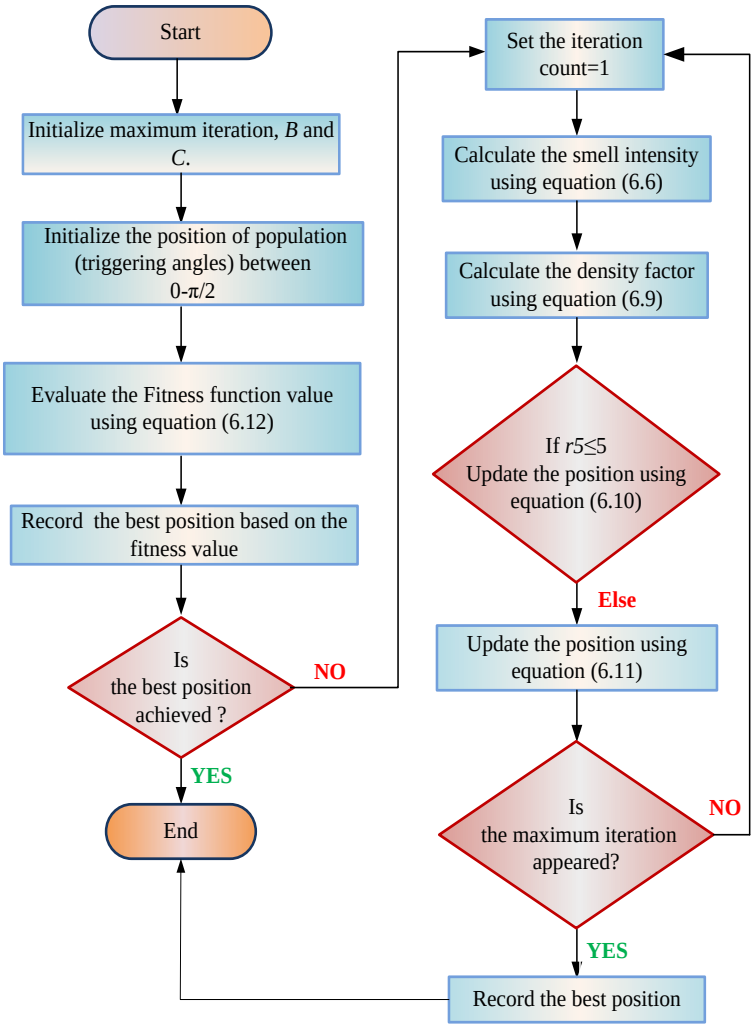
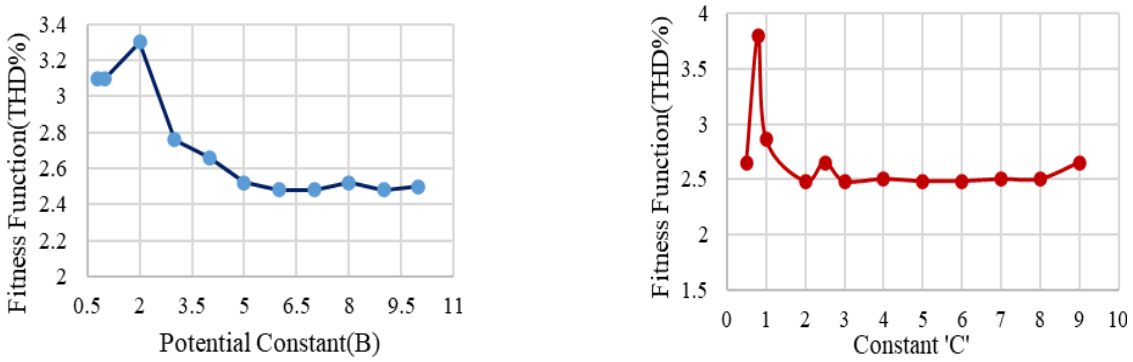


Figure 6.7. Description of Honey Badger Optimization



(a) (b)

Figure 6.8. Plot of HBA constants (a) THD vs potential constant, (b) THD vs constant 'C'

From figure 6.8 (a), it can be observed that the minimized THD is achieved between *B*=6 to *B*=7. So, for solving this problem B can be taken between 6 and 7. Also from figure 6.8(b) it is seen that for THD minimization of MLI, "*C*' can be taken in the range of 4 to 6. The parameter '*B'* of HBA algorithm depends on maximum iteration count. Threshold value for fitness function(%THD) is set to 5% for solving the problem and it has been verified that the fitness function does not exceed the threshold limit which has discussed in the next section. This proves the efficiency of the algorithm towards solving the THD minimization problem.

6.4 RESULTS AND DISCUSSION

The 9-level cascaded MLI with two unequal DC sources and eight switching devices is simulated using MATLAB Simulink tool. The optimized switching angles are derived using HBA to obtain the minimum THD of output voltage for different modulation indices. The minimum voltage THD achieved for single phase and three phase 9-level MLI with the optimum angles are given in Table 6.2. The FFT analysis of three phase line voltage is done to observe the supressed nth order harmonic voltages before grid synchronization. The line voltage waveform, load current waveform for a load of 500Ω and 10mH in series, FFT analysis of line voltage for 9-level MLI at a modulation index of 0.92 and variation of harmonic voltages for different modulation indices are shown in figure 6.9. The MLI is integrated to a 415V grid to verify the effect on power quality due to proposed switching algorithm through real time simulator using OPALRT-5650 embedded with the PC. The grid voltage waveform and corresponding THD after synchronizing with MLI has been shown in figure 6.10.

Table 6.2. Minimum THD with optimum switching angles for 9-level MLI

Switching Angles (In degree)					
	α_1	α_2	α_3	α_4	O/P voltage THD
Single Phase	6.22	23.4	37.2	58.02	5%
Three Phase	4.03	12.2	20.329	33.6	2.48%

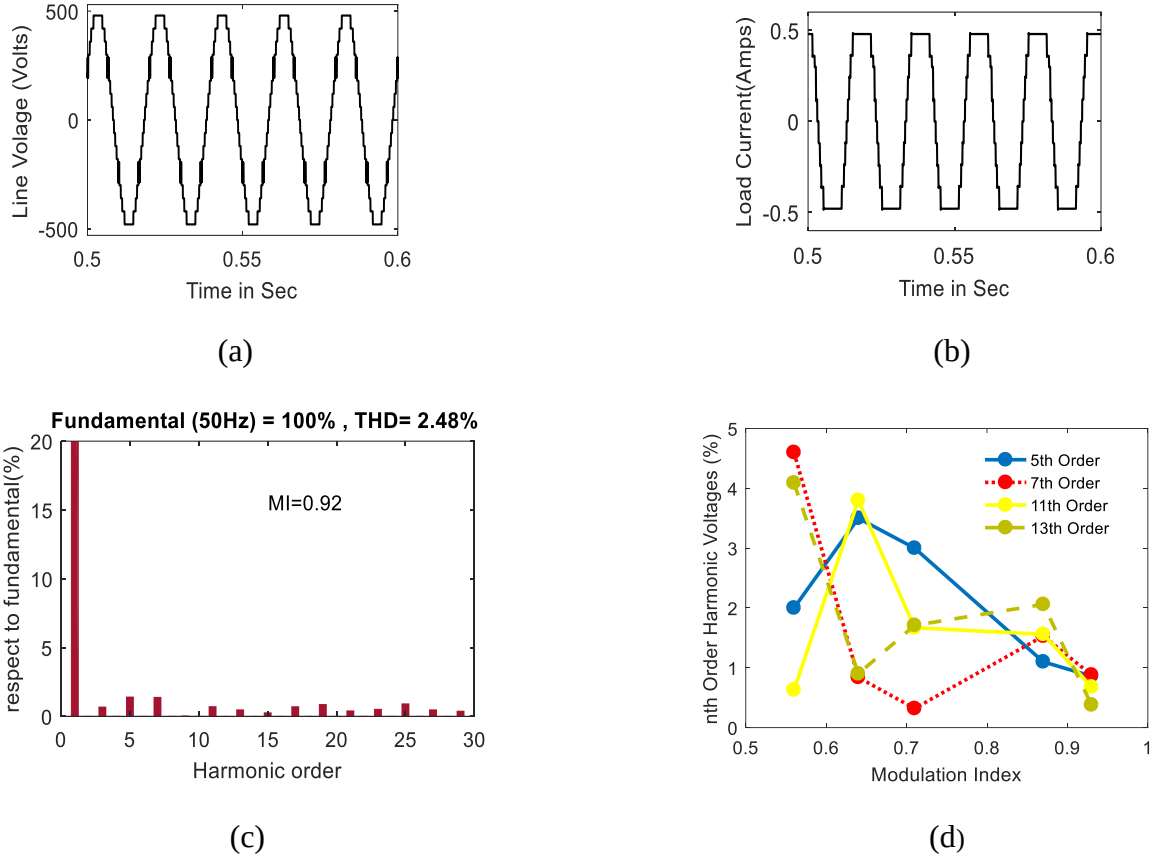


Figure 6. 9. MLI output results before grid synchronization (a) Line voltage vs Time, (b) Load current vs Time, (c) FFT analysis of line voltage, (d) Harmonic voltages vs Modulation index

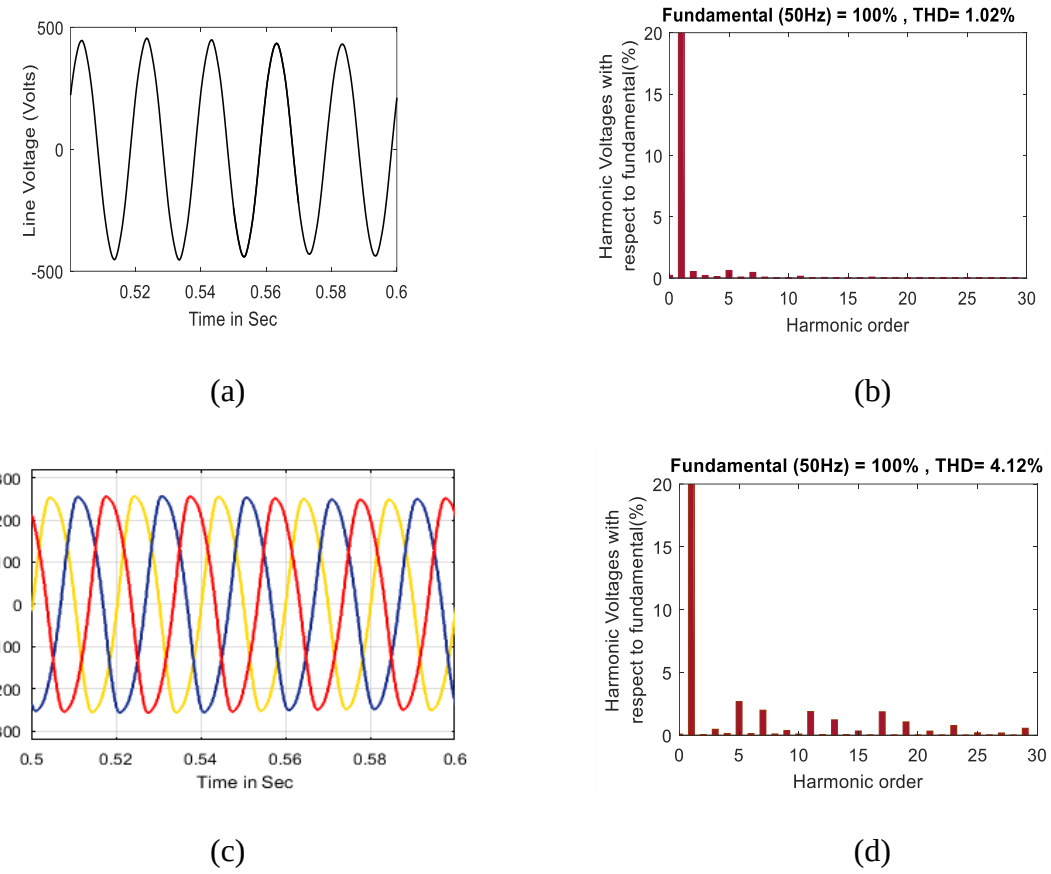


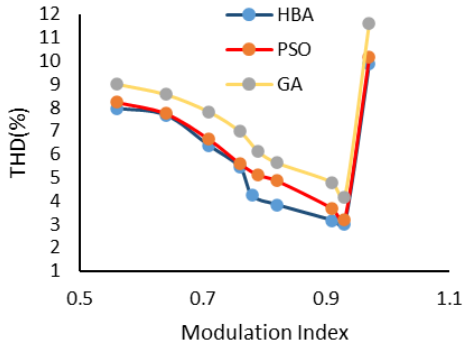
Figure 6.10. Grid parameters (a) Grid Voltage vs Time (V_{AB}), (b) FFT analysis of V_{AB}, (c) Grid Voltages (phase to neutral), (d) FFT analysis of grid phase voltage

6.4.1 Comparative study

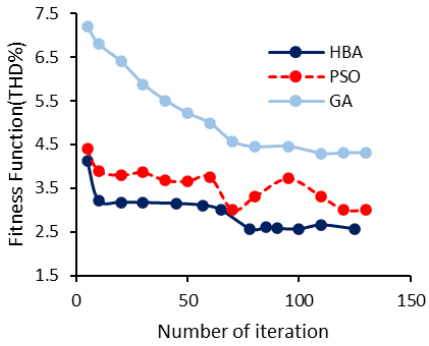
Through MATLAB programme and simulation, the effectiveness of HBA and its superiority over alternative optimization algorithms are demonstrated. For harmonic minimization using similar types of inverters, the PSO and GA algorithms are found in most literatures [6.12-6.16]. In order to justify the suggested algorithm, a comparison with PSO and GA is made. The minimum THD achieved at modulation index 0.92 using proposed HBA, PSO, and GA and the n^{th} harmonic voltage value with respect to fundamental for respective algorithms are presented in Table 6.3. From Table 6.3, it is observed that the lowest voltage THD has been achieved by HBA and the harmonic voltages are supressed prominently in comparison to PSO and GA. The performance of HBA is also verified by comparing with other existing switching techniques of MLI and it has been presented in Table 6.6.

Table 6.3. Optimum switching angles and minimum voltage THD achieved using HBA, PSO and GA algorithm

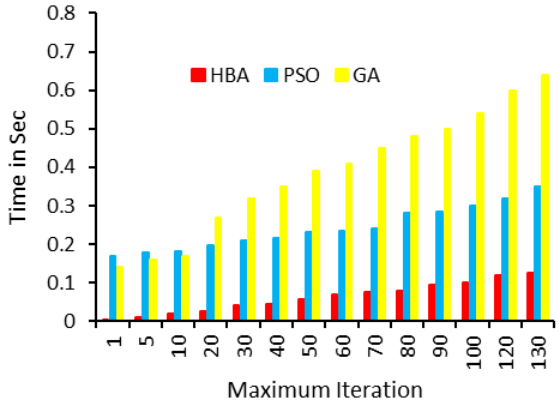
Optimization Algorithms	Switching Angles (in degree)				Operational time	O/P voltage THD	MI	nth order harmonic voltages with respect to fundamental (%)			
	α_1	α_2	α_3	α_4				V5	V7	V11	V13
HBA	4.027	12.21	20.329	33.56	0.07sec	2.48%	0.92	0.86%	0.91%	0.70%	0.46%
PSO	3.94	11.66	20.623	34.44	0.35sec	3.06%	0.92	1.33%	1.01%	0.90%	0.51%
GA	1.66	11.886	20.09	34.966	0.7sec	4.29%	0.92	1.72%	1.06%	1.10%	0.58%



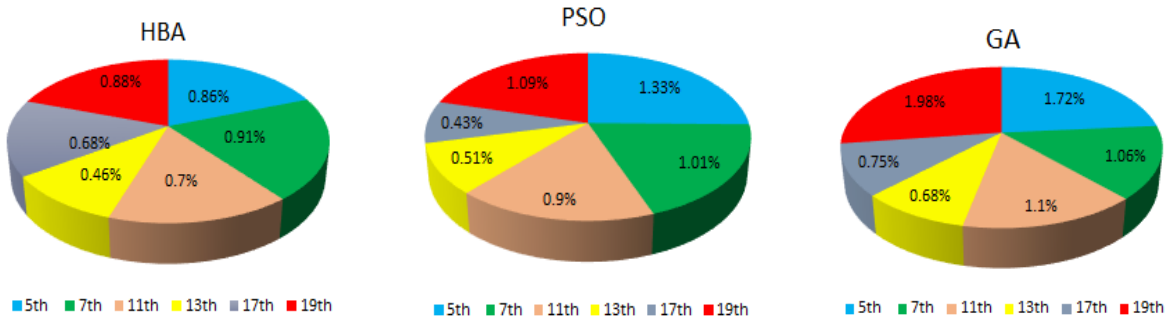
(a)



(b)



(c)



(d)

Figure 6.11. Comparative study of HBA, PSO and GA techniques (a)Output voltage THD vs Modulation index, (b) Fitness function vs Number of iteration, (c) Computational time with respect to set maximum iteration, (d) nth order harmonics present in the output voltage

The output voltage THD obtained at different modulation indices using three above discussed algorithms is presented in figure 6.11(a) and from this figure, it is shown that HBA has resulted the lowest THD at each modulation index in comparison to PSO and GA. To determine the rapid convergence rate, the fitness value is recorded for different set maximum iteration using HBA, PSO and GA, which is presented in figure 6.11(b). From this figure, it is validated that the minimum THD (fitness value) has been achieved with minimum iteration count for HBA. Figure 6.11(c) presents the computational time at each set maximum iteration for obtaining the optimal switching angles. From this figure it verifies that HBA requires minimum time of operation for solving the THD minimization problem than PSO and GA. Figure 6.11(d) shows that the lower as well as higher order harmonic voltages are reduced successfully in comparison to PSO and GA. Statistical results of the above algorithms are obtained from the hypothetical test for different iteration count and population size at a constant modulation index of 0.92 which are shown in Table 6.4 and Table 6.5 respectively. The p-values obtained after undertaking t-test between HBA and the remaining competitor algorithms are reported in Table 6.4 and Table 6.5. It is evident that the p-value in each case is less than the level of significance s_α=0.05, indicating rejection of null hypothesis. It implies that HBA outperforms its competitor in a statistically significant manner.

Table 6.4. Statistical results obtained for different iteration count using t-test

Maximum Iteration	Significant analysis by t-test							
	HBA		p value HBA vs PSO	PSO		p value HBA vs GA	GA	
	Best	Mean		Best	Mean		Best	Mean
5	4.10%	4.17%	$1.47e^{-4}$	4.81%	4.92%	$6.01e^{-13}$	7.50%	7.51%
10	3.91%	4%	$4.14e^{-4}$	4.7%	4.85%	$7.5e^{-9}$	7.01%	7.20%
20	3.60%	3.63%	$4.37e^{-4}$	4.58%	4.65%	$8.1e^{-9}$	6.65%	6.77%
30	3.42%	3.58%	$8.32e^{-7}$	4.48%	4.56%	$3.12e^{-9}$	6.42%	6.57%
40	2.94%	3%	$8.45e^{-7}$	4.09%	4.10%	$6.23e^{-9}$	5.66%	5.80%
50	2.78%	2.89%	$4.6e^{-4}$	3.6%	3.92%	$4.01e^{-10}$	5.74%	5.75%
60	2.60%	2.68%	$7.56e^{-7}$	3.74%	3.88%	$2.65e^{-9}$	5.63%	5.66%
70	2.45%	2.50%	$8.2e^{-7}$	3.6%	3.65%	$6.68e^{-9}$	5.28%	5.30%
90	2.47%	2.48%	$4.11e^{-4}$	3.4%	3.56%	$1.38e^{-9}$	5.10%	5.15%
100	2.60%	2.70%	$2.14e^{-4}$	3.48%	3.50%	$4.65e^{-8}$	4.73%	4.84%
110	2.56%	2.60%	$2.68e^{-4}$	3.41%	3.50%	$4.16e^{-8}$	4.41%	4.56%
120	2.40%	2.48%	$3.01e^{-4}$	3.3%	3.42%	$6.02e^{-9}$	4.38%	4.47%
130	2.50%	2.52%	$1.35e^{-4}$	3.06%	3.12%	$7.13e^{-9}$	4.20%	4.26%

Table 6.5 Statistical results obtained for different population size using t-test

Population Size	Significant analysis by t-test							
	HBA		p value HBA vs PSO	PSO		p value HBA vs GA	GA	
	Best	Mean		Best	Mean		Best	Mean
5x4	4.16%	4.20%	$1.53e^{-4}$	4.83%	4.92%	$5.38e^{-11}$	7.61%	7.65%
7x4	3.41%	3.49%	$4.02e^{-4}$	4.29%	4.32%	$4.87e^{-13}$	6.72%	6.74%
9x4	2.71%	2.80%	$2.68e^{-4}$	3.57%	3.60%	$6.13e^{-9}$	5.59%	5.60%
10x4	2.47%	2.48%	$1.86e^{-4}$	3.2%	3.21%	$5.66e^{-9}$	4.7%	4.75%
15x4	2.471%	2.483%	$2.21e^{-4}$	3.22%	3.25%	$7.15e^{-9}$	4.6%	4.66%
20x4	2.47%	2.486%	$1.47e^{-4}$	3.1%	3.2%	$7.35e^{-9}$	4.4%	4.42%

Table 6.6. Comparative study with existing switching Techniques

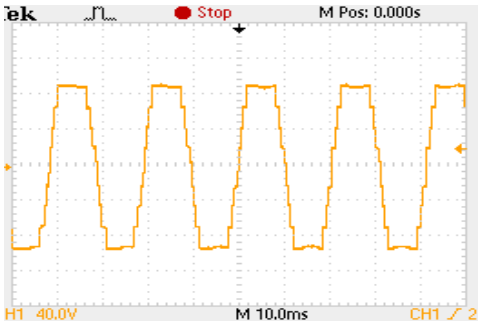
References	**Switching Techniques**	**output Voltage level**	**Voltage THD**
[6.6]	SPWM	9	13.65%
[6.7]	Staircase PWM	9	8.49%
		17	4.12%
[6.10]	Adaptive Neuro Fuzzy Interference System	7	9.17%
[6.12]	GA	9(1-phase)	16.90%
[6.19]	Asynchronous PSO-GA	7	11.47%
[6.21]	Opposition-based quantum bat algorithm	7	5.08%
		11	2.70%
[6.24]	PSO	5	7.21%
Presented scheme	HBA	9	2.48%

In Table 6.6, different switching techniques adopted by the MLI topologies of varying voltage level to minimize the output voltage THD are presented. It is observed that, HBA optimization technique has attained the lowest voltage THD for 9-level cascaded MLI effectively in comparison to other techniques applied in the literatures.

6.5 EXPERIMENTAL RESULTS

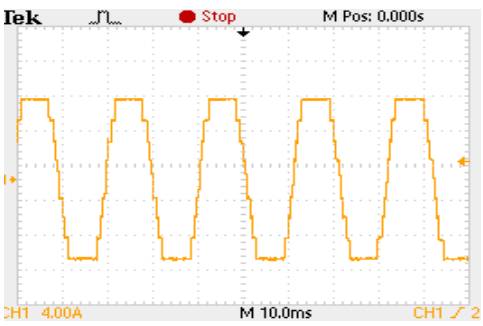
The development of a small-scale prototype in the lab has confirmed the functionality of a cascaded asymmetrical MLI with HBA switching control. Eight IGBTs (FGA25N120) are used in a single phase, 9-level cascaded MLI that has two DC voltage sources of 10V and 30V. Driver circuits based on TLP250H optocouplers activate the inverter switches. PIC microcontroller (PIC18f452) provides the gate pulses to the driving circuits. The switching angles for Modulation Index 0.8 are derived. The 9-level output voltage and current waveforms of the MLI are recorded while it is operating with an RL load of 100 and 15mH. The OPALRT -5650 real-time simulator is used to synchronise the grid with the three phase MLI. The output voltage, load current, grid voltage, and harmonic spectra of the voltage and current are recorded using a DSO model no-TDS 2022B. Figures 6.12 and 6.13, respectively, display the hardware and real-time simulator findings. Figure 6.14(a) depicts the OPALRT software setup installed on a PC, and Figure 6.14(b) depicts the prototype design created in the lab. After taking into account DC sources with adequate ratings, the suggested method can be used to create grid integrated converters up to a medium power level of 100 kW at LV (Low Voltage) distribution.

Y axis:20V/div, X axis: 5ms/div

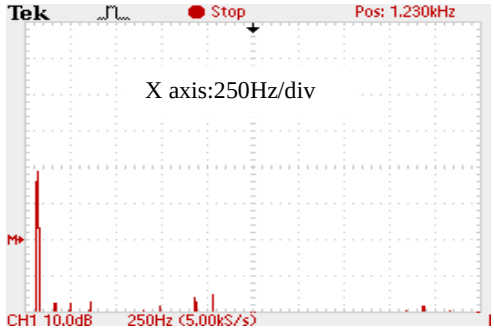


(a)

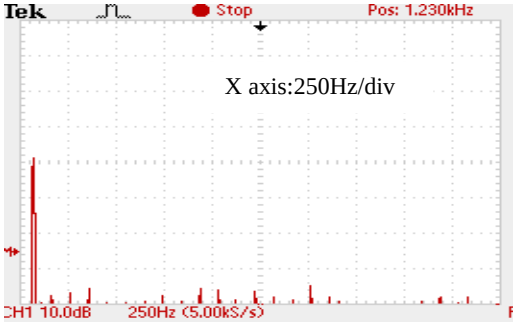
Y axis: 0.2A/div, X axis:5ms/div



(b)



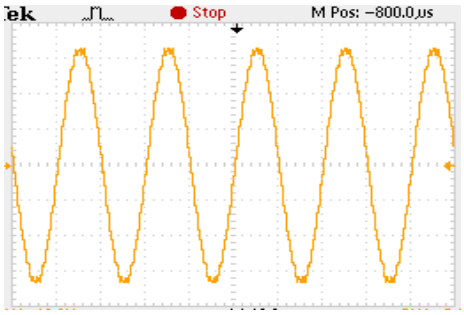
(c)



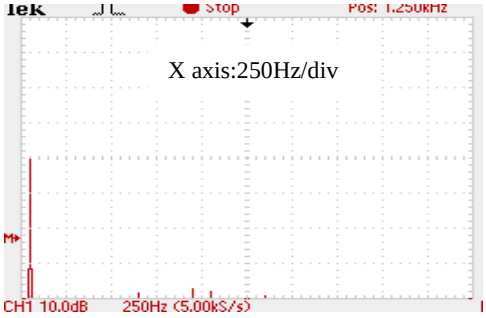
(d)

Figure 6.12. Hardware results (a) Output Voltage waveform, (b) Load Current waveform, (c) Output voltage harmonic spectrum, (d) Load current harmonic spectrum

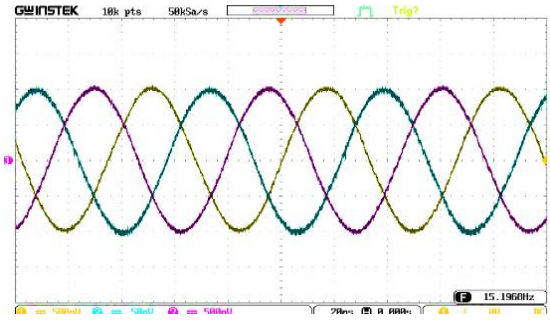
Y axis:200V/div, X axis:5ms/div



(a)

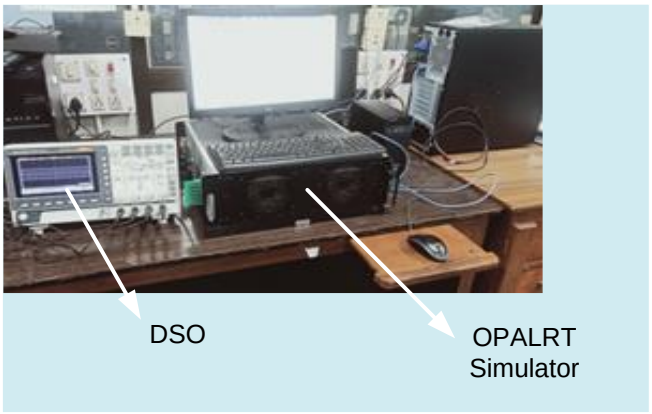


(b)

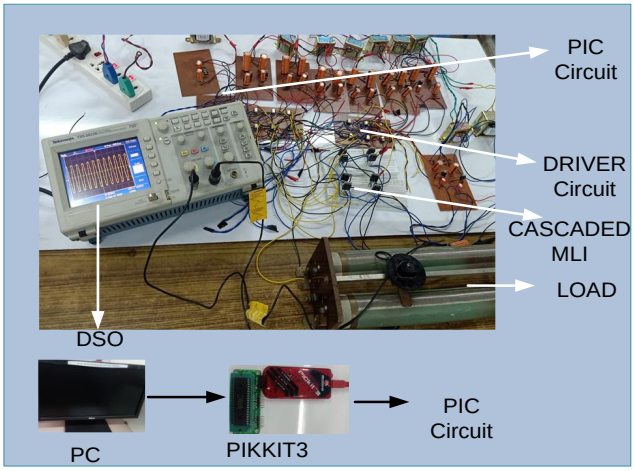


(c)

Figure 6. 13. Real time simulator results (OPALRT-5650) (a) Grid Voltage waveform (V_{AB}), (b) Harmonic spectrum of grid voltage, (C) Grid Voltages (phase to neutral)



(a)



(b)

Figure 6.14. Images of experimental set up (a) OPALRT set up picture, (b) Prototype developed in the laboratory

6.6 OBSERVATION

An asymmetrical voltage source MLI is used to develop higher output voltage level with minimum number of DC sources for grid synchronization. Minimising the harmonic distortion cascaded MLI verifies the superiority and efficacy of the newly developed metaheuristic algorithm HBA. By developing a simulation model of a nine-level MLI, the efficacy of HBA has been demonstrated, and the THD of output voltage has been reduced to 2.48 percent. Using the voltage and frequency control method, the MLI output voltage is incorporated into a 415V grid under suitable conditions, and the THD of the grid voltage is reduced to 1.02 percent. The employed algorithm determines the optimal switching angles at a faster convergence rate than other extant nature-based algorithms. Developing the hardware model of a nine-level cascaded

MLI verifies the simulation results. The proposed methodology has also been evaluated for grid integration using the OPALRT-5650 real-time simulator. To verify the capability of HBA, the harmonic spectra of the output voltage, load current of MLI, and grid voltage are also recorded. This newly developed algorithm can be implemented to solve various SHE problems for high-power converters with a larger number of stages, and it is also suitable for PV-grid integration utilising higher level MLI. The restricted DC voltage magnitudes, however, can be a problem for high-voltage grid integration.

6.7 PUBLICATION

[1] R. Mohanty, D Chatterjee, S. Suman, "Honey Badger Optimization based grid interactive asymmetrical cascaded MLI with minimum voltage distortion," Evolving Systems, Springer, 2023, DOI:10.1007/s12530-023-09493-1.

6.8 REFERENCES

[6.1] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4399–4406, 2009, doi: 10.1109/TIE.2009.2029579.

[6.2] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular Cascaded H-Bridge Multilevel PV Inverter with Distributed MPPT for Grid-Connected Applications," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1722–1731, 2015, doi: 10.1109/TIA.2014.2354396.

[6.3] H. Toopchizadeh, M. Zallaghi, M. Moradi, and S. Shahmoradi, "An effective shunt active power filter based on novel binary multilevel inverter and optimal type-2 fuzzy system to accurately mitigate harmonic currents," *Evol. Syst.*, no. 0123456789, 2022, doi: 10.1007/s12530-022-09465-x.

[6.4] A. M. Amjad, Z. Salam, and A. M. A. Saif, "Application of differential evolution for cascaded multilevel VSI with harmonics elimination PWM switching," *Int. J. Electr. Power Energy Syst.*, vol. 64, pp. 447–456, 2015, doi: 10.1016/j.ijepes.2014.07.023.

[6.5] S. Haq *et al.*, “An Advanced PWM Technique for MMC Inverter Based Grid-Connected Photovoltaic Systems,” vol. 31, no. 8, pp. 8–12, 2021.

[6.6] R. A. Vargas, A. Figueroa, S. E. Deleon, J. Aguayo, L. Hernandez, and M. A. Rodriguez, “Analysis of Minimum Modulation for the 9-Level Multilevel Inverter in Asymmetric Structure,” *IEEE Lat. Am. Trans.*, vol. 13, no. 9, pp. 2851–2858, 2015, doi: 10.1109/TLA.2015.7350030.

[6.7] C. Dhanamjayulu, D. Prasad, S. Padmanaban, P. K. Maroti, J. B. Holm-Nielsen, and F. Blaabjerg, “Design and Implementation of Seventeen Level Inverter with Reduced Components,” *IEEE Access*, vol. 9, pp. 16746–16760, 2021, doi: 10.1109/ACCESS.2021.3054001.

[6.8] G. S. Kulothungan, A. K. Rathore, J. Rodriguez, and D. Srinivasan, “Fundamental Device Switching Frequency Control of Current-Fed Nine-Level Inverter for Solar Application,” *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 1839–1849, 2020, doi: 10.1109/TIA.2019.2957714.

[6.9] K. Haghdar, “Optimal DC Source Influence on Selective Harmonic Elimination in Multilevel Inverters Using Teaching-Learning-Based Optimization,” *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 942–949, 2020, doi: 10.1109/TIE.2019.2901657.

[6.10] G. Nageswara Rao, P. Sangameswara Raju, and K. Chandra Sekhar, “Harmonic elimination of cascaded H-bridge multilevel inverter based active power filter controlled by intelligent techniques,” *Int. J. Electr. Power Energy Syst.*, vol. 61, pp. 56–63, 2014, doi: 10.1016/j.ijepes.2014.02.023.

[6.11] V. Mahajan, P. Agarwal, and H. O. Gupta, “An artificial intelligence based controller for multilevel harmonic filter,” *Int. J. Electr. Power Energy Syst.*, vol. 58, pp. 170–180, 2014, doi: 10.1016/j.ijepes.2014.01.020.

[6.12] S. K. Rai, L. Mathew, and S. L. Shimi, “Software and Hardware Implementation of a Nine Level Inverter with Low Component Count,” *IECON Proc. (Industrial Electron.*

Conf., vol. 2020-Octob, pp. 3318–3324, 2020, doi: 10.1109/IECON43393.2020.9254836.

[6.13] S. Y. Nikouei, B. M. Dehkordi, and M. Niroomand, "A Genetic-Based Hybrid Algorithm Harmonic Minimization Method for Cascaded Multilevel Inverters with ANFIS Implementation," *Math. Probl. Eng.*, vol. 2021, no. 1, 2021, doi: 10.1155/2021/6642317.

[6.14] R. N. Ray, D. Chatterjee, and S. K. Goswami, "An application of PSO technique for harmonic elimination in a PWM inverter," *Appl. Soft Comput. J.*, vol. 9, no. 4, pp. 1315–1320, 2009, doi: 10.1016/j.asoc.2009.05.002.

[6.15] V. K. Gupta and R. Mahanty, "Optimized switching scheme of cascaded H-bridge multilevel inverter using PSO," *Int. J. Electr. Power Energy Syst.*, vol. 64, pp. 699–707, 2015, doi: 10.1016/j.ijepes.2014.07.072.

[6.16] M. Tarafdar Hagh, H. Taghizadeh, and K. Razi, "Harmonic minimization in multilevel inverters using modified species-based particle swarm optimization," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2259–2267, 2009, doi: 10.1109/TPEL.2009.2022166.

[6.17] K. P. Panda and G. Panda, "Application of swarm optimisation-based modified algorithm for selective harmonic elimination in reduced switch count multilevel inverter," *IET Power Electron.*, vol. 11, no. 8, pp. 1472–1482, 2018, doi: 10.1049/iet-pel.2017.0697.

[6.18] A. Routray, R. K. Singh, and R. Mahanty, "Harmonic Reduction in Hybrid Cascaded Multilevel Inverter Using Modified Grey Wolf Optimization," *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 1827–1838, 2020, doi: 10.1109/TIA.2019.2957252.

[6.19] Memon MA, Siddique MD, Mekhilef S, et al (2022) Asynchronous Particle Swarm Optimization-Genetic Algorithm (APSO-GA) Based Selective Harmonic Elimination in a Cascaded H-Bridge Multilevel Inverter IEEE Trans Ind Electron 14: 1477–1487. https: //doi.org/10.3390/su14010310.

[6.20] K. Haghdar and H. A. Shayanfar, “Selective Harmonic Elimination with Optimal DC Sources in Multilevel Inverters Using Generalized Pattern Search,” *IEEE Trans. Ind. Informatics*, vol. 14, no. 7, pp. 3124–3131, 2018, doi: 10.1109/TII.2018.2790931.

[6.21] J. Islam *et al.*, “Opposition-Based Quantum Bat Algorithm to Eliminate Lower-Order Harmonics of Multilevel Inverters,” *IEEE Access*, vol. 9, pp. 103610–103626, 2021, doi: 10.1109/ACCESS.2021.3098190.

[6.22] J. Stöttner, A. Rauscher, and C. Endisch, “Pareto optimization of multilevel inverter structures regarding the DC magnitude, switching frequency and switching angles,” *Int. J. Electr. Power Energy Syst.*, vol. 142, no. PA, p. 108259, 2022, doi: 10.1016/j.ijepes.2022.108259.

[6.23] F. A. Hashim, E. H. Houssein, K. Hussain, M. S. Mabrouk, and W. Al-Atabany, “Honey Badger Algorithm: New metaheuristic algorithm for solving optimization problems,” *Math. Comput. Simul.*, vol. 192, pp. 84–110, 2022, doi: 10.1016/j.matcom.2021.08.013.

[6.24] R. N. Ray, D. Chatterjee, and S. K. Goswami, “Harmonics elimination in a multilevel inverter using the particle swarm optimisation technique,” *IET Power Electron.*, vol. 2, no. 6, pp. 646–[652, 2009, doi: 10.1049/iet-pel.2008.0180.

Chapter-7

PROPOSED S-CROSS REDUCED SWITCH MLI for GRID INTEGRATION

This Chapter proposes a new topology of reduced switch MLI with minimum asymmetrical voltage sources of different combination. The proposed topology uses cascaded cross switch pattern and 'S' switch pattern across the voltage sources to develop higher output voltage level. The optimum switching angles are derived from an efficient and computationally in extensive Black Widow Optimization algorithm. The performance of the proposed MLI is verified by developing a prototype under both grid connected and isolated condition.

PROPOSED S-CROSS REDUCED SWITCH MLI for GRID INTEGRATION

7.1 INTRODUCTION

MLI topologies with asymmetrical DC voltage sources provide higher voltage level in comparison to the symmetrical ones using same number of power devices. In the previous chapter the performance of cascaded MLI with asymmetrical voltage sources is discussed, which requires smaller number of power devices to generate higher voltage level. A reduced MLI design has been proposed in [7.1] with minimum numbers of power switches using different combination of DC voltage sources. A switched diode based cascaded MLI has been introduced in [7.2] with minimum switching devices in order to reduce the driver circuit and power loss. MLI with two unequal DC voltage sources and two capacitors for 13 level output has also been proposed in [7.3]. But all these asymmetrical MLIs use extra capacitors, diodes, and bidirectional switches, which can lead to additional losses and reduced reliability. A compact 5 level MLI with modified packed U cell structure has been proposed for PV application [7.4] and a reduced cross switched MLI (CSMLI) with symmetrical voltage sources is presented in [7.5]. These above topologies avoid the use of extra component for generating higher number of steps in output voltage.

Development of MLI topologies comes with a challenge of designing the switching schemes to generate suitable triggering angles for obtaining minimum distortion in output voltage. Sinusoidal pulse width modulation (SPWM) has been adopted for CHBMLI in [7.6] and level shifting SPWM for developing the switching strategy of a newly designed reduced MLI has been presented in [7.7]. The performance of the modular MLI has been improved with a well-developed PWM switching technique [7.8] to achieve low THD of the output voltage. But this MLI has used the filter circuit to reduce the THD below 5%. The PWM switching techniques are performed under high frequency that leads to high switching loss. Another major point of concern is, for developing the higher voltage level PWM techniques require more number of nonlinear equations to be solved which increases the complexity. Thus, different heuristic or metaheuristic algorithm e.g., Genetic Algorithm (GA), Ant colony Algorithm (ACA), Particle Swarm Optimization (PSO) algorithm proposed in different articles for solving complex optimization problem. The output voltage THD of a

CHBMLI has been minimized with PSO algorithm in [7.9],[7.10]. This algorithm has the limitation to get stuck in local optima for higher number of population which has been avoided in [7.11] and [7.12] by implementing species based PSO and modified PSO respectively. In order to improve the convergence of optimization a chaotic search based Grey Wolf Optimization (MGWO) algorithm has been presented in [7.13]. This algorithm has been implemented efficiently to discard the lower order harmonics from the output voltage of CHBMLI.

This chapter presents a novel S-Cross topology of reduced switch MLI with the following unique features.

a) Higher number of output voltage level to source ratio compared to existing topologies. This is achieved by cascading both the cross switch and 'S' switch structure across input DC voltage sources.
b) Moreover, the proposed topology uses lower number of switching devices which can be suitable for grid integration with better reliability.
c) This topology avoids the use of H-Bridge to generate full cycle AC voltage unlike [7.14 – 7.16] and hence reduces the switching losses.
d) As the distortion is low for the output voltage, the proposed MLI does not require any output filter circuit for power quality improvement.
e) The proposed topology has showed minimum voltage THD with optimized switching angles which is presented in section 7.4. The lower and higher order harmonic voltages are minimized through the switching angles obtained by Black Widow Optimization algorithm [7.17] with modified steps.

Simulation and experimental analysis of a 3 phase 19 level MLI has been carried out to corroborate the developed methodology. The performance of the proposed topology for grid interconnection is also verified through real time simulation using OPALRT-5650.The working principle of the proposed MLI topology is discussed in the next section.

7.2 PROPOSED S-CROSS SWITCHED MLI

The proposed MLI topology requires only three DC voltage sources per phase to generate different output voltage levels by selecting suitable voltage ratios of the energy sources. The proposed topology can generate 15,17,19 and 21 level of output voltage which depends on

the ratio of DC voltage sources. More than 21 level of output voltage can be generated by connecting the cross switch pattern and S-switch pattern alternatively (S-cross structure) as shown in figure 7.1. This chapter presents a 19-level S-Cross MLI with the suitable switching pattern discussed in Table 7.1. The ratios of input DC voltage sources for generating the above discussed voltage level are given in equation (1).

$$V1:V2:V3 = 1:2:6 \tag{7.1}$$

Developed MLI has achieved minimum voltage THD with optimum switching angles. The proposed MLI circuit for single phase is shown in figure.1.

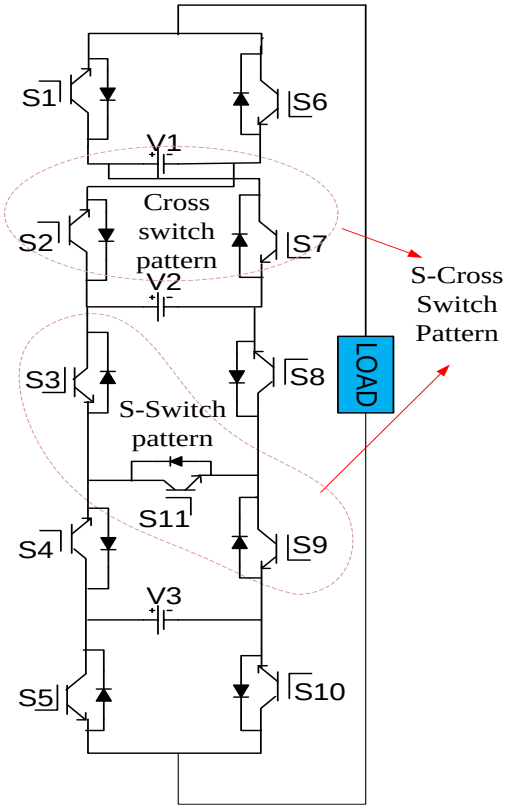


Figure 7.1. Proposed MLI configuration for single phase

The maximum output voltage can be derived by using equation (7.2).

$$V_{max} = V1 + V2 + V3 \tag{7.2}$$

$V_{max} = 9V_D$ for 19 level S-cross MLI. V_D is the step voltage magnitude at each level which has explained in previous chapters. The three phase circuit arrangement for the proposed topology is shown in figure 7.2.

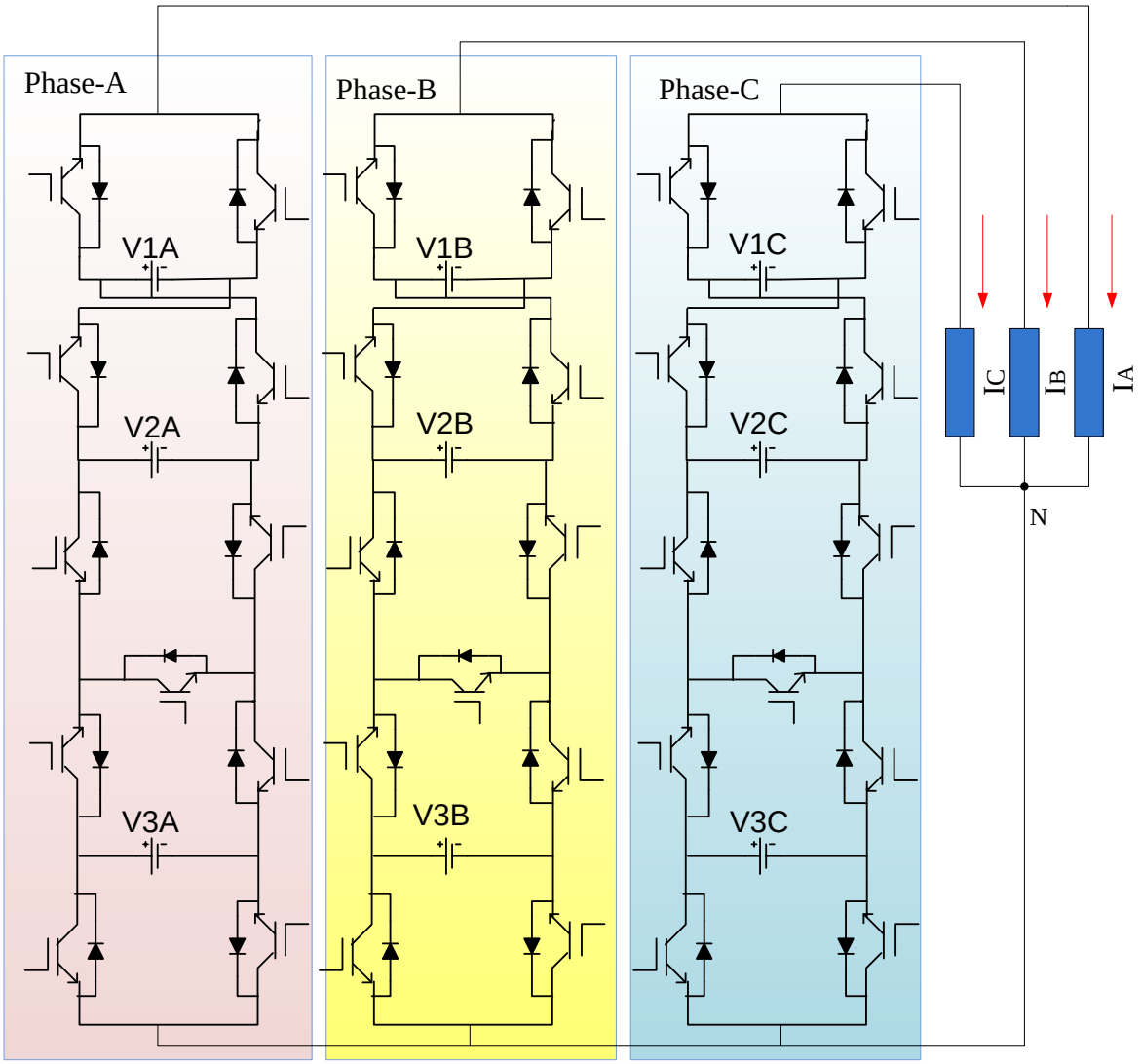


Figure 7.2. Proposed MLI configuration for three phase

Table 7.1. Switching pattern for 19 level S-Cross MLI

Switching Scheme for 19 Level Output Voltage																	
Switches	V1	V2	V1+V2	V3-V2	V3-V1	V3	V3+V1	V3+V2	V1+V2+V3	-V1	-V2	-(V1+V2)	-(V3-V2)	-(V3-V1)	-V3	-(V3+V1)	-(V3+V2)	-(V1+V2+V3)
S1	1	0	1	1	0	0	1	0	1	0	1	0	0	1	1	0	1	0
S2	1	1	1	0	0	1	1	1	1	0	0	0	1	1	0	0	0	0

S3	1	0	0	1	0	1	1	0	0	0	1	1	0	1	0	0	1	1
S4	1	0	0	1	1	1	1	1	1	0	1	1	0	0	0	0	0	0
S5	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
S6	0	1	0	0	1	1	0	1	0	1	0	1	1	0	0	1	0	1
S7	0	0	0	1	1	0	0	0	0	1	1	1	0	0	1	1	1	1
S8	0	1	1	0	1	0	0	1	1	1	0	0	1	0	1	1	0	0
S9	0	1	1	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
S10	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
S11	0	0	0	0	1	0	0	1	1	0	0	0	0	1	0	0	1	1

Different output voltage level of the proposed MLI depends on the combination of DC voltage sources which is cited in Table 7.2. The proposed MLI exhibits the relationship for developing maximum output voltage level (V_{lmax}) with the input DC voltage sources by the following equation.

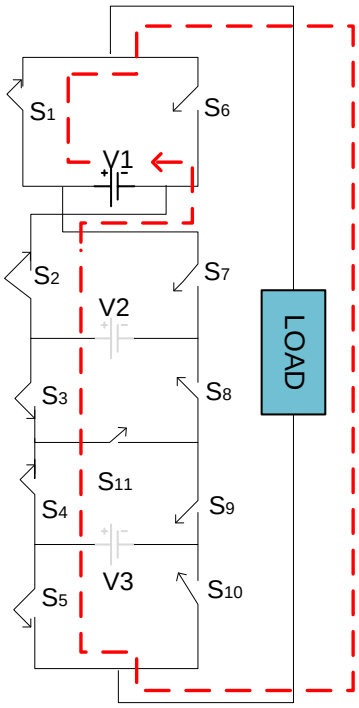
$$V_{lmax} = 3 * (2^N - 1) \tag{7.3}$$

Table 7.2. Output voltage level, DC voltage source combination and number of switching devices for the proposed MLI

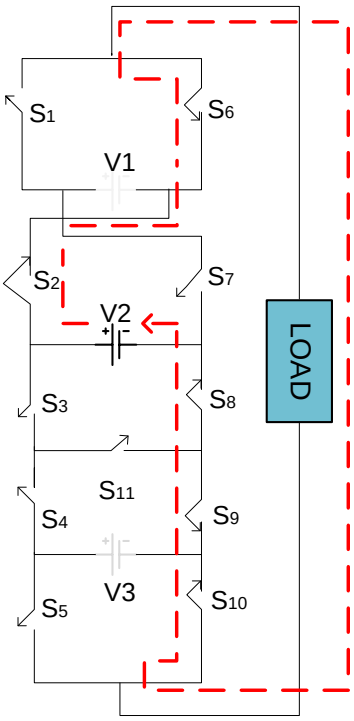
Proposed MLI with 3 Voltage Sources				Proposed MLI with 2 Voltage Sources			
V1:V2:V3	Structure	Voltage Level	No of Power Devices	V1:V2	Structure	Voltage Level	No of Power Devices
1:4:2	Combination of cross structure and S structure	15	11	1:1	only cross structure	5	6
1:2:5		17	11	1:2	only cross structure	7	6
1:2:6		19	11	1:3	only S structure	9	9
1:2:7		21	11				

7.2.1 Operation of 19-level S-Cross MLI

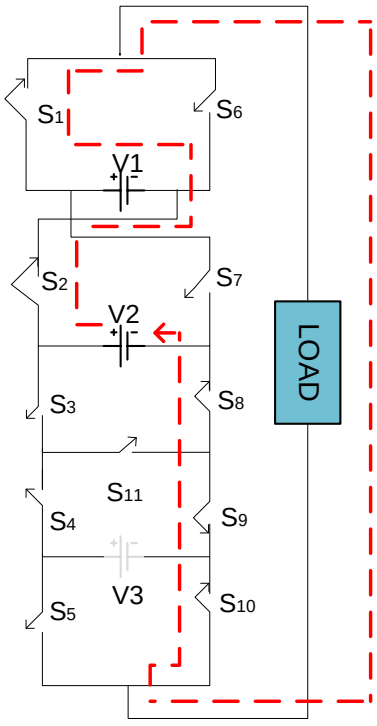
The working of S-Cross MLI has been explained by nine modes and at each mode the generation of output voltage level is also explained in the following figures.


S1
S6
V1
S2
S7
V2
S3
S8
S11
S4
S9
V3
S5
S10
LOAD

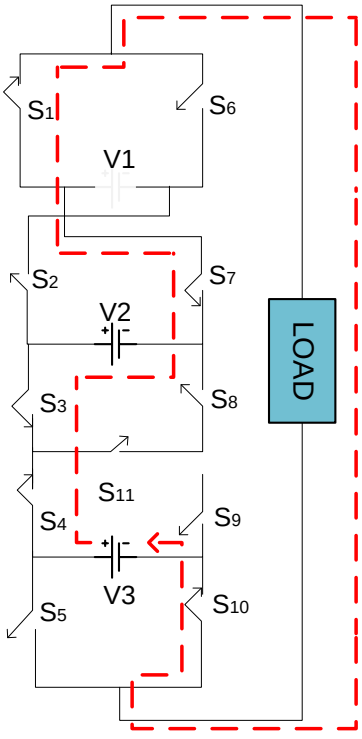
(a)


S1
S6
V1
S2
S7
V2
S3
S8
S11
S4
S9
V3
S5
S10
LOAD

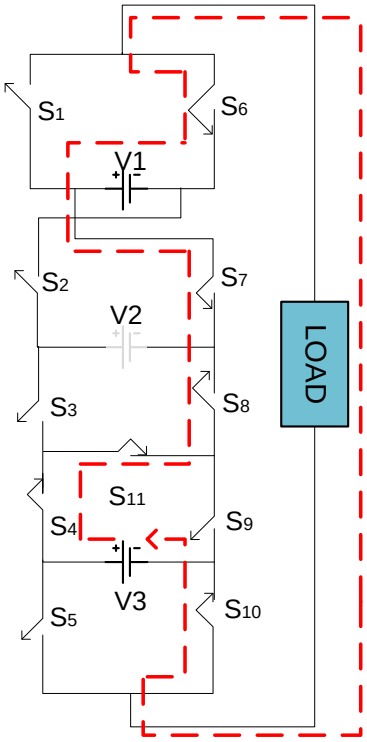
(b)


S1
S6
V1
S2
S7
V2
S3
S8
S11
S4
S9
V3
S5
S10
LOAD

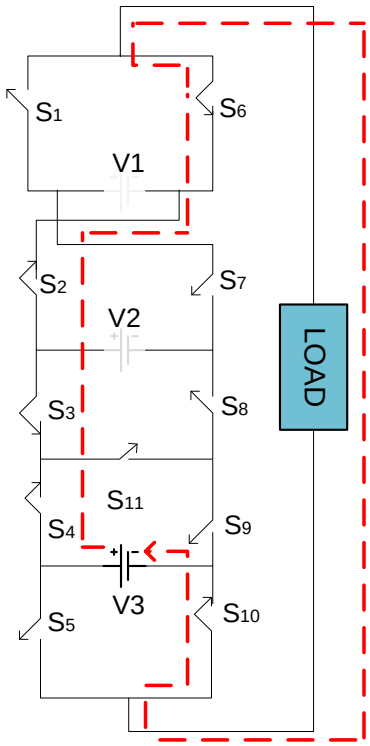
(c)


S1
S6
V1
S2
S7
V2
S3
S8
S11
S4
S9
V3
S5
S10
LOAD

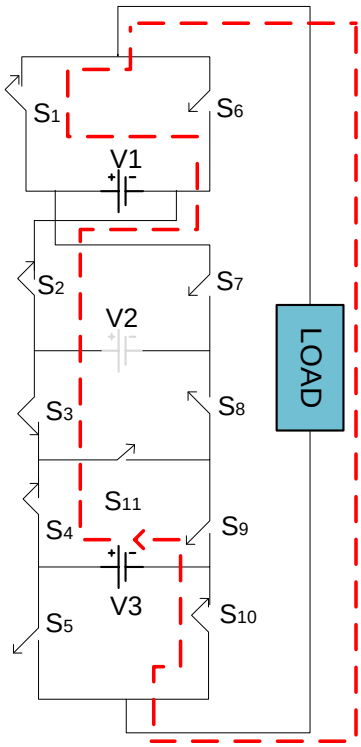
(d)


S1
S6
V1
S2
S7
V2
LOAD
S3
S8
S11
S4
S9
V3
S5
S10

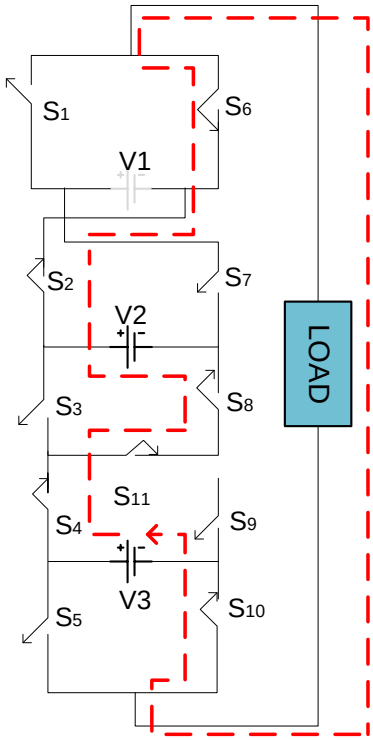
(e)


S1
S6
V1
S2
S7
V2
LOAD
S3
S8
S11
S4
S9
V3
S5
S10

(f)


S1
S6
V1
S2
S7
V2
LOAD
S3
S8
S11
S4
S9
V3
S5
S10

(g)


S1
S6
V1
S2
S7
V2
LOAD
S3
S8
S11
S4
S9
V3
S5
S10

(h)

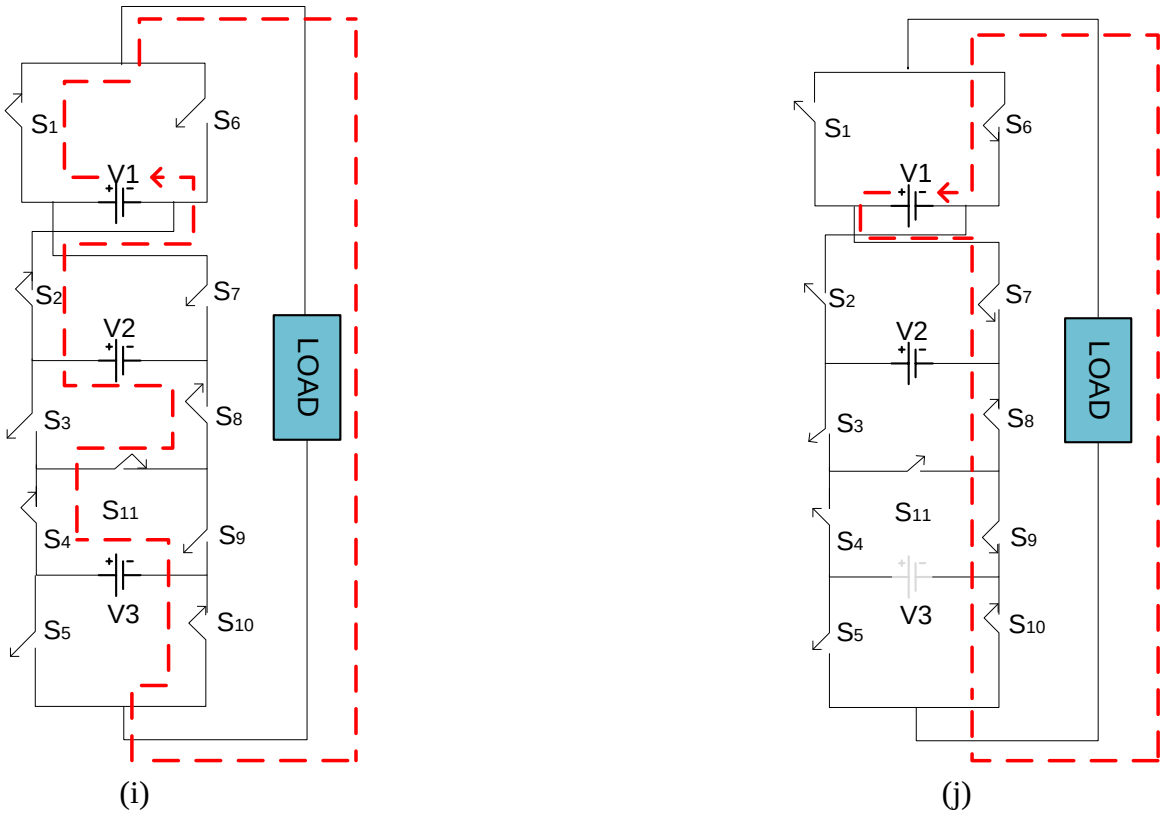
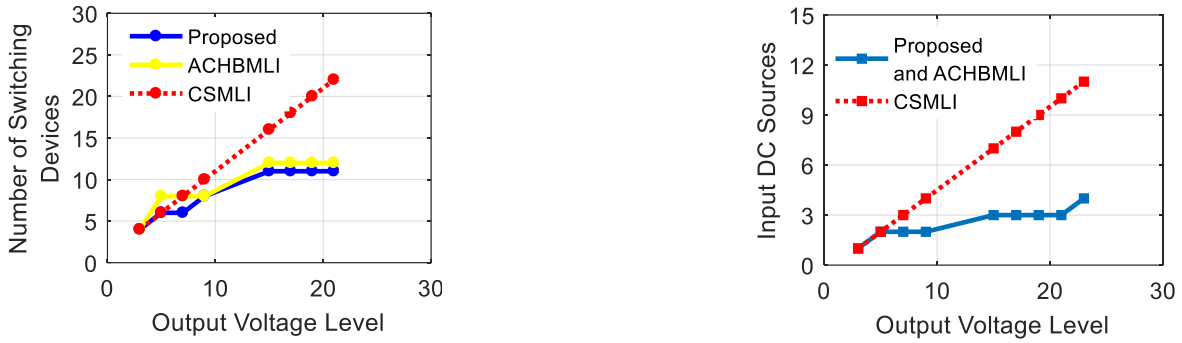


Figure 7.3. Nine Mode operation of 19 level S-Cross MLI. (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5, (f) Mode 6, (g) Mode 7, (h) Mode 8, (i) Mode 9, (j) Mode 1 of negative cycle

To generate the 19-level output voltage, 11 power switches are operated according to Table 7.1 for different steps. In 5,8, and 9 modes, six power switches are operated and in rest of the modes only five power switches are operated to generate the desired voltage levels. Figure 7.3 (a) describes mode 1 operation of the MLI, where the output voltage is V1. Current flow in the inverter is shown by arrow in the figures. In mode 2, the output voltage of the MLI is V2, which has explained in figure 7.3(b). In mode 3, MLI generates (V1+V2) across load describes by figure 7.3(c). In mode 4, MLI generates (V3-V2) across load describes by figure 7.3(d). In mode 5, MLI generates (V3-V2) across load describes by figure 7.3(e). In mode 6, MLI generates (V3) across load describes by figure 7.3(f). In mode 7, MLI generates (V1+V3) across load describes by figure 7.3(g). In mode 8, MLI generates (V3+V2) across load describes by figure 7.3(h). The maximum output voltage (V1+V2+V3) is resulted in mode 9 and the circuit operation is explained in figure 7.3(i). Similarly, the negative cycle voltage levels are generated by following the switching pattern developed in

Table 7.1. Mode 1 operation of the negative cycle is explained through figure 7.3(j) for the reference.

Number of DC voltage sources and switching devices required by the proposed MLI and other existing MLIs for generating different output voltage level has been illustrated in figure 7.4. From figure 7.4 it can be observed that proposed reduced MLI requires a smaller number of switching devices and voltage sources for developing higher output voltage level than the other reduced MLI discussed in the literatures.



(a) (b)

Figure 7.4. (a) Output voltage Level vs Number of Switching Devices, (b) Output Voltage Level vs Input Dc sources, required by Proposed MLI and other existing MLIs

7.3 MATHEMATICAL MODELLING

7.3.1 Voltage Harmonic elimination

The output voltage waveform of the MLI is half wave symmetry in nature. The expression of the 19-level MLI output voltage has been derived in the following equation.

$$V(\omega t) = \sum_{\alpha=1}^{ai} \frac{4V_D}{n\pi} \left(\cos(n\alpha_1) + \cos(n\alpha_2) + \cdots + \cos(n\alpha_{ai}) \sin(\omega t)\right) \quad (7.4)$$

In the above equation '*ai*' represents the number of switching angles for the proposed MLI. For the proposed 19- level MLI, *ai* = 9. 'n' represents odd harmonics content in the output voltage. The nonlinear equations are solved to get the optimum switching angles for minimizing the harmonic distortion of out put voltage are given below.

$$\left.\begin{aligned}
&\cos(\alpha_1) + \cos(\alpha_2) + \cdots + \cos(\alpha_9) = KV_1 \\
&\cos(5\alpha_1) + \cos(5\alpha_2) + \cdots + \cos(5\alpha_9) = 0 \\
&\cos(7\alpha_1) + \cos(7\alpha_2) + \cdots + \cos(7\alpha_9) = 0 \\
&\cos(11\alpha_1) + \cos(11\alpha_2) + \cdots + \cos(11\alpha_9) = 0 \\
&\cos(13\alpha_1) + \cos(13\alpha_2) + \cdots + \cos(13\alpha_9) = 0
\end{aligned}\right] \quad (7.5)$$

'*K*' value is already discussed in chapter 3. The modulation index has been derived in equation 7.6.

$$MI = \frac{V_1}{V_{Max}} \quad (7.6)$$

$$V_{Max} = \frac{(V_l - 1)}{2} * V_D \quad (7.7)$$

Output voltage level of the MLI is denoted by V_l.

7.3.2 Control Scheme for Grid Integration

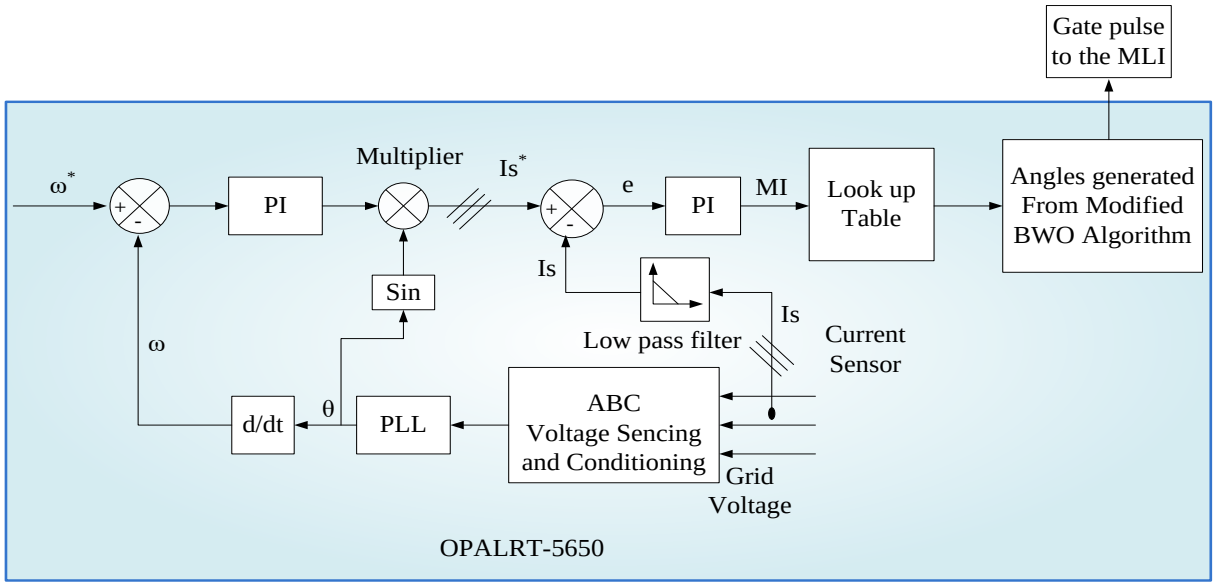


Figure 7.5. Control scheme of grid integrated MLI

In this chapter the optimum switching angles for S-Cross MLI are derived by using Black Widow Optimization (BWO) algorithm with reduced steps. The eficasy of the algorithm has

been verified by connecting the MLI to three phase grid system of 50Hz. The harmonic distortion of grid voltage has been minimized by adopting the control scheme in real time simulator using OPALRT-5650. The control scheme is shown in figure 7. 5. The grid voltage and curent are measured through voltage and current sensor respectively. As the MLI is operated in fundmental frequency, the deviation in voltage angle is controlled through the outer loop. The error of angular frequency has been processed by PI controller and through multiplier the reference current is generated which has been compared with the grid current. The difference in current is regulated through PI controller and the output is treated as the modulation index (MI) as shown in figure 7.5. The switching angles for the respective MI developed from modified BWO algorithm are provided to the MLI gate circuits using the pre defined look up table. The results of grid output voltage and the harmonic spectrum are verified using the RT simulator that has discussed in section 7.5.

7.3.3 Total Standing Voltage

Total Standing Voltage (TSV) is the essential factor for inverter that decides the rating of power switches. Standing voltage is the maximum blocking voltage of a power switch during its turn off condition. Maximum blocking voltage of the switch debends on the connected voltage sources across it. From figure 7.1 and figure 7.3 the standing voltage across each switch is as follows.

$$\left.\begin{aligned} V_{S1} &= V_{S6} = V1 \\ V_{S2} &= V_{S7} = V1 + V2 \\ V_{s3} &= V_{S8} = V_{S11} = V2 \\ V_{S4} &= V_{S5} = V_{S9} = V_{S10} = V3 \end{aligned}\right] \tag{7.8}$$

From equation (7.8), TSV of the proposed MLI has been determined by the following equation.

$$TSV_{MLI} = 4 * (V1 + V2 + V3) + V2 \tag{7.9}$$

The TSV in terms of source voltage for 19-level proposed MLI can be expressed as:

$$4(N^2 + 2) * V_D \tag{7.10}$$

Here $(4N^2 + 2)$ has been treated as the TSV factor. The TSV for different output voltage level is showm in figure 7.6.

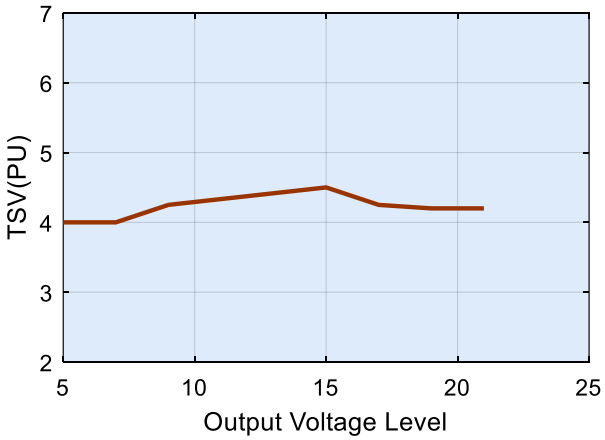


Figure 7.6. TSV per unit vs Output Voltage level of the proposed MLI

A Comparitive analysis of proposed MLI with the existing reduced switch MLIs, in terms of requirement of component, output voltage level and TSV is shown in Table 7.3

Table 7.3. Requirement of component, output voltage level and TSV in terms of dc voltage source

MLI Topologies with 'S_{DC}' number of DC Sources	Type of DC Sources	MLI Topologies	Output Voltage level	No of Power Switches	No of diodes	No of capacitors	No of driver Circuits	No of antiparallel diodes	TSV factor in terms of DC voltage source
	Symmetrical DC Sources	[7.5]	$2N+1$	$2(N+2)$	0	0	$2(N+2)$	$2(N+2)$	$4N$
		[7.14]	$2N+1$	$2(N+1)$	0	0	$2(N+1)$	$2(N+1)$	$6N$
	Asymmetrical DC Sources	[7.1]	$5N+1$	$7N/2$	0	N	$7N/2$	$7N/2$	$19(N/2)$
		[7.2]	$2*6^{N/3}-1$	$N+4$	N	0	$N+4$	$N+4$	$\frac{34}{5}\left(6^{N/3}-1\right)$
		[7.3]	$6N+1$	$7N$	0	N	$5N+1$	$7N$	$16N$
		[7.4]	$2^{N+1}-1$	$2(N+1)$	0	0	$2(N+1)$	$2(N+1)$	$2^{N+2}-4$
		[7.13]	$6N-1$	$6N$	0	$N/2$	$6N$	$6N$	$5N$
		[7.18]	$3*2^N-5$	$4N$	0	0	$4N$	$4N$	$4N^2$

		Proposed	$3(2^N)-5$	$4N-1$	0	0	$4N-1$	$4N-1$	$4N^2+2$
			$3(2^N-1)$	$4N-1$	0	0	$4N-1$	$4N-1$	$4N^2+6$

7.4 SIMULATION RESULTS AND COMPARATIVE STUDY

The operation and performance of the presented MLI has been verified by simulating it for three phase,19 level with output voltage of 450V RMS. The output voltage and current waveforms are evaluated for RL load of 0.98 power factor. The FFT analysis of the output voltage has been recorded to test the effectiveness of the MLI. For getting the optimum switching angles, BWO algorithm with modified steps has been implimented. The cannibalism process makes this algorithm most efficient by avoiding the local optima which is the major disadvantages of GA and conventional PSO. The mutation step of BWO algorithm is dropped to reduce the operational time. The population is updated from the strongest child, which has introduced in this research. Coherence of this algorithm has been verified by the comparative study of solving THD minimization problem with conventional PSO algorithm.

7.4.1 Black Widow Optimization Algorithm with modified Steps

Black widow Optimization has been proposed by V. Hayyolalam and A.P Kazem in the year 2020 to solve the real world problem. The mating process of Black Widow spider and reproduction of their offspring has been mimicked to develop this algorithm. This algorithm has set a benchmark for solving real engineering problem with a greater accuracy as discussed in [7.17]. The new offspring or child can be generated by the following equation.

$$\left.\begin{aligned} Ch_1 &= \gamma * p_1 + (1-\gamma) * p_2 \\ Ch_2 &= \gamma * par_2 + (1-\gamma) * p_1 \end{aligned}\right] \qquad (7.11)$$

Where p_1 and p_2 are the two group of parents and γ is the randomly generated array with same length of parents. After reproduction of new child, the stronger child is selected and

rest are discarded by cannibalism. In order to achieve the better convergence, the steps of BWO algorithm are limited and the population selected from the stronger child is updated using equation (7.12).

$$Ps_{new} = Ps_{old} + R(Ch_{best} - Ps_{old}) \quad (7.12)$$

Where Ps_{new} is the updated Black widow spider, Ch_{best} is the stronger child and 'R' is the random number between 0 and 1.

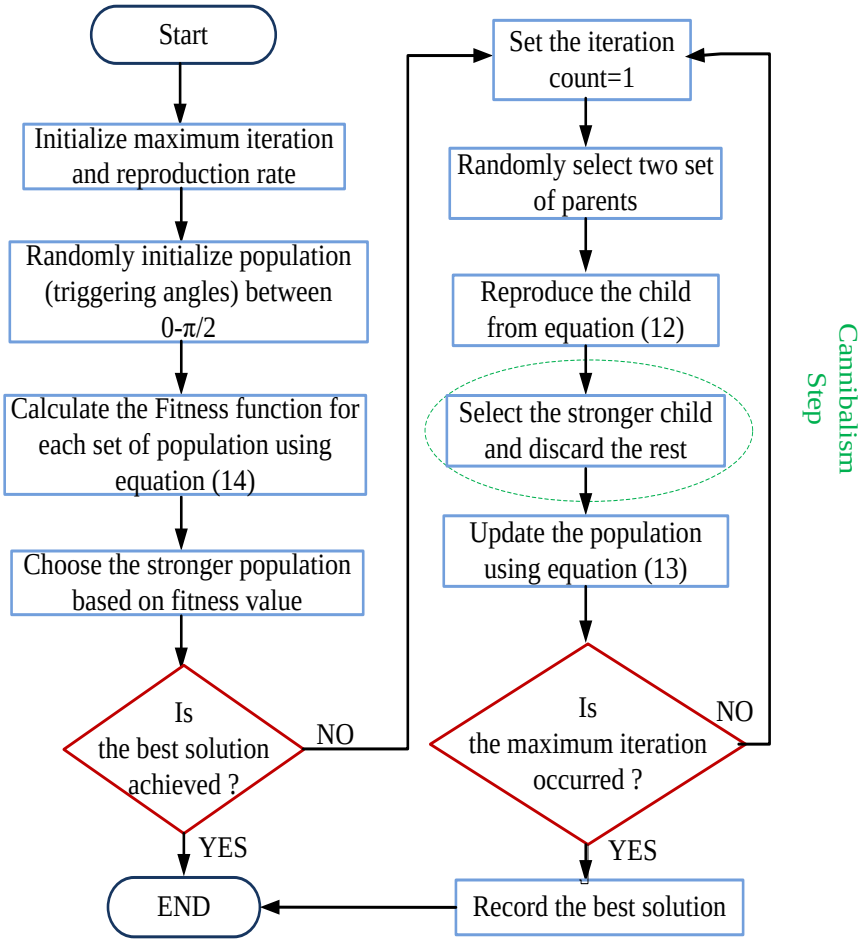


Figure 7.7. BWO Algorithm with reduced steps

Here the switching angles are treated as the population or widow that need to initialize randomly between 0 to π/2. A population matrix of [k x i] is generated for the mating and reproduction process as discussed in section A. The steps for the algorithm to obtain the best

solution or the minimum voltage THD are explained using the flowchart shown in figure 7.7. The fitness function is expressed using equation (7.13).

$$F = min \frac{\sqrt{\sum_{n=3,5\ldots}^{49} V_n^2}}{V_1} \tag{7.13}$$

The performance of reduced step BWO algorithm has been verified from the simulation results by operating the MLI with the optimum switching angles. The efficiency of the above algorithm has been substantiated through comparison analysis with the most popular swarm based algorithm known as PSO.

7.4.2 Simulation Results

The optimum switching angles derived from BWO and PSO algorithms with the respective voltage THD are given in Table 7.4. The three phase 19-level MLI is simulated with the optimum angles for modulation Index 0.92. Line voltage and load current waveforms using RL load are shown in figure 7.8 (a) and 7.8 (b) respectively. The grid connection of proposed MLI has also been studied in MATLAB 2016b. The grid voltage waveform and synchronized MLI output voltage with grid voltage are shown in figure 7.8 (c) and 7.8 (d) respectively. The output voltage harmonic spectrum using PSO and BWO algorithm are shown in figure 7.9 (a) and 7.9 (b) respectively. Harmonic spectrum of grid voltage and respective THD is shown by figure 7.9 (c).

Table 7.4. Switching angles obtained from PSO and BWO optimization with respective voltage THD

Optimization Algorithm	Switching Angles (Degrees)									Overall Voltage THD (%)
	α_1	α_2	α_3	α_4	α_5	α_6	α_7	α_8	α_9	
PSO	2.67	3.94	8.48	14	21.6	27	32	39.6	49.7	2.68%
BWO	3.26	3.39	11.96	13.4	21	23	30	40.4	46.4	1.96%

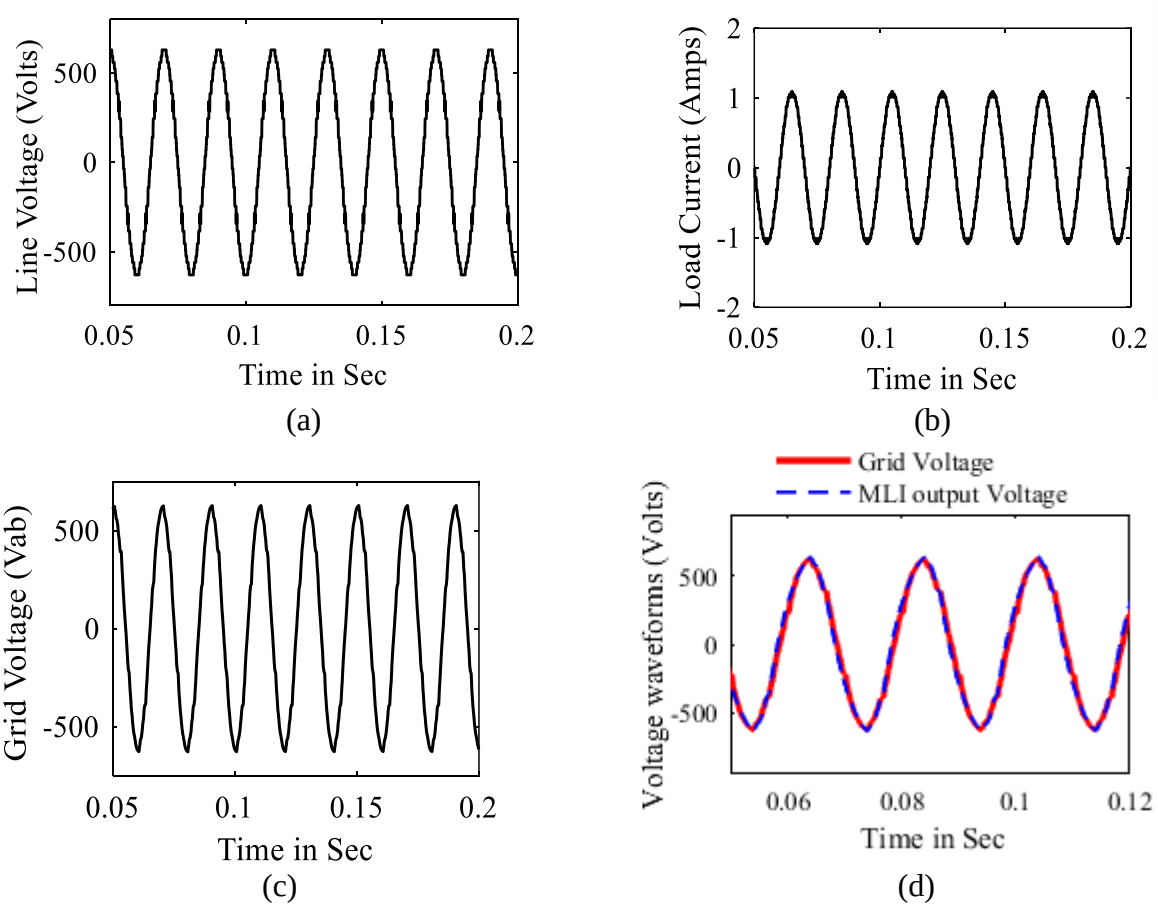
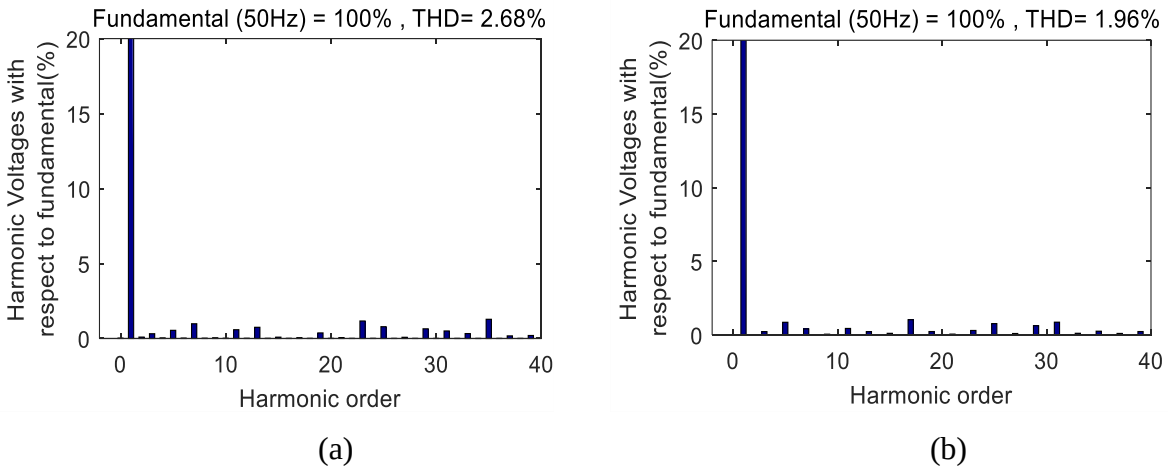
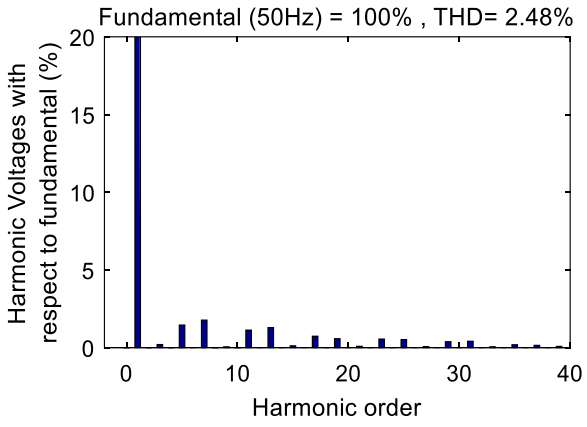


Figure 7.8. MLI output waveforms. (a) Line voltage waveform with RL load, (b) Load current waveform, (c) Grid Voltage Waveform (b) Synchronized MLI and grid Voltages

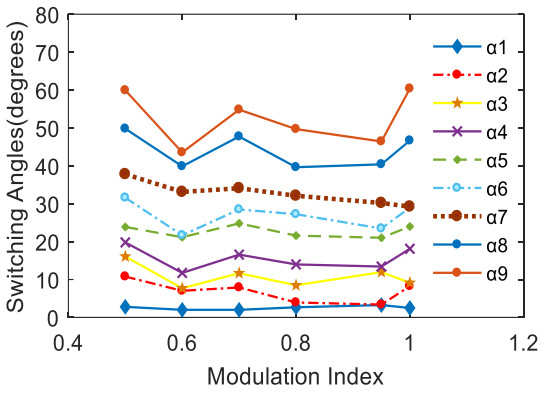




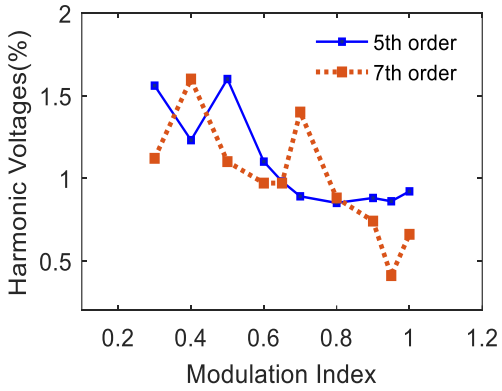
(c)

Figure 7.9. Harmonic Spectrum for output voltage and overall THD (a) MLI using PSO algorithm, (b) MLI using BWO algorithm, (c) Grid connected MLI with BWO algorithm

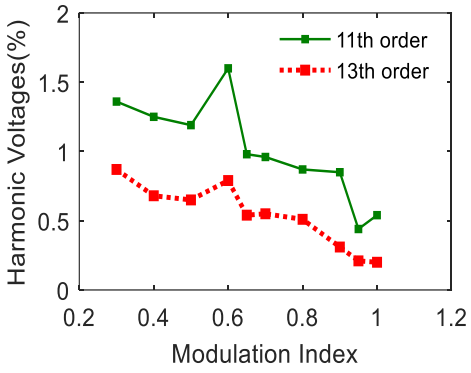
From figure 7.9 it can be observed that the proposed topology can develop higher level output voltage with minimum distortion and provides the lowest voltage THD using BWO algorithm. The optimum switching angles are determined offline over a wide range of modulation index and lowest THD has been achieved at modulation index 0.92. This can be stored in the form of mixed model equations [7.19] for online application. The switching angles for varying modulation indices and behaviour of nth order harmonic voltages with respect to modulation index obtained from BWO algorithm are shown in figure 7.10. By conducting a comparison study with the generally recommended PSO method, the effectiveness of the modified step BWO approach for solving the THD minimization problem is confirmed. Figure 7.11(a) illustrates the minimal voltage THD for a range of modulation indices, demonstrating that BWO produces the lowest voltage THD for each modulation indices. Figure 7.11(b) illustrates a typical covergence feature for both algorithms. It can be seen from this figure that BWO has a faster convergence rate for every maximum iteration value that is specified. Figure 7.11(c) also displays the objective function values for different maximum iteration settings, demonstrating that the BWO method achieves the best convergence.



(a)

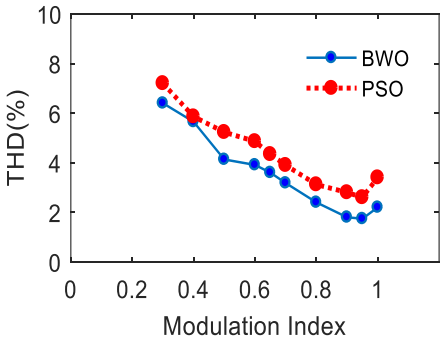


(b)

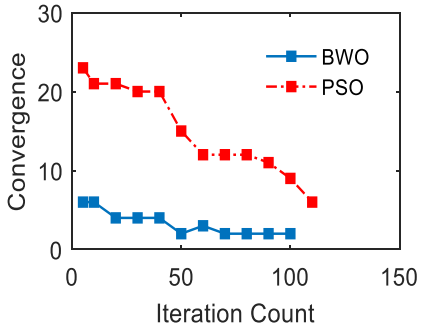


(c)

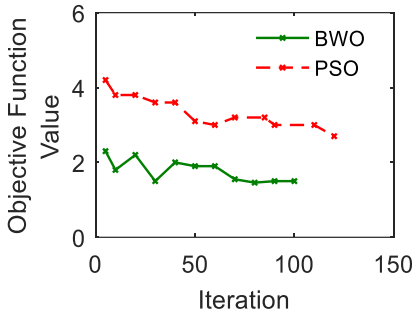
Figure 7.10. (a) Optimum switching angles vs Modulation index, (b) 5th order and 7th order harmonic voltages (% to fundamental) vs modulation index, (c) 11th order and 13th order harmonic voltages (% to fundamental) vs modulation index



(a)



(b)



(c)

Figure 7.11. Comparative study of BWO with PSO algorithm.(a) Overall Voltage THD vs Modulation Index, (b) Convergence vs Iteration count, (c) Objective Function value vs Iteration

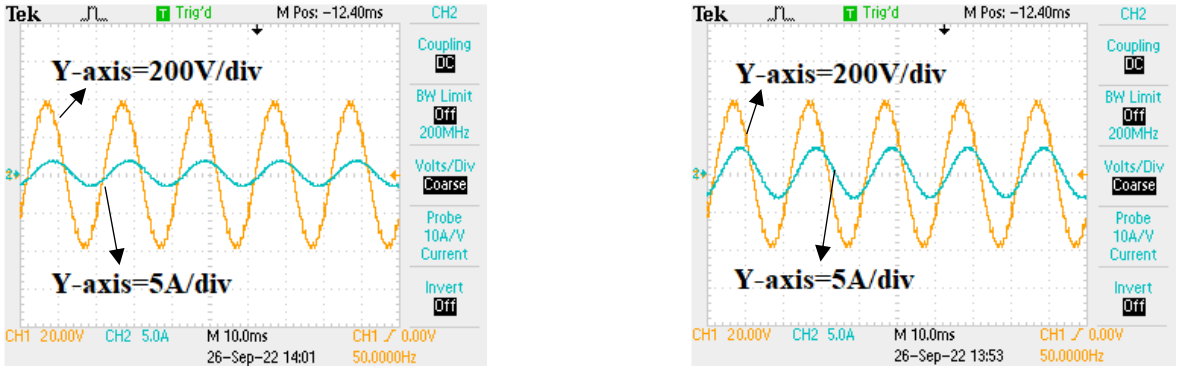
7.5 EXPERIMENTAL RESULTS

According to Table 7.2, the three voltage sources to the MLI are adjusted to 10, 20, and 60 Volts to provide the 19-level output voltage. The components used to design the prototype of the proposed MLI are cited in Table 7.5. Figure 7.12 (a) and 7.12(b) demonstrate, respectively, the dynamic behavior of the line voltage and load current waveforms. Real-time simulators are used to test the proposed MLI's functionality for grid applications. In figure 7.13(a) and 7.13(b), the grid voltage and synchronization with the MLI output voltage are reported.

Table 7.5. Component List

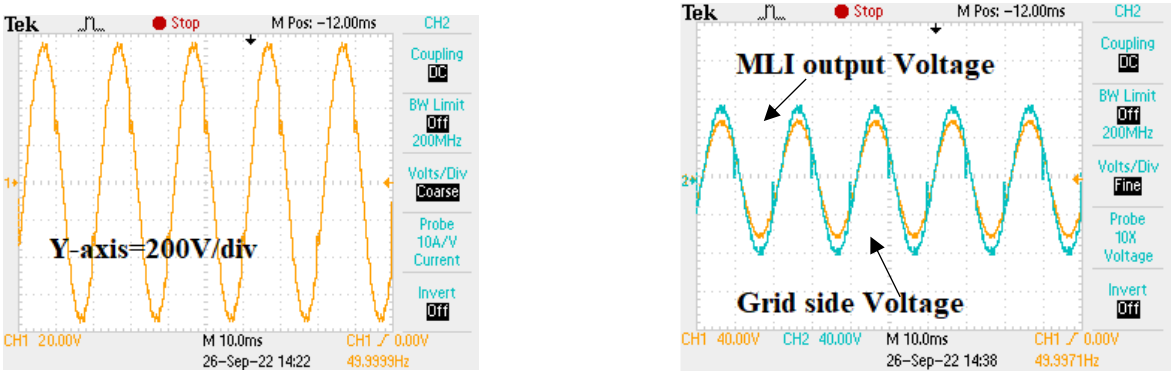
SI NO	COMPONENTS	
1	Optocoupler (Driver Circuit)	TLP250H
2	Microcontroller	PIC18f452
3	IGBT (11)	IE15AB
4	Load	R= 100Ω, L= 25mH
5	DSO	TDS 2022B
6	RT simulator	OPALRT-5650

The harmonic spectrum of line voltage, load current and grid voltage waveforms are shown in figure 7.14.



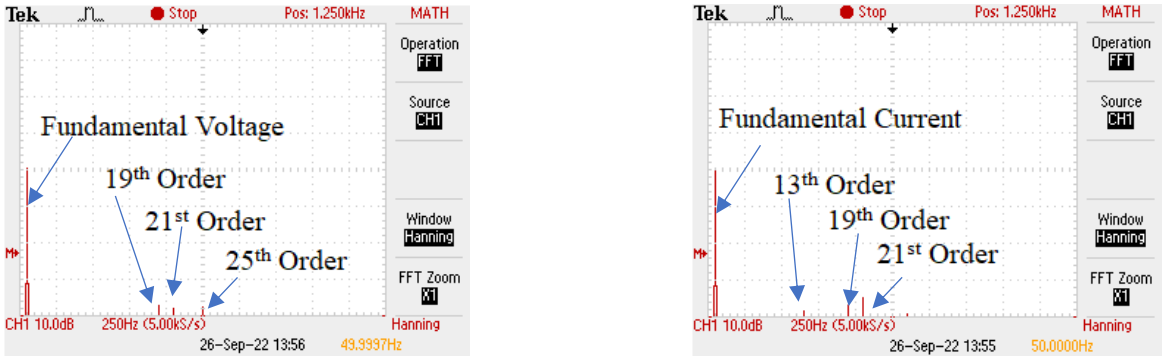
(a) (b)

Figure 7.12. Line Voltage and load current (a) at normal loading, (b) at 50% increased of loading

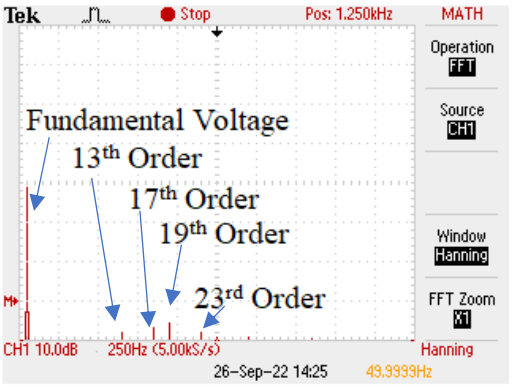


(a) (b)

Figure 7.13. Grid Output (a) Grid Voltage, (b) Syncronized MLI and Grid voltages



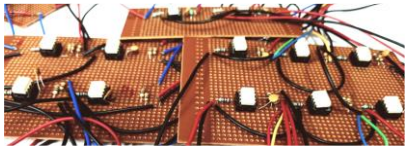
(a) (b)



(c)

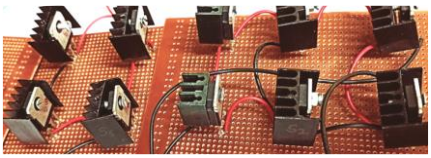
Figure 7.14 Harmonic spectrum (a) MLI line voltage, (b) Load current, (c) Grid connected MLI Voltage

The picture of laboratory setup for hardware model and for OPALRT software are shown in figure 7. 15.



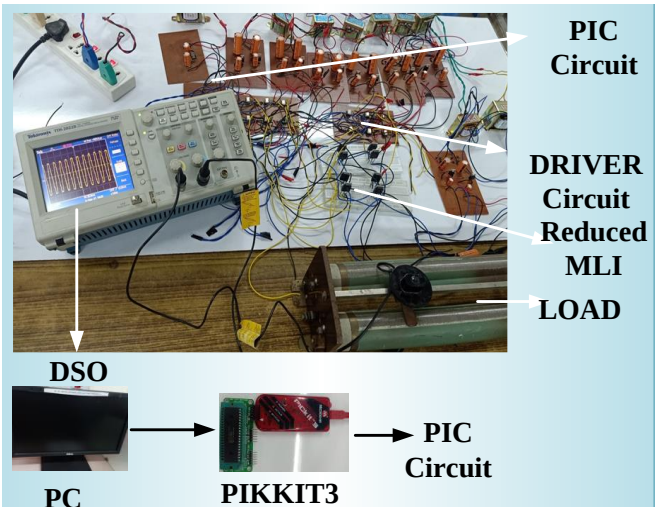
TLP-250H Optocoupler based Driver Circuit

(a)

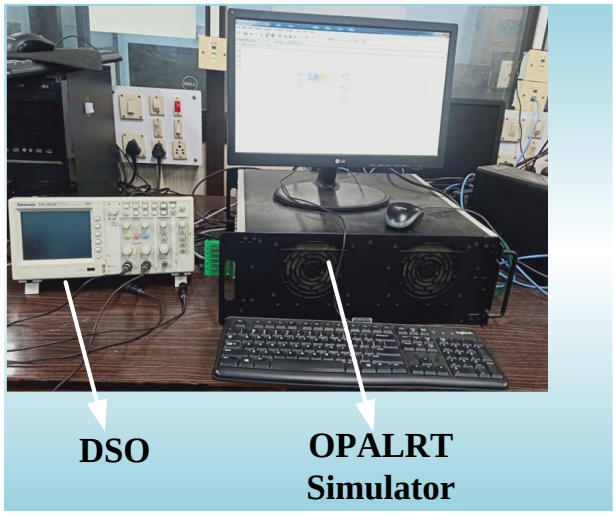


MLI Power Switches

(b)



(c)



(d)

Figure 7.15. Hardware setup pictures (a) Driver Circuit, (b) MLI circuit, (c) Experimental setup, (d) OPALRT laboratory setup

7.6 OBSERVATION

The proposed S-Cross switch MLI's performance is examined in hardware and simulation for both off-grid and grid-connected modes. Eleven switches are sufficient for generating 19 level output voltage which is less than the existing equivalent level MLIs. This proposed MLI has inherent low output voltage THD which is further reduced through switching angle optimization. To achieve the ideal switching angles, the BWO algorithm with modified steps is used. The comparison research with the conventional most commonly used method, such as PSO over a wide range of modulation index, shows the aforementioned algorithm's proficiency in solving the THD minimization problem. BWO has achieved 1.96% voltage THD with faster convergence rate at 0.92 modulation index, where PSO has obtained 2.68% voltage THD at the same modulation index. Similar results are also obtained over a wide range of modulation indices. The obtained output voltage THD for grid-integrated operation of the proposed MLI is 2.48%, which is well within the IEEE-519 standard.

7.7 REFERENCES

[7.1] R. Agrawal and S. Jain, “Multilevel inverter for interfacing renewable energy sources with low/medium- and highvoltage grids,” *IET Renew. Power Gener.*, vol. 11, no. 14, pp. 1822–1831, 2017, doi: 10.1049/iet-rpg.2016.1034.

[7.2] M. A. Hosseinzadeh, M. Sarebanzadeh, M. Rivera, E. Babaei, and P. Wheeler, “A Reduced Single-Phase Switched-Diode Cascaded Multilevel Inverter,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 3, pp. 3556–3569, 2021, doi: 10.1109/JESTPE.2020.3010793.

[7.3] E. Samadaei, M. Kaviani, and K. Bertilsson, “A 13-Levels Module (K-Type) With Two DC Sources for Multilevel Inverters,” vol. 66, no. 7, pp. 5186–5196, 2019.

[7.4] H. Vahedi, S. Member, M. Sharifzadeh, and S. Member, “Modified Seven-Level Pack U-Cell Inverter for Photovoltaic Applications,” vol. 6, no. 3, pp. 1508–1516, 2018.

[7.5] M. F. Kangarlu and E. Babaei, “Cross-switched multilevel inverter: An innovative topology,” *IET Power Electron.*, vol. 6, no. 4, pp. 642–651, 2013, doi: 10.1049/iet-pel.2012.0265.

[7.6] H. Zhao, S. Wang, and A. Moeini, “Critical Parameter Design for a Cascaded H-Bridge with Selective Harmonic Elimination/Compensation Based on Harmonic Envelope Analysis for Single-Phase Systems,” *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2914–2925, 2019, doi: 10.1109/TIE.2018.2842759.

[7.7] H. Khoun-jahan, A. M. Shotorbani, M. Abapour, and K. Zare, “Switched Capacitor Based Cascaded Half-Bridge Multilevel Inverter With Voltage Boosting Feature,” vol. 6, no. 1, pp. 63–73, 2021.

[7.8] S. Haq *et al.*, “An Advanced PWM Technique for MMC Inverter Based Grid-Connected Photovoltaic Systems,” vol. 31, no. 8, pp. 8–12, 2021.s

[7.9] R. N. Ray, D. Chatterjee, and S. K. Goswami, “Harmonics elimination in a multilevel inverter using the particle swarm optimisation technique,” *IET Power Electron.*, vol. 2, no. 6, pp. 646–652, 2009, doi: 10.1049/iet-pel.2008.0180.

[7.10] V. K. Gupta and R. Mahanty, “Optimized switching scheme of cascaded H-bridge multilevel inverter using PSO,” *Int. J. Electr. Power Energy Syst.*, vol. 64, pp. 699–707, 2015, doi: 10.1016/j.ijepes.2014.07.072.

[7.11] M. Tarafdar Hagh, H. Taghizadeh, and K. Razi, “Harmonic minimization in multilevel inverters using modified species-based particle swarm optimization,” *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2259–2267, 2009, doi: 10.1109/TPEL.2009.2022166.

[7.12] K. P. Panda and G. Panda, “Application of swarm optimisation-based modified algorithm for selective harmonic elimination in reduced switch count multilevel inverter,” *IET Power Electron.*, vol. 11, no. 8, pp. 1472–1482, 2018, doi: 10.1049/iet-pel.2017.0697.

[7.13] A. Routray, R. K. Singh, and R. Mahanty, “Harmonic Reduction in Hybrid Cascaded Multilevel Inverter Using Modified Grey Wolf Optimization,” *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 1827–1838, 2020, doi: 10.1109/TIA.2019.2957252.

[7.14] E. Babaei and S. H. Hosseini, “New cascaded multilevel inverter topology with minimum number of switches,” *Energy Convers. Manag.*, vol. 50, no. 11, pp. 2761–2767, 2009, doi: 10.1016/j.enconman.2009.06.032.

[7.15] E. Babaei, M. Farhadi, and M. Sabahi, “Cascaded multilevel inverter using sub-multilevel cells,” *Electr. Power Syst. Res.*, vol. 96, pp. 101–110, 2013, doi: 10.1016/j.epsr.2012.10.010.

[7.16] E. Najafi and A. H. M. Yatim, “Design and implementation of a new multilevel inverter topology,” *IEEE Trans. Ind. Electron.*, vol. 59, no. 11, pp. 4148–4154, 2012, doi: 10.1109/TIE.2011.2176691.

[7.17] V. Hayyolalam and A. A. Pourhaji Kazem, “Black Widow Optimization Algorithm: A novel meta-heuristic approach for solving engineering optimization problems,” *Eng. Appl. Artif. Intell.*, vol. 87, no. September 2019, p. 103249, 2020, doi: 10.1016/j.engappai.2019.103249.

[7.18] Y. Suresh and A. Kumar, “Investigation on hybrid cascaded multilevel inverter with reduced dc sources,” *Renew. Sustain. Energy Rev.*, vol. 26, pp. 49–59, 2013, doi: 10.1016/j.rser.2013.04.027.

[7.19] D. Chatterjee, “A novel magnetizing-curve identification and computer storage technique for induction machines suitable for online application,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 12, pp. 5336–5343, 2011, doi: 10.1109/TIE.2011.2126539.

8. Conclusion

8.1 SUMMARY ON THE THESIS WORK

This thesis discusses several Multilevel Inverter topologies, their functioning, and switching control methods. The application of MLI for PV-grid integration and PV standalone system with efficient power conversion are presented. Discussion is held regarding MLI topologies, their drawbacks, and methods for getting around those drawbacks by having access to other input sources. The optimisation of switching angles is carried out by various nature-inspired algorithms in order to lower the distortion of output voltage and current below 5% by reduced count MLI. The following is a description of this thesis' contributions.

a- The performance of an 11-level reduced switch MLI has been studied and simulated using the Particle Swarm Optimization algorithm. Implementation of PSO algorithm increases the power conversion efficiency by reducing the output voltage THD to 4.8%. The switching loss calculation and the overall efficiency of the converter has been determined and compared with the conventional CHBMLI.

b- A proposed PV-Grid integration approach based on reduced switch MLI is given. Using an isolated multi-winding DC-DC converter, a single PV panel serves as the MLI's input source. The system is cost-effective and compact because to the use of asymmetrical DC sources, which decreased the number of switching devices and input sources. Using the effective metaheuristic algorithm known as the Black Widow Optimization algorithm, optimal switching angles are determined. Comparative analysis with other swarm-based algorithms serves to demonstrate the offered algorithm's proficiency.

c- Proposed an asymmetrical MLI for PV standalone system. The MLI uses minimum number of power switches in comparison to the other developed topologies. To minimize the voltage distortion a modified JAYA algorithm is proposed. The proposed algorithm limits the output voltage THD to 2.23%.

d- A single PV source based reduced H-bridge MLI for grid interface is proposed. The multi input sources to the MLI are provided with the help of series capacitors connected across the PV voltage. The optimum value of switching angles and capacitance ratios

are determined using Red Deer Optimization algorithm in order to reduce the harmonic content across output. Piecewise mixed model equations are used for online control of switching angles due to variation of output voltage.

e- An asymmetrical CHBMLI for grid integration is proposed. The MLI is designed with two DC voltage sources and eight power switches to develop a nine-level output voltage. To generate a minimum distorted voltage waveform, Honey Badger Optimization algorithm is implemented. This algorithm provides faster convergence due to its exploration and exploitation behaviour of searching. The effectiveness of the proposed algorithm to solve the harmonic minimization problem is studied by real time simulation and hardware model of the asymmetrical MLI.

f- Proposed a S-Cross reduced switch based MLI with unequal DC sources. The three voltage sources of ratios 1:2:6 has been used to develop 19-level output voltage with minimum voltage distortion. The proposed MLI is interfaced with grid by implementing suitable control scheme. The performance of the proposed MLI has been verified with grid connection through real time simulator and off grid through a hardware prototype. The presented MLI with BWO algorithm minimizes the voltage THD that satisfies the IEEE standard.

The comparative study of the above proposed MLI topologies with their switching techniques and requirement of devices is shown in Table 8.1. According to the requirement of industrial application or efficient energy conversion of PV sources the data given in the table will be helpful to choose the appropriate topology.

Table 8.1. Comparative study of proposed different MLI topologies

MLI Topology	Optimization Algorithm for switching	Output Voltage level	Input DC sources	No of power Switches	No of Diodes	No of driver circuits	Output Voltage THD (%)	Application
Asymmetrical CSMLI	Black Widow Optimization	$2N(N-2)+7$	*N*	*2*(N+1)*	Nil	*2*(N+1)*	2.27	PV-Grid Integration
HybMLI	Modified JAYA	$2^{N+1}-1$	*N*	*2*(N+1)*	Nil	*2*(N+1)*	2.23	PV standalone system
Reduced H-bridge MLI	Red Deer Optimization	*2*N+1*	*N*	*4+N*	N-1	*4+N*	3.52	PV-Grid Integration (Low Voltage)
Asymmetrical CHBMLI	Honey Badger Optimization	3^N	*N*	*4*N*	Nil	*4*N*	2.48	Grid Integration
S-Cross MLI	Reduced step BWO	$3(2^N-1)$	*N*	$4N-1$	Nil	$4N-1$	1.96	Grid Integration

8.2 FUTURE WORK

Application of different reduced MLI topologies for PV standalone system and PV-grid synchronization is presented in this thesis. Some new topology with unequal voltage sources of different combination is also proposed. To minimize the voltage harmonics across output of the MLI, some metaheuristic algorithms and modified search-based algorithms are implemented. The further work that to be carried out are mentioned below.

1- Suitable control scheme can be implemented to HybMLI for PV grid integration.
2- Proper capacitor voltage balancing control technique can be implemented for reduced H-bridge MLI to use it in medium/high voltage grid.

3- S-Cross MLI with modified structure can be used for PV-grid synchronization of higher voltage level.
4- Advanced or efficient algorithm can be implemented to reduce the output voltage THD with faster convergence and minimum computational cost.