Development of Improved MLI Topology with Low Switching Loss and Low Output Voltage Harmonics Suitable For PV-Grid Integration

Abstract: This thesis proposes reduced switched multilevel inverters with minimum power loss and minimum voltage distortion. In order to integrate solar power with high or medium voltage grids an isolated multilevel inverter with asymmetrical DC sources has been developed. Isolating and decreasing energy sources is achieved in this setup by using a single photovoltaic (PV) panel coupled with a multi-winding flyback converter to power the MLI. A **13-level** output voltage has been generated by using **3 input sources of ratios 1:3:2 and 8 power switches** for the cross switched MLI. The proposed topology obtained **2.27% voltage THD** across output with the help of BWO algorithm. For PV standalone systems, a hybridised reduced switch MLI is designed to generate a greater output voltage level using a smaller set of power switches and a smaller set of input voltage sources. This proposed topology can generate **15-level output voltage with 3 input sources and 8 power devices**. The conventional JAYA algorithm is modified and proposed for deriving the optimum switching angles for the developed MLI in order to achieve the lowest voltage THD. The proposed method reduces the produced MLI output **voltage THD to 2.23%**, satisfying IEEE standard-519 requirements. A modified structure of reduced H-bridge Multilevel inverter is proposed for PV-grid synchronization using **single PV panel per phase**. This has been achieved by connecting series capacitors of different ration across the PV panel. An **11-level MLI** has been designed with **5 capacitors of unequal values**, PV boost converter regulated by PI controller and 9 power switches. Unequal capacitors provide asymmetrical input voltages across MLI to generate output voltage of uneven grading. To obtain minimum THD across output the suitable switching angles and optimum capacitors ratios for the proposed MLI are derived using Red Deer Optimization algorithm. This nature inspired algorithm minimizes the **output voltage THD to 3.52%** and **grid side voltage to 2.33% after integration**. This topology with single PV panel has been designed for low voltage application. For effective power conversion and grid application, cascaded H-bridge MLI with asymmetrical voltage sources is constructed utilising a computationally efficient method that is inspired by **Honey Badger foraging behaviours**. This effective algorithm expedites the process by avoiding confinement in the local optima. **8 power switches, 2 DC sources with a ratio of 1:3,** and an appropriate

switching combination are used to create a **9-level CHBMLI**. In order to achieve the minimum voltage distortion at grid side after integrating with MLI voltage, the voltage frequency control technique has been adopted in this research. This MLI topology with proposed switching scheme has been employed successfully for synchronization with grid of 415V. The MLI output voltage **THD is reduced to 2.48%** with minimum computational time by adopting Honey Badger Optimization Algorithm. After taking into account DC sources with adequate ratings, the suggested method can be used to create grid integrated converters up to a medium power level of 100 kW at LV (Low Voltage) distribution. An asymmetrical DC source based reduced structure Multilevel inverter named S-Cross MLI is proposed to generate higher voltage level by suitable combination of input voltage sources as per the requirement. By cascading the **S-switch pattern and cross switch pattern** the proposed MLI can develop higher voltage level with smaller number of power devices than the other presented topologies which is suitable for grid synchronization with better reliability. This MLI topology has generated **19- level output voltage** with the help of **3 DC voltage sources** and **11 power switches**. Optimum switching angles for the proposed MLI are derived from the **modified Black Widow Optimization** which achieved the lowest output voltage THD with minimum time and minimum steps. The proposed MLI is implemented for grid integration using suitable control scheme to verify the efficiency of the S-Cross MLI and modified BWO algorithm as well. The proposed modified BWO algorithm reduces the **MLI voltage THD to 1.96%** and synchronised **grid output voltage to 2.48%**.

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