Simulation and Analytical Modeling of Various Nano TFET Structures for Performance Improvement and Validation with Circuits

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2023

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Registration no:1021907001
Ref.No:D-7/E/223/19
Dated April 29, 2019
Exam Roll No: PHDETC20103
Class Roll No:101910705003

.

1. Title of the Thesis:
Simulation and Analytical Modeling of Various Nano TFET Structures for Performance Improvement and Validation with Circuits

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List of Publications:

1. Journal Publications: (Total 9 Nos. including under review)

1. Disha Bhattacharjee, **Bijoy Goswami,** Dinesh Kumar Dash, Ayan Bhattacharya and Subir Kumar Sarkar “Analytical modelling and simulation of drain doping engineered splitted drain structured TFET and its improved performance in subduing ambipolar effect” IET Circuits, Devices & Systems (Volume: 13, Issue: 6, 9 2019), Page(s): 888 – 895, DOI: 10.1049/iet-cds.2018.5261

2. Swarnav Mukhopadhyay, Dipanjan Sen, **Bijoy Goswami**, Subir Kumar Sarkar, "*Performance Evaluation of Dielectrically Modulated Extended Gate Single cavity InGaAs/Si HTFET based Label-free Biosensor Considering Non-ideal Issues*" IEEE Sensors Journal (Volume: 21, Issue: 4, Feb.15, 15 2021) Page(s): 4739 – 4746 DOI: 10.1109/JSEN.2020.3033576
3. Dipanjan Sen, Arpan De, **Bijoy Goswami,** Sharmistha Shee, Subir Kumar Sarkar, "*Noise Immune Dielectric Modulated Dual Trench Transparent Gate Engineered MOSFET as a Label Free Biosensor: Proposal and Investigation*" *Journal of Computational Electronics* **20,** 2594–2603 (2021). https://doi.org/10.1007/s10825-021-01780-x.
4. Savio Jay Sengupta, **Bijoy Goswami**, Pritam Das, Subir Kumar Sarkar, "*A Noise Immune Double Suspended Gate MOSFET for Ultra-Low-Power Applications"* Silicon (2021). https://doi.org/10.1007/s12633-021-01283-1.
5. **Bijoy Goswami,** Sutanni Bhowmick, Wasim Riza and Subir Kumar Sarkar, *"Analytical Current Modelling and Simulation of Double Trench Gate Covered Source-Channel TFET for Low-Power Applications."* Semiconductor Optoelectronics, (under print).
6. **Bijoy Goswami,** Debadipta Basak, Wasim Riza, and Subir Kumar Sarkar, *"Gate Centric Extended Source SOI TFET."* ADBU Journal of Engineering Technology, (under print).
7. **Bijoy Goswami**, Pritam Das, Savio Jay Sengupta, Wasim Reja, Subir Kumar Sarkar, *"Symmetrical Double Source SOI TFET for Low Power Circuit Application"* Submitted to International Journal of High-Speed Electronics and Systems, world scientific, June 2022(Waiting for Decision)
8. **Bijoy Goswami**, Savio Jay Sengupta, Pritam Das, Subir Kumar Sarkar, "*A Source-Drain Engineered Dielectrically Modulated Double Gate TFET Based Label-Free Biosensor for RF Applications"* Iranian Journal of Science and Technology, Transactions of Electrical Engineering May 2022 (Under Review)
9. **Bijoy Goswami**, Savio Jay Sengupta, Pritam Das, Subir Kumar Sarkar, "Innovative *Twin Channel TFET with reduced ambipolar conduction and suitable for Low Power Applications"* AEÜ - International Journal of Electronics and Communications, Elsevier, May 2023(Under Review).

2. Book Chapters: (Total 6 Nos)

1. **Bijoy Goswami**, Disha Bhattacharjee, Dinesh Kumar Dash, Ayan Bhattacharya, and Subir Kumar Sarkar "Drain Doping Engineering and its influence on Device Output Characteristics and Ambipolar Conduction on a Splitted-Drain TFET model" Springer Nature Singapore Pte Ltd 2019, "Advances in Communication, Devices and Networking" DOI 10.1007/978-981-13-3450-4 ISBN 9789811334504 (online) 9789811334498 (print)
2. **Bijoy Goswami,** Sutanni Bhowmick, Arindam Halder, Debadipta Basak, Goutika Paul, and Subir Kumar Sarkar "*Implementation of L-shaped Double Metal Dual Gate TFET towards Improved Performance Characteristics and Reduced Ambipolarity*" Springer Nature Singapore Pte Ltd. "Information, Photonics and Communication" DOI 10.1007/978-981-32-9453-0
3. Dipanjan Sen, Savio Jay Sengupta, Abhishek Sharma, Wasim Reja**, Bijoy Goswami** & SubirKumar Sarkar "*A Novel Approach for RFID Based Smart EVM System"*, Springer Nature Singapore Pte Ltd. 2020, Lecture Note Electrical Engineering, DOI: 10.1007/978-981-15-5262-5_49
4. Anup Dey, Komal Kumari, Abir Jana, **Bijoy Goswami**, Poushali Nandi and S. K. Sarkar *"Room temperature Pt modified WO3/p-Si Film Gas Sensor for Detection of Methanol"* Springer Nature Singapore Pte Ltd 2020, Smart Trends in Computing and Communications: Proceedings of SmartCom 2020. DOI: 10.1007/978-981-15-5224-3_19
5. Abir Jana, Disha Bhattacharjee, Komal Kumari, Anup Dey, **Bijoy Goswami**, Subir Kumar Sarkar, *"Designing Memristor Based Timing Circuits and Performance Comparison with CMOS Counterparts"* Springer Nature Singapore Pte Ltd 2020, Smart Trends in Computing and Communications: Proceedings of SmartCom 2020, DOI: 10.1007/978-981-15-5224-3_26
6. Dipanjan Sen, **Bijoy Goswami,** Anup Dey and Subir Kumar Sarkar "*Performance Evaluation of Novel Channel Engineered Junctionless Double Gate MOSFET for Radiation Sensing and Low Power Circuit Application"* "Electrical and Electronic Devices, Circuits and Materials: Design and Applications 2020" CRC Taylor & Francis, DOI: https://doi.org/10.1201/97810030977

3. International/National Conference Publications: (Total 18 Nos.)

1. **Bijoy Goswami,** Savio Jay Sengupta, Wasim Reja, Pritam Das, Subir Kumar Sarkar **"***Validation of Input/Output characteristics of Symmetrical Double Source TFET device"* 2021 Devices for Integrated Circuit (DevIC), 19-20 May 2021**,** Kalyani**,** India, Publisher: IEEE, DOI: 10.1109/DevIC50843.2021.9455764
2. **Bijoy Goswami,** Pritam Das, Abhishek Dey; Savio Jay Sengupta, Subir Kumar Sarkar *"Trapezoidal Channel Double Gate Tunnel FET Suitable for better Scalability, Speed and Low Power Application"* 2021 Devices for Integrated Circuit (DevIC), 19-20 May 2021, Kalyani, India**,** Publisher: IEEE, DOI: 10.1109/DevIC50843.2021.9455811
3. Abhishek Roy, **Bijoy Goswami,** Ujjwal Dey, Debasish Gayen, Wasim Reja and Subir Kumar Sarkar, *"Impact of Trapezoidal Channel in Double-Gate Tunnel Field Effect Transistor on Ambipolar Conduction for Ultra-Low-Power Application"* The 17th IEEE International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON 2020), June 24th - 27th,2020, Phuket, Thailand,
4. Dipanjan Sen, **Bijoy Goswami**, Anup Dey, Priyanka Saha and Subir Kumar Sarkar *"Impact of Self-Heating and Nano-Gap Filling Factor on AlGaAs/GaAs Junction-Less DG-MOSFET Based Biosensor for Early-Stage Diagnostics*" 2020 IEEE Region 10 Symposium (TENSYMP), 5th -7th June 2020, Dhaka, Bangladesh.
5. Abir Jana, Disha Bhattacharjee, Komal Kumari, Anup Dey, **Bijoy Goswami**, Subir Kumar Sarkar *"Designing Memristor Based Timing Circuits and Performance Comparison with CMOS Counterparts"* in Fourth International Conference on Smart Trends for Computing & Communications (SmartCom 2020), January 24-25, 2020 at Hotel Novotel, Siam Square, Bangkok, Thailand
6. Anup Dey, Komal Kumari, Abir Jana, **Bijoy Goswami**, Poushali Nandi, S. K. Sarkar *"Room temperature Pt modified WO3/p-Si Film Gas Sensor for Detection of Methanol"* in Fourth International Conference on Smart Trends for Computing & Communications (SmartCom 2020), January 24-25, 2020 at Hotel Novotel, Siam Square, Bangkok, Thailand
7. **Bijoy Goswami,** Kousik Naskar, Sharmistha Shee kanra, Anup Day, Abir Jana and Subir Kumar Sarkar *"The Hypothesis of Two-Sources on TFET's Ambipolar Current and its Quantum Confinement Effect",* 2020 8th International Electrical Engineering Congress

(iEECON-2020),4-6 March 2020, Chiang Mai, Thailand, Publisher: IEEE, DOI:10.1109/iEECON48109.2020.229576,

8. **Bijoy Goswami,** Lavlesh Kumar Barman, Abir Jana, Anup Day, Wasim Reja and Subir Kumar Sarkar, *"A Source Pocket Doping in PNPN-DG TFET to Preclude Ambipolar Current– Two Dimensional Simulation*", 2020 8th International Electrical Engineering Congress (iEECON-2020),4-6 March 2020, Chiang Mai, Thailand. Publisher: IEEE, DOI: 10.1109/iEECON48109.2020.229575
9. **Bijoy Goswami,** Ayan Bhattacharya, Komal Kumari, Priyadarshini Das, Wasim Reja, and Subir Kumar Sarkar, ***"A Novel Double Source TFET for Low Power Application"*** 14th Conference on Industrial and Information Systems (ICIIS), 18-20 Dec. 2019, Kandy, Sri Lanka, Publisher: IEEE, DOI: 10.1109/ICIIS47346.2019.9063290, Print on Demand (PoD) ISSN: 2164-7011.
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11. **Bijoy Goswami,** Debadipta Basak, Koelgeet Kaur, Ayan Bhattacharya, Sutanni Bhowmick and Subir Kumar Sarkar, *"Reduction of Ambipolar Conduction in Centrally Aligned PNPN-DG TFET"***,** 16th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), 10-13 July 2019, Pattaya, Chonburi, Thailand, Publisher: IEEE, DOI: 10.1109/ECTI-CON47248.2019.8955417
12. **Bijoy Goswami,** Debadipta Basak, Ayan Bhattacharya, Koelgeet Kaur, Sutanni Bhowmick, Subir Kumar Sarkar *"Analytical Modeling and Simulation of Low Power Salient Source Double Gate TFET"***,** Devices for Integrated Circuits (DevIC 2019), Kalyani University, 23-24 March 2019, Publisher: IEEE
13. Goutika Paul, **Bijoy Goswami** and Subir Kumar Sarkar, *"H-shaped Double Gate Tunnel FET For Low Power Applications"* International Conference In Recent Trends on Electronics & Computer Science, (ICRTECS-2019) 18th-19th March 2019, NATIONAL INSTITUTE OF TECHNOLOGY SILCHAR
14. Mandira Biswas, Goutika Paul, **Bijoy Goswami,** and Subir Kumar Sarkar, *"PPV Based Bottom Gate Organic Field Effect Transistor (BGOFET)"* International Conference in Recent Trends on Electronics & Computer Science, (ICRTECS-2019) 18th-19th March 2019, NATIONAL INSTITUTE OF TECHNOLOGY SILCHAR.

15. **Bijoy Goswami**, Sutanni Bhowmick, Arindam Halder, Debadipta Basak, Goutika Paul, and Subir Kumar Sarkar, *"Implementation of L-shaped Double Metal Dual Gate TFET towards Improved Performance Characteristics and Reduced Ambipolarity*" in Information, Photonics and Communication 2019 (IPC'19) held in B. P. Poddar Institute of Management and Technology, Kolkata, 1st-3rd February 2019.
16. Disha Bhattacharjee, **Bijoy Goswami**, Dinesh Kumar Dash, Ayan Bhattacharya, Subir Kumar Sarkar *"Influence of Drain Doping Engineering in Triple Splitted-Drain TFET model"* International Conference on Recent Innovations in Electrical, Electronics & Communication Engineering -ICRIEECE". July 27th and 28th 2018, School of Electrical Engineering, Kalenga Institute of Industrial Technology (KIIT), Bhubaneswar, India. Publisher: IEEE
17. **Bijoy Goswami**, Disha Bhattacharjee, Dinesh Kumar Dash, Ayan Bhattacharya, Subir Kumar Sarkar *"Drain Doping Engineering and its influence on Device Output Characteristics and Ambipolar Conduction on a Splitted-Drain TFET model"* International Conference in Communication, Devices and Networking (ICCDN 2018) Sikkim Manipal Institute of Technology, Majhitar, Sikkim, 2-3rd June 2018.
18. **Bijoy Goswami**, Disha Bhattacharjee, Dinesh Kumar Dash, Ayan Bhattacharya, Subir Kumar Sarkar "Demonstration of T-Shaped Channel Tunnel Field-Effect Transistors" 2018 2nd International Conference on Electronics, Materials Engineering & Nano-Technology (IEMENTech), 4-5 May 2018, Publisher: IEEE, **DOI:** 10.1109/IEMENTECH.2018.8465213

4. List of Patents: -NIL-

5. List of Presentations at International Conferences: (Total 5 Nos)

1. "Validation of Input/Output characteristics of Symmetrical Double Source TFET device" 2021 Devices for Integrated Circuit (DevIC), 19-20 May 2021**, Kalyani**, India**,**

2. "Trapezoidal Channel Double Gate Tunnel FET Suitable for better Scalability, Speed and Low Power Application" 2021 Devices for Integrated Circuit (DevIC), 19-20 May 2021, **Kalyani**, India**.**

3. "*Impact of Trapezoidal Channel in Double-Gate Tunnel Field Effect Transistor on Ambipolar Conduction for Ultra Low-Power Application"* The 17th IEEE International

Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON 2020), 24-27 June 2020, Phuket, Thailand,

4. *"Reduction of Ambipolar Conduction in Centrally Aligned PNPN-DG TFET",* 16th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON) by IEEE, 10-13 July 2019, Pattaya, Chonburi, Thailand,

5. *"Demonstration of T-Shaped Channel Tunnel Field-Effect Transistors"* 2nd International Conference on Electronics, Materials Engineering & Nano-Technology (IEMENTech), 4-5 May 2018, KIIT, Odisha,

6. Best Presentation Awardee Paper:

1. *"Implementation of L-shaped Double Metal Dual Gate TFET towards Improved Performance Characteristics and Reduced Ambipolarity"* in Information, Photonics and Communication 2019 (IPC'19) held in B. P. Poddar Institute of Management and Technology, Kolkata, 1st-3rd February 2019.

“Statement of Originality”

*I Bijoy Goswami registered on 29/04/2019 do hereby declare that this thesis entitled “**Simulation and Analytical Modeling of Various Nano TFET Structures for Performance Improvement and Validation with Circuits**” contains a literature survey and original research work done by the undersigned candidate as part of Doctoral studies.*

All information in this thesis has been obtained and presented by existing academic rules and ethical conduct. I declare that, as required by these rules and conduct, I have fully cited and referred all materials and results that are not original to this work.

I also declare that I have checked this thesis as per the “Policy on Anti Plagiarism, Jadavpur University, 2019”, and the level of similarity as checked by Ternitin software is ***…7...%.***

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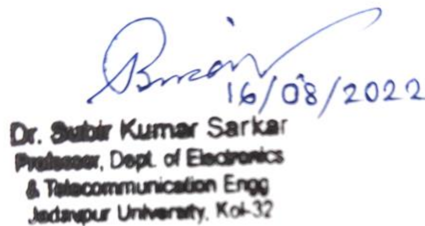

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DEDICATED TO

MY PARENTS
DR. BASANTA KUMAR DEVA GOSWAMI
MRS. USHA GOSWAMI
FOR THEIR UNCONDITIONAL SUPPORT
&
MY SPOUSE
MRS. KAKOLI SARMAH
FOR HER CONSTANT SUPPORT AND COOPERATION
AND
MY DAUGHTERS
MISS. DARSHITA GOSWAMI
&
MISS. JANVI GOSWAMI
TO SPARE ME ALL THE TIME FOR MY WORK

ACKNOWLEDGEMENT

I would like to extend my sincere appreciation and profound gratitude to my supervisor Prof. Subir Kumar Sarkar of Electronics and Telecommunication Engineering Department, Jadavpur University, for his invaluable guidance and constant encouragement in carrying out my research. I was allowed to enjoy all the necessary freedom in carrying out the research work and at the same time, the intense supervision by my supervisor helped me in significant enhancement of the quality of the research. This work could not have reached this stage without profiting from his expertise, encouragement, and valuable criticisms. I would also like to express my sincere gratitude towards him for his invaluable guidance towards my research and his active role in helping me with my overall personal and professional development.

I would like to thank FET and the Head of the Department, all the faculty members, and technical staff of the Department of Electronics and Tele-Communication Engineering, Jadavpur University for allowing me to carry on my research work.

I would extend special thanks to my fellow research scholars Dr. Koushik Naskar, Dr. Manas Ranjan Nayak, Dr. Subhashis Roy, Dr. Priyanka Saha, Dr. Anup Dey, Dr. Dinesh Kumar Dash, Mrs. Komal Kumari, Mrs. Devdipta Basak, Mr. Abir Jana, Miss Disha Bhattacharjee, Miss Sutanni Bhoumick, Mr. Ayan Bhattacharyya, Mr. Bikram Biswas for providing their continuous emotional support and for making the lab an interesting place.

I would also like to be thankful to the Principal, HoD, Dept. of ETE, Assam Engineering, Guwahati, and Govt. of Assam for allowing me to pursue a Ph.D. (Engg.) in Jadavpur University through the Quality Improvement Programme (QIP) Scheme by A.I.C.T.E. I would also like to thank my colleagues for providing enormous support in terms of sharing my academic load during the QIP period for the successful conduct of my research work.

I would express my love and respect towards my parents, my spouse, and my daughters Darshita and Janvi for their sacrifice, love, belief, never-ending support, and encouragement throughout this entire journey. I express my indebtedness to each and every one who rekindled the spark of research in me throughout this remarkable journey.

Finally, heartful thanks to everyone for whom this thesis would have seen the light of day.

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Abstract

In the last decade, there has been a gradual reduction in the dimension of the devices, and the reduction of dimension leads to the short channel effect in MOSFET. Researchers tried to overcome those short channel effects by incorporating geometrical modification of device structures including Silicon On Insulator (SOI) and Silicon On Nothing (SON) MOSFET which focused significant research limelight. Owing to the superior scalability and much reduced parasitic capacitive effects, they emerge as improved structures over traditional MOSFETs which exhibit higher circuit speed, better subthreshold behaviors, and subdued SCEs. However, in spite of all these benefits, SOI/SON technology faces two crucial challenges to further scaling. Firstly, the downscaling of the channel length causes the gate to lose its electrostatic control over the channel potential thus degrading the device electrostatics significantly. The second one being the most critical is the scaling constraint of supply voltage owing to the thermionic limitation of the steepness of sub-threshold swing which leads to increased power consumption.

That has created a path for a new type of device structure an innovative structure called TFET (Tunnelling Field–Effect Transistors) where we can overcome the short channel effect and we can reduce the power dissipation. The predominant benefit of TFETs is current conduction through modulation of quantum mechanical Band-to-Band Tunnelling (BTBT), which is a result of finite but non-zero probability of tunneling through a potential barrier, a process in which electrons tunnel from the valence band through the semiconductor bandgap to the conduction band or vice versa without any trap assistance. This attribute carries forward the advantages over the thermionic injection across an energy barrier for carrier transport in MOSFET. Thus, due to its built-in tunnel barrier, where the channel current in TFET is

controlled by the tunneling mechanism from the source, the TFET device is resistant to the short channel effect and allows TFETs to have SS as low as 25 mv/decade, which is a root cause of designing of low power devices. Again, it may be pointed out that TFETs differ from the MOSFET only in the type of source doping, so f the TFET fabrication process is not much different from the MOSFET fabrication process.

The primary constraints concerning TFET devices are ambipolar conduction which originates from the BTBT at the drain–channel junction and the other is low I_{ON}, which is considerably poorer than MOSFETs. Hence there is a need for a structural modification methodology that reduces the ambipolarity of TFETs without compromising the I_{ON} as well as improving SS has been to be introduced and examined by researchers. Various modifications such as the multi-gate device geometry e.g., double gate (DG), tri-gate (TG), quadruple gate (QG), gate all around (GAA) TFET have been to mitigate these limitations faced by the conventional TFET.

The aim of the work herein presented in this thesis is to explore the physical phenomena and mechanisms to be studied for a precise understanding and description of the different innovative TFET device structures. Identification of the existing limitations, incompatibilities, and problems that arise during simulation processes, using the SILVACO ATLAS. Use of a high-*k* gate dielectric or a low-*k* spacer to reduce the barrier at the source-channel interface boosting the tunneling current and keeping the bandgap in other regions large to subdue the ambipolar behaviour and elevate the I_{ON} of the conventional TFET. Development of analytical modeling to pursue a better comprehensive study of device physics for its further improvement. The analytical results obtained are further validated with relevant simulated data for substantiating the accuracy of the resultant model and facilitating implementation in low-power circuit-level analysis.

CONTENTS

Acknowledgments

Abstract

List of Figures v

List of Tables x

List of Abbreviations xi

Chapter-1: Introduction and Organization of Thesis 2

1.1 Introduction and Motivation 2
1.2 Literature Review 8
1.3 Organisation of the Thesis 11
References 14

Chapter-2: Basics of Semiconductor Devices 23

2.1 Introduction to Semiconductor Devices 23
2.1.1 Overview 0f Metal Oxide Semiconductor Field Effect Transistor (MOSFET) 24
2.1.2 Types of MOSFET 26
2.1.2.1 Enhancement mode MOSFET (e-MOSFET) 26
2.1.2.2 Depletion mode MOSFET or d-MOSFET 27
2.1.3 Operational regions of MOSFET 28
2 .1.4 Complementary Metal Oxide Semiconductor (CMOS) 31
2.1.5 Power Dissipation in CMOS 32
2.1.6 Issues with Scaling and Moor's law 34
2.1.7 Short Channel Effects in MOSFET 36
2.1.7.1 Drain Induced Barrier Lowering and Threshold voltage roll-off 36
2.1.7.2 Mobility Degradation (Surface Scattering) and Velocity Saturation 37
2.1.7.3 Impact Ionization 38
2.1.7.4 Hot carrier effect 39
2.1.7.5 Channel Length Modulation 40
2.1.7.6 Body Effect (Back Gate Effect) 40
2.1.7.7 Gate Tunneling 41
2.1.8. Evolution of advanced MOSFET structures 41
2.1.8.1 Silicon on Insulator (SOI) MOSFET 41
2.1.8.2 Silicon on Nothing (SON) MOSFET 43
2.1.8.3 Multi-gate MOSFET 44
2.1.8.4. Gate work function engineering: The emerging performance-boosting technique of scaled devices 45
2.2 Introduction to Tunnelling 46
2.2.1 A Brief Introduction to Band-to-Band Tunnelling 47
2.2.2 Band-to-Band Tunnelling Models 48

2.2.3 Basic Construction of TFET 50
2.2.4 Working Principle of TFET in Brief 50
2.2.5. Transfer characteristics of traditional TFET structures..52
2.2.5.1 Without any external bias 52
2.2.5.2 OFF State 53
2.2.5.2 In ON State 53
2.2.5.4 Pinning of Channel Potential 55
2.2.5.5 Ambipolarity in TFETs 56
2.3 A Brief Literature Review on various TFET Designs for Performance Enhancement.....57
2.3.1. Using multiple Gate Oxide Materials 57
2.3.2. Using Multiple Materials as Gate Metal 58
2.3.3 PNPN or NPNP TFET Structure 59
2.3.4 Raised Germanium Source Structure 59
2.3.5 Si-Ge Source UTFET 60
2.3.6 L-Shaped TFET (LTFET) 60
2.3.7 L-Shaped Gate TFET (LG-TFET) 61
2.3.8 Doping-less TFET 61
2.3.9 III-V Semiconductor Homo and Hetero-Junction TFETs 62
2.3.10 Ferroelectric TFETs 63
2.3.11 Phase Change TFET (PC-TFET) 64
2.3.12 Tri-Gate or Fin-TFET 65
2.3.13 Gate All Around TFET (GAA-TFET) 65
2.3.14 Carbon Nanotube and Graphene TFETs 66
Reference 67

Chapter-3: Drain Doping Engineered Splitted Drain TFET Structures to Improved Performance in Subduing Ambipolar Effect- An Analytical Modelling and Simulation 79

3.1 Introduction 79
3.2 Literature Survey 80
3.3 Device structure and Parameters 82
3.4 Analytical Modelling 84
3.4.1 Electric field 84
3.4.2 Potential distribution 85
3.4.3 Drain Current 86
3.5 Simulation Setup 88
3.6 Results and discussions 88
3.6.1 Potential and Electric Field Profile 88
3.6.2 Band Diagram Analysis 92
3.6.3 Optimization of Ambipolar Conductivity 93
3.6.4 Transfer Characteristics 94
3.6.5 Drain Output Characteristics 95
References 97

Chapter-4: Analytical Modelling and optimization of Double Trench Gate Covered TFET suitable for Low-Power Application 105

4.1 Introduction........105
4.2 Literature Review........107
4.3 Proposed Device Structure and its Parameters........109
4.4 Analytical Modeling........111
4.5 Device Structure and Simulation Setup........117
4.6 Results and Discussion........119
4.6.1 Voltage Optimization........119
4.6.2 Variation of Extended Source Length Ls........121
4.6.2.1 Energy Band Diagrams........121
4.6.2.2 Electric Field........123
4.6.2.3 Potential profile........124
4.6.3 Transfer Characteristics........125
4.6.4 Quantum Confinement Effect........126
4.7 DTG-CSC-TFET Inverter........128
References........131
Chapter-5: To Study the Impact of Source Pocket Doping in PNPN-DG TFET........136

5.1 Introduction........136
5.2 Literature Review........138
5.3 Incorporation of Centrally Aligned Source Pocket Region in TFET: 2D- Modeling and Simulation-Based Performance Assessment........140
5.3.1 Device Structure of a CA-PNPN-DG TFET........140
5.3.2 Analytical Model........141
5.3.3 Results and Discussions........146
5.3.3.1 Potential Distribution........146
5.3.3.2 Electric Field Distribution........148
5.3.3.3 Conduction Band and Valence Band Energy........149
5.3.3.4 Transfer Characteristics........150
5.4. Incorporation of two symmetric pockets at Source Region in TFET: 2D-Modeling and Simulation-Based Performance Assessment........150
5.4.1 Device Structure of a TB-PNPN-DG TFET........150
5.4.2 Analytical Model........151
5.4.3 Results and Discussions........155
5.4.3.1 Potential Distribution........155
5.4.3.2 Electric Field Distribution........157
5.4.3.3 Conduction and Valence Band Energy........158
5.4.3.3 Transfer Characteristics........159
5.5 Comparison........159
5.6 Frequency Analysis........160
5.7 Circuit Design........162
References........164

Chapter-6: Investigating Ambipolar Current and Quantum Confinement Effect in Two-Source TFET........171

6.1 Introduction........171
6.2 Literature Survey........172

6.3 Device structure and Parameters....175
6.4 Results and Discussion....177
6.4.1 Transfer Characteristics of propose TFETs for Various Channel length....177
6.4.2 Variation of Oxide Thickness....178
6.4.3 Variation of Gate Work Function....179
6.4.4 Total Current Density & Band to Band Tunneling(BTBT)....180
6.4.5 Output Characteristics of proposed DSS-TFETs....181
6.5 Circuit-level Analysis....182
References....189
Chapter-7: Gate Centric Extended Source SOI-TFET for Low Power Circuit Application ... 196

7.1 Introduction....196
7.2 Literature Survey....198
7.3 Device Structures and Parameters....201
7.4 Simulation Setup And Model Descriptions....202
7.5 Tunneling Mechanism....203
7.5.1 Point Tunneling....203
7.5.2 Line Tunneling....205
7.6 Results and Discussions....207
7.6.1 Optimum VDS....207
7.6.2 Centric Source Extension....208
7.6.3 Position of Source and Drain Contact....208
7.6.4 Band Diagram....209
7.6.5 Electric Field....209
7.6.6 Surface Potential....210
7.6.7 Transfer Characteristics....210
7.7 Quantum Confinement....211
7.7.1 Transfer Characteristics....211
7.7.2 Electron Concentration....212
7.7.3 Comparison of Subthreshold Slope....213
7.8 GCES SOI TFET Inverter....214
References....216
Chapter-8: Concluding Remarks and Future Scope....219

8.1. Concluding Remarks....219
8.2 Future scope....222

LIST OF FIGURES

Figure 2.1: Basic MOSFET structure 24
Figure 2.2: n-channel MOSFET schematic representation........ 25
Figure 2.3: (a) n-channel Enhancement mode MOSFET (b) I_{DS}-V_{GS} characteristics (c) I_{DS}-V_{DS} of n-channel Enhancement mode MOSFET 26
Figure 2.4: (a) Depletion mode MOSFET (b) I_{DS}-V_{GS} characteristics (c) I_{DS}-V_{DS} characteristics of Depletion mode MOSFET........ 27
Figure 2.5:(a) MOSFET driven by a gate voltage; (b) depletion region formation; (c) onset of inversion (d) inversion layer formation........ 29
Figure 2.6: Illustration of different regions of operation in drain current characteristics of MOSFET........ 30
Figure2.7: Representation of Complementary Metal Oxide Semiconductor (CMOS)........ 31
Figure 2.8: Representation of (a) CMOS Circuit Configuration (b) Transfer Characteristic (c) CMOS inverter current vs Vin 31
Figure 2.9: Representation of MOSFET Power consumption factor with respect to channel length 32
Figure 2.10: Current flows via MOS Circuit........ 33
Figure 2.11: (a) Scaling rule; (b) Scaling trend of the supply voltage........ 34
Figure 2.12: Transistor Density, Power Limit, Frequency Limit with respect to Scaling of an IC 35
Figure 2.13: Logic device and Shrinking roadmap 36
Figure 2.14: Variation of surface potential along channel position........ 37
Figure 2.15: Electrons effective path due to surface scattering........ 38
Figure 2.16: Comparison of in short-channel and long-channel device at the onset of saturation........ 38
Figure 2.17: Schematic illustration of the impact ionization in an N-MOSFET........ 39
Figure 2.18: Schematic illustration of carriers being injected into the gate dielec- tric........ 39
Figure 2.19: Channel length modulation [4] 40
Figure 2.20: Schematic illustration of Body effect [4]........ 41
Figure 2.21: Cross-sectional representation of SOI MOSFET........ 42
Figure 2.22: Cross-sectional view of (a) PD-SOI MOSFET(b) FD-SOI MOSFET........ 43
Figure 2.23: Cross-sectional view of SON MOSFET structure 44
Figure 2.24: (a) The amplitude of the emerging EMW is insignificant (b) The amplitude of the incoming EMW is reduced, but not to zero 47
Figure 2.25: Visualization of Band-to-band Tunnelling........ 47
Figure 2.26: Tunnelling under application of the electric field........ 49
Figure 2.27: Comparison between basic MOSFET and TFET Structure........ 50
Figure 2.28: Visualization of Line and Point Tunnelling 51
Figure 2.29: Energy Band Diagram of n-TFET........ 52
Figure 2.30. At zero bias, n-channel TFET’s band structure at the surface 52
Figure 2.31. Band diagram of a TFET in the OFF-state (VGS = 0 V)........ 53
Figure 2.32 (a) At the start of ON state (b) ON state at higher VGS 54
Figure 2.33: Channel Pinning in N-TFET........ 55

Figure.2.34: Energy Band Diagram of n-TFET during ambipolar conduction at positive drain bias 56
Figure.2.35: Transfer Characteristic of n-TFET 57
Figure 3.1. Device Structure of (a) Splitted-Drain Single-Gate TFET (SD-SG TFET),(b) Top-Splitted-Drain Single-Gate TFET (TSD-SG TFET), (c) Mesial-Splitted-Drain Single-Gate TFET (MSD-SG TFET) and (d) Basal-Splitted-Drain Single-Gate TFET (BSD-SG TFET) 82
Figure 3.2. Approximation of space charge distribution 84
Figure 3.3. Simulated and analytical Potential profile (V) of SD-SG TFET w.r.t distance along horizontal direction (µm) 87
Figure 3.4. Net absolute doping in the SD-SG TFET under ON state 88
Figure 3.5. Potential Distribution profile of(a) Splitted-Drain Single-Gate TFET (SD-SG TFET),(b) Top-Splitted-Drain Single-Gate TFET (TSD-SG TFET), (c) Mesial-Splitted-Drain Single-Gate TFET (MSD-SG TFET), and (d) Basal-Splitted-Drain Single-Gate TFET (BSD-SG TFET) 89
Figure 3.6. Electric Field distribution Profile of (a) Splitted-Drain Single-Gate TFET (SD-SG TFET),(b) Top-Splitted-Drain Single-Gate TFET (TSD-SG TFET), (c) Mesial-Splitted-Drain Single-Gate TFET (MSD-SG TFET) and (d) Basal-Splitted-Drain Single-Gate TFET (BSD-SG TFET) 90
Figure 3.7. Comparative Plot of Potential distribution graph of SD-SG TFET, TSD-SG TFET, MSD-SG TFET and BSD-SG TFET w.r.t distance along horizontal direction (µm) 91
Figure 3.8. Comparative Plot of electric field distribution graph of SD-SG TFET, TSD-SG TFET, MSD-SG TFET and BSD-SG TFET w.r.t distance along horizontal direction (µm) 91
Figure 3.9. Comparative Plot of Density of states switch of energy band diagram (eV) (conduction and valence band) of SD-SG TFET, TSD-SG TFET, MSD-SG TFET and BSD-SG TFET w.r.t distance along horizontal direction (µm) 92
Figure 3.10. Comparative Plot of Density of states switch of energy band diagram (conduction and valence band) for width modulation of highly doped upper drain region D1, for width Yd1=20nm, Yd1=30nm, Yd1=15nm w.r.t distance along horizontal direction (µm) 93
Figure 3.11. Comparative Plot of (a) linear and (b) log transfer characteristics of SD-SG TFET, TSD-SG TFET, MSD-SG TFET and BSD-SG TFET for Vds=0.5V 94
Figure 3.12. Drain Characteristics of (a) Splitted-Drain Single-Gate TFET (SD-SG TFET),(b) Top-Splitted-Drain Single-Gate TFET (TSD-SG TFET), (c) Mesial-Splitted-Drain Single-Gate TFET (MSD-SG TFET) and (d) Basal-Splitted-Drain Single-Gate TFET (BSD-SG TFET) 95
Figure 3.13. Comparative Plot of drain output characteristics of the proposed models and conventional TFETs 96
Figure 4.1. Schematic of the proposed DTG-CSC-TFET 110
Figure 4.2. Direction of Point Tunneling and Line Tunneling 112
Figure 4.3. Cutline shown for quantifying Line tunneling, where ymax represents the depletion region when positive gate bias is applied for the proposed n-DTG-CSC-TFET 115
Figure 4.4. Band Diagram along cutline AA’ of Figure 4.3. depicting wtun 116
Figure 4.5. Absolute net doping profile for DTG-CSC-TFET for (a) LS=10nm, (b) LS=15nm, (c) LS=20nm 118
Figure 4.6. (a) - (f) Steps for the fabrication of the proposed DTG-CSC-TFET 118
Figure 4.7. Bar graph for comparing the approximate $I_{ON}/I_{OF}F$ ratios of the three structural variations (LS = 10nm, 15nm, 20nm) 119

Figure 4.8 (a) Bar graph for comparing the Subthreshold Swing (SS) of the three structural variations (LS = 10nm, 15nm, 20nm). (b) Bar graph for comparing the Threshold Voltage (Vth) of the three structural variations (LS = 10nm, 15nm, 20nm). 120
Figure 4.9 (a) Comparison of the Energy Band Diagrams of the three structural variations (LS = 10nm, 15nm, 20nm) for DTG-CSC-TFET. (b) Comparison of the Energy Band Diagrams for cutline 1 and cutline 2 for LS = 15nm.. 121
Figure 4.10. The contour diagram of the BTBT rates for cutline 1 and cutline 2.................. 122
Figure 4.11. (a) Comparison of the Electric Fields of the three structural variations (LS = 10nm, 15nm, 20nm) for DTG-CSC-TFET. (b) Comparison of the Electric Fields for cutline 1 and cutline 2 for LS = 20nm. (b) shows the electric field for cutline 1 & cutline 2 for the sake of comparison. It is clear that the peak overshoot is higher for the cutline 1 than for cutline 2, indicating greater degree of tunneling for the former. 123
Figure 4.12. (a) Comparison of the Potential Profile of the three structural variations (LS = 10nm, 15nm, 20nm) for DTG-CSC-TFET. (b) Comparison of the Potential Profile for cutline 1 and cutline 2 for LS = 20nm 124
Figure 4.13. Log Scale plot of Transfer Characteristics for the DTG-CSC-TFET for the three structural variations (LS = 10nm, 15nm, 20nm)... 125
Figure 4.14. Simulation based validation of the Analytical Model for the DTG-CSC-TFET for LS = 20nm 126
Figure 4.15. Electron Concentration for LS=20nm (a) without including Quantum Models (b) including Quantum Models.. 127
Figure 4.16. Transfer Characteristics for L_S=20nm with and without including Quantum Models 127
Figure 4.17. Proposed Inverter consisting DTG-CSC-TFET 128
Figure 4.18. (a) VTC of the DTG-CSC-TFET inverter with supply voltage (VDD) from 0.2 V to 0.5 V. (b) voltage gain of the DTG-CSC-TFET inverter under various VDD, showing high gain even at VDD = 0.2 V. 128
Figure 4.19. Input signal and transient response of the DTG-CSC-TFET inverter 129
Figure 5.1 Structure of CA-PNPN-DG TFET along with the doping concentration of the proposed TFET structure for (a) 7nm, (b) 14nm, and (c) 24nm gate length......................... 141
Figure 5.2: Potential distribution of the proposed CA-PNPN-DG TFET structure for (a) 7nm, (b) 14nm and (c) 24nm gate length 146
Figure 5.3. Comparison of analytical result of the surface potential distribution and simulation outcome for (a)7nm, (b) 14nm and (c) 24nm gate length 147
Figure 5.4: Potential Distribution along the length of the proposed CA-PNPN-DG TFET structure for (a) 7nm, (b) 14nm and (c) 24nm gate length.. 147
Figure 5.5: Electric field distribution of the proposed CA-PNPN-DG TFET structure for (a) 7nm, (b) 14nm and (c) 24nm gate length 148
Figure 5.6: Electric field along the length of CA-PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths.. 149
Figure 5.7: Comparison of valence and conduction band energy for 7nm, 14nm and 24nm gate lengths.. 149
Figure 5.8. Transfer Characteristics of CA-PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths... 150

Figure 5.9 Structure of TB-PNPN-DG TFET for gate length of (a)7nm , (b)14nm and (c) 24nm. 151
Figure 5.10. The Potential distribution for different gate lengths (a) 7nm, (b) 14nm , (c) 24nm 156
Figure 5.11. Simulation-based results of surface potential distribution for 7nm, 14nm and 24nm gate lengths 156
Figure 5.12. Electric field distribution profile for gate length (a) 7nm, (b) 14nm and (c) 24nm. 157
Figure 5.13. Electric field distribution profile for gate length (a) 7nm, (b) 14nm and (c) 24nm. 158
Figure 5.14. Comparison of valence and conduction band energy for 7nm, 14nm, and 24nm gate lengths........ 158
Figure 5.15. Transfer Characteristics of TB-PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths........ 159
Figure 5.16. Transfer Characteristics of PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths........ 159
Figure 5.17: Plot of (a) C_{gs} (b)C_{gd} w.r.t V_{GS}........ 160
Figure 5.18: Plot of (a)g_m (b) f_T (c) GBP wrt V_{GS}........ 161
Figure 5.19: Plot of Transit-time(τ) w.r.t V_{GS}........ 161
Figure 5.20: Plot of (a) TGF (b) TFP w.r.t V_{GS}........ 162
Figure 5.21: I_{DS} VS V_{GS} at V_{DS}=0.5V for n and p-type CA-PNPN-DG TFET 162
Figure 5.22: Schematic Diagram of CA-PNPN-DG TFET inverter........ 163
Figure 5.23: VTC of CA-PNPN-DG TFET inverter........ 163
Figure 6.1 . Device structure of (a) n and (b) p- type DSS-TFET 176
Figure 6.2 Calibration of simulation data with the experimental result of Reference [13]. 176
Figure 6.3 Process flow for the fabrication of the proposed DSS- TFET structure 176
Figure 6. 4. I–V characteristics for both n and p- type DSS-TFET at VDS=0.1V 178
Figure 6.5 Comparison of Subthreshold Swing for both n-type and p-type SDS-TFET at VDS=0.1V........ 178
Figure 6.6. Variation of oxide thickness for both n-type and p- type DSS-TFET at VDS=0.1V 179
Figure 6.7. Variation of Gate Work function for both n and p-type DSS-TFET at VDS=0.1V . 179
Figure 6.8. Total Current Density of 13-nm gate length (a) n-type and (b) p-type DSS-TFET180
Figure 6.9. BTBT rate of 13-nm gate length (a) n- type and (b) p-type DSS-TFET........ 181
Figure 6.10. IDS-VDS carve for both p-type and n-type DSS-TFET at different VGS 182
Figure 6.11. (a) Proposed Inverter consisting DSS-TFET (b) Truth Table 182
Figure 6.12. (a) VTC of the DSS-TFET inverter with VDD varied from 0.2 V to 0.5 V (b) voltage gain of the DSS-TFET inverter under various VDD, showing high gain even at VDD = 0.2 V. 183
Figure 6.13. VTCs of the proposed inverter at VDD=0.2 V… 184
Figure 6.14. I/P and O/P of the proposed NOT gate 185
Figure 6.15. NAND gate (a) circuit connection (b) Truth Table........ 186
Figure 6.16. I/P and O/P of the proposed NAND gate 187
Figure 6.17. NOR gate (a) circuit connection (b) Truth Table 188
Figure 6.18. I/P and O/P of the proposed NOR gate........ 188
Figure 7.1 Structure of Gate Centric Extended Source SOI TFET 201

Figure 7.2 Fabrication steps of the proposed structure 202
Figure 7.3 Line and Point tunneling 203
Figure 7.4 Line tunneling through the energy bands along cutline (a) AA’ and (b) BB’......... 206
Figure 7.5 Variation of VDS for 10nm gate length of GCES SOI TFET Gate 207
Figure 7.6 Variation of gate source overlap region for 7nm gate length of GCES SOI TFET .. 208
Figure 7.7 Variation of drain and source contact position.. 208
Figure 7.8 Comparison of band diagrams of GCES SOI TFET for three different gate lengths of 10nm, 7nm and 5nm.. 209
Figure 7.9 Comparison of electric fields along the length of GCES-SOI TFET for three different gate lengths of 10nm, 7nm and 5nm.. 209
Figure 7.10 Comparison of surface potential along the length of GCES-SOI TFET for three different gate lengths of 10nm, 7nm and 5nm.. 210
Figure 7.11 Transfer Characteristics for GCES SOI TFET for gate lengths of 10nm, 7nm and 5nm. 210
Figure 7.12 Comparison of analytical current modeling with simulation result of drain current for GCES SOI TFET.. 210
Figure 7.13 Comparison of Transfer characteristics of GCES SOI TFET with considering quantum effects and classical behaviour for three gate lengths of (a) 10nm, (b) 7nm and (c) 5nm. 211
Figure 7.14 Electron concentration for 10nm gate length of GCES SOI TFET for (a) classical behaviour and considering (b) quantum confinement. 212
Figure 7.15 Electron concentration for 7nm gate length of GCES SOI TFET for (a) classical behaviour and considering (b) quantum confinement. 212
Figure 7.16 Electron concentration for 5nm gate length of GCES SOI TFET for (a) classical behavior and considering (b) quantum confinement. 213
Figure 7.17 Comparison of SS for gate length of 10nm, 7nm and 5nm of GCES SOI TFET 213
Figure 7.18: Transfer characteristics of P type and N type GCES SOI TFET structures 214
Figure 7.19 Proposed Inverter consisting SDS-TFET 214
Figure 7.20 (a) VTC of the GCES SOI TFET inverter with supply voltage (VDD) (b) voltage gains 215
Figure 7.21 Input signal and transient response of the GCES SOI TFET inverter 215

List of Tables

Table No **Description** **Page No**

Table 2.1: MOSFET Region of Operation 28
Table 3.1: Summarizes all the parameters for all the structures..83
Table 4.1: Different DC parameters of the proposed inverter at Vdd=0.2 volt.................... 129
Table 5.1: Different parameters of the inverter based on the proposed CA-PNPN-DG TFET structure.. 164
Table 6.1. Different DC parameters of the inverter based on our proposed structure of TFET ……….. 185
Table 6.2. Calculated the power of the inverter based on our proposed structure of TFET.186
Table 6.3. Power-delay comparison of the proposed and compared NAND gates 187
Table 6.4. Power-delay comparison of the proposed and compared NOR gates................. 188

List of Abbreviations

ALD: Atomic Layer Deposition

BJT: Bipolar junction transistor

BSD-SG TFET: Basal-Splitted-Drain Single-Gate TFET

B2B/BTBT: Band-to-Band tunneling

BMA: Binary metal alloy

BG-TFET: Broken gate TFET

CLM: Channel Length Modulation

CA-PNPN TFET: Centrally Aligned Source Pocket Reigned TFET

CB: Conduction band

CLM: Channel-length modulation

CMOS: Complementary Metal-oxide field-effect transistor

CTFETs: Complementary TFET

DICE: Drain Induced Conductivity Enhancement

DTG-CSC-TFET: Double Trench Gate Covered TFET

DG TFETs: Double-gate tunnel FETs

DG-TFET: Double Gate TFET

DMG: Dual Material gate

DM: Dual-material

d-MOSFET: Depletion mode MOSFET

DIBL: Drain-induced Barrier Lowering

DSS-TFET: Dual Source TFET

EB: Energy band

EHBTFET: Electron-hole bilayer tunnel field-effect transistor ().

e-MOSFET: Enhancement mode MOSFET

fA: femto amperes

FET: Field effect transistor

GAA-TFET: Gate All Around TFET

GaAs: Gallium Arsenide

GCA: Gradual Channel Approximation

GCES SOI TFET: Gate Centric Extended Source SOI-TFET

HCEs: Hot Carrier Effects

HFO_2: Hafnium (IV) oxide

HGD: Hetero-Gate-Dielectric)

IC: Integrated Circuit

IFETs: Impact Ionization in Impact Ionization FET

IoT: Internet of things

IOE: Internet of everything

ITRS: International Technology Roadmap for Semiconductors

JFET: Junction field-effect transistor

JL-TFET: Junctionless tunnel field-effect transistor

LBD: Localized body doping

LDD: Lightly Doped Drain

LTFET: L-Shaped TFET

LG-TFET: L-Shaped Gate TFET

LTFET: L-shaped tunnel field-effect transistor

MOSFET: Metal oxide field-effect transistor

MSD-SG TFET: Mesial-Splitted-Drain Single-Gate TFET

NC-FET: Negative Capacitance FET

NEM-FET: Nano-Electromechanical FETs

NWTFETs: Nanowire tunneling field-effect transistors

PC-TFET: Phase Change TFET

QCE: Quantum confinement effect

RF: Radio Frequency

SCE: Second order effect

SD-SG TFET: Splitted-Drain Single-Gate TFET

S.E.: Schrödinger's equation

SiNW: Silicon nanowire

SiO_2: Silicon Dioxide

SOI: Silicon on Insulator

SON: Silicon on Nothing

SS: Subthreshold Swing

TB-PNPN-DG TFET: Two symmetric pockets at Source Region in TFET

TFET: Tunnel field-effect transistor

TSD-SG TFET: Top-Splitted-Drain Single-Gate TFET

TVRO: Threshold Voltage Roll-Off

GAA -TFET: Gate All Around TFET

TG-TFET: Triple gate TFET

t_{ox}: Gate dielectric thickness

t_{si}: Channel thickness

TBW: Tunneling Barrier Width

TBM: Tunnel barrier modulation

TDM: Tunneling distance modulation

TM-DG-TFET: Triple metal double gate tunnel FET

TSRs: Two source regions

V_P: pinch-off voltage

VB: valence band

Chapter :1

Chapter-1: Introduction and Organization of Thesis

1.1 Introduction and Motivation 2
1.2 Literature Review 8
1.3 Organization of the Thesis 11
References 14

1.1 Introduction and Motivation:

According to G. Busch [1.1], in the year 1782, Italian physicist **Alessandro Volta** uses the term "semiconducting" for the first time. While investigating the effect of temperature in the year 1833, **Michael Faraday** observed in silver sulfide crystals that the electrical conductivity increases with temperature, which is opposed to the behaviors that are observed in copper and other metals, where conductivity decreases as the temperature increases which is the first documented observation towards semiconductor behaviors [1.2]. The history of semiconductors focused on two important properties, one is the rectification of metal-semiconductor junction and the other one is the sensitivity of semiconductors. Semiconductor point-contact rectifier effect was discovered where current flows freely in only one direction at the contact between a Galena crystal and a metal point, is the first description of a semiconductor diode by **Ferdinand Braun** in the year 1874, [1.3]. This discovery played a significant role in the evolution of the radio and radar systems leading to his Nobel award in physics in 1909. The first electronic device was a PbS-based point contact rectifier and was invented by Radio pioneer **Jagadish Chandra Bose** (obtained patent) in the year of 1901 [1.4]. It was shown that these rectifiers were capable of detecting radio waves and G. Pickford was the first human to establish it in the year 1906. Based on the semiconducting properties of copper sulfide, **Julius Lilienfeld** described a three-electrode amplifying device [1.5] and thus patented the concept of the Field-Effect-Semiconductor Device in the year 1926. William Shockley proposed the idea of a semiconductor amplifier based on the field-effect theory in 1945. The idea was that applying a transverse EF to a semiconductor layer would affect its conductance. However, evidence of this effect was not found during the lab experiment. This,

according to John Bardeen, is due to surface states removing the majority of the substance from the field. In 1947, he published his surface theory [1.6]. Also, it was the year when the first point-contact transistor was invented by W. Brattain and J. Bardeen. The mechanism responsible for transistor operation was, however, a source of controversy [1.7]. Surface-related phenomena, according to Bardeen and Brattain, played the most important role in the operation of the new system, while Shockley preferred bulk conduction of minority carriers. He established a junction transistor as well as p-n junction theory about a month later [1.8]. In 1956, Shockley, Brattain, and Bardeen were awarded the Nobel prize in Physics. At Texas Instruments, **Jack Kilby** invented the first Integrated Circuit (IC) [1.9] – the microchip on Sept. 12, 1958. After six months of Kilby's first Integrated circuit design, **Robert Noyce** developed his own idea of an IC that solved many shortcomings of Kilby's design. Using the planar process Noyce's monolithic IC was fabricated easily by Jean Hoerni in the year 1959. Unlike Jack Kilby's chip which was made of Germanium (Ge), Robert Noyce designed the IC using Silicon (Si). At Sprague Electric, **Robert Noyce** credited **Kurt Lehovec** explores the principle of how to isolation p–n junction, which was a key concept in the improvement of the IC design [9]. This isolation technique allowed each transistor to operate without any interference to and from the neighbouring transistor, despite being on the same silicon chip. **Dawon Kahng** and **Martin M. (John) Atalla** invented the first MOSFET at Bell laboratory in 1959, as a variation on the patented FET design [9]. There is a difference in opinion on whom to be exactly credited for the invention of the IC. In the 1960s, four people: **Kilby, Lehovec, Noyce,** and **Hoerni**, were being recognized by the American press. But by the 1970s the list was curtailed to **Kilby** and **Noyce** only. In the year 2000, the Nobel Prize in Physics was awarded to **Jack Kilby** for his part in the invention of the IC [1.9], which changed the daily life just as spectacularly as **Thomas Alva Edison** did and **Henry Ford** did. But nobody's ever heard of **Jack Kilby** making him Probably the most unassuming Nobel laureate in the history of physics."

After a few years of the invention of the Integrated circuit, i.e., in the late sixties, designers were trying to integrate all the components of a central processing unit (CPU) into a handful of chips and were successful to a certain extent. **Ted Hoff** and **Stanley Mazor**, assisted by **Masatoshi Shima** and **Federico Faggin** designed Intel's first microprocessor, **4004**, which

had almost all the components of a central processing unit integrated into it, except for the memories, in the year **1971** [1.10].

The commercialization of microprocessor ICs led to the computer revolution which changed the future of mankind. The ripples of this major scientific achievement, the commercialization of micro-computers, manifested itself as a huge wave and washed humanity to the shores of the Information age. It is a long way from **Charles Babbage's** mechanical computer "The Difference Engine" to the Vacuum tube-based computers like the Colossus, ENIAC and the commercially available IBM 650, etc., to transistorized ones like Harwell CADET, IBM 604 calculator, etc., and finally to integrated circuit-based computers, we see in our everyday lives. At present, microprocessors and microcontrollers have become an indispensable part of our life. Almost in all everyday items, starting from refrigerators, microwaves, modern toasters, washing machines, sewing machines, to smartphones and high-end digital cameras, etc., electronic computation is omnipresent [1.11-1.13]. With the gain in traction of the Internet of things (IoT) and currently, the Internet of Everything (IoE), integration of computers into our daily lives is inevitable.

The key component of the IC industry is MOSFET which belongs to the category of Field-Effect Transistors, like JFETs and unlike BJTs. Almost all of the digital appliances that we use are primarily based on MOSFET. The MOSFET can be fabricated using n or p-type substrate, leading to p-channel and n-channel MOSFETs respectively. The devices thus formed, are complementary in nature and can be used in pairs to implement different Boolean-logic circuits. These circuits are collectively called as the Complementary MOSFET circuits or CMOS circuits, which are the work-horse of the industry to this day. The main advantages of MOSFETs are based on the fact that their fabrication and integration are simple and it requires negligible drive current at the gate for controlling the load current. The use of "metal" in the name of MOSFET is not at all justified considering the current technology. The gate is formed using Polycrystalline Silicon (and not metal) due to the ease and accuracy of fabrication, because of its endurance to high temperatures. Also, different high-k dielectric materials are being used as the oxide instead of the more common Silicon Dioxide (SiO_2) [1.14-1.18]. Due to the amazing scaling property of the MOSFET, unlike other transistors, the number of MOSFETs in a digital IC has reached billion.

The relentless shrinking in the size of the MOSFETs is only possible due to the advancement in Silicon-CMOS fabrication technology. Only a decade or two back, the MOSFET channel lengths were in order of micrometers and now it is nearing a few nanometres. The advantages of having a smaller device are many folds. The reduced device dimension means a greater number of transistors in a given silicon chip area, which directly translates to more functionality per chip, thus compact appliances [1.19]. Also, since the cost of fabrication and processing per silicon chip is almost constant, the overall price for a more functionally powerful device is reduced, and the history of prices on consumer electronics bears proof of this statement. Smaller devices, especially MOSFETs tend to switch faster than their larger channel counterparts. This is because; the main dimensions of channel length, channel width & oxide thickness are scaled. Scaling down dimensions by an equal factor, the overall channel resistance of the device is not changed, but the gate capacitance is curtailed by a factor, hence lower time delays and faster switching speeds. Thus, scaling has led to faster devices [1.19].

However, to continue the unhindered progress in designing the complex ICs and to fulfil the assiduous demand for ameliorated device functionality, gradual downscaling of each of the device dimensions is required allowing a larger number of components to be fabricated on a single semiconductor wafer; by thus, reducing the overall circuit area with subsequent increase in packaging density. Hence, the concept of device scaling plays a crucial role in amending the device performance and is inclined to improve the processing speed, and package density while reducing its volume, power consumption, and fabrication cost per function [1.20]. This device dimension miniaturization of CMOS transistors thus acts as a catalyst to the growth of the semiconductor industry for future ultra-low-power circuits with reduced circuit volume, and minimized power dissipation by each functional unit accompanied by the momentous speed of operation [1.21-1.23].

Integrated circuit pioneer **Gordon Moore** made his famously insightful and accurate prediction that the exponential increase in the number of transistors in IC per unit area of silicon would double every 18th month thanks to the excellent scalability of MOSFETs, noting that chip performance increases while price decreases. But this law must slow down since:

1. Electrons can tunnel through the barrier of silicon transistors smaller than 5nm.

2. Intense heat will generate as increasing transistor density increases power density.

3. Each new miniaturized chip iteration represents a significant increase in design and implementation costs.

Thus, it should be the mission to go beyond "***More than Moore***" [1.24-1.27] or to find alternate devices that can replace MOSFET, just as it replaced its predecessors (BJTs, Vacuum tubes, relays, etc). Before looking for alternatives, let's look on the shortcomings of MOSFET, which bore the brunt of the electronic industry for many decade.

The shortcomings associated with MOSFETs [1.28] can be described briefly as follows:

1. The drain current of MOSFET is dependent on the overdrive voltage (V_{DS}-V_T), the threshold voltage needs to be reduced along with the supply voltage for better current drive.

2. The increase in overdrive voltage (through V_T reduction) not only increases the current drive but also increases the $I_{leakage}$, increasing the I_{OFF} exponentially.

3. This exponential increase in I_{OFF} is due to the fact that the sub-threshold swing (SS) of the MOSFET is not scalable, and has a fixed lower limit, i.e., 60mV/decade at room temperature.

4. Hence, by reducing the power supply voltage and keeping the overdrive constant, it is observed that the leakage increases to unacceptable amounts. Thus, making the option of achieving lower sub-threshold swings a necessity, which as we know is impossible for MOSFET.

5. As the device dimensions keep on decreasing, the voltages have to be scaled accordingly to reduce the leakage and to reduce the power consumption, but after a while the voltage scaling might not be possible due to compatibility issues with the peripherals and increased delays associated with lower supply voltages.

6. If the channel length goes down below tens of nanometre, the carriers can just directly tunnel between source and the drain, thus increasing the I_{OFF} current through leakage.

7. The fabrication of short channel length MOSFETs reliably have always been a problem. But in recent years with the help of Atomic Layer Deposition (ALD) technique, MOSFETs with channel lengths lower than 10s of nm have been fabricated.

8. Smaller devices are harder to fabricate with consistency and the variability of device performance increases; hence the overall performance of the IC becomes unpredictable, with reliability problems.

9. The limited voltage scaling options led to increased power dissipation per transistor in an IC.

In a MOSFET, the sub-threshold swing (SS) is limited to a lower value because of the fundamental nature through which the carriers travel through the channel. Due to the thermionic injection of electrons, current flow over the source-channel energy barrier.

The thermal dependence sets a fundamental limit to the slope of the OFF to ON transition and vice-versa. The sub-threshold swing, *SS* which determines the gate voltage required to change the drain current by an order of 10 (decade). Two factors namely "ɑ" is the transistor body factor and "b" is the factor that relates to surface potential Ψ_S with the drain current I_D. The C_d and C_{ox} are depletion region and oxide capacitances respectively, while 'k' is Boltzmann's constant, 'q' is the magnitude of electronic charge and 'T' is the temperature in Kelvin. The 60mV/dec limit can only be reduced by using a physical phenomenon other than thermionic injection for carrier conduction. The solution thus can be broadly classified into two sections, depending upon the 'a' and 'b' factors.

i. The body factor "a" can be made less than unity by making the gate active in nature, unlike the passive gates employed in MOSFET. The active gate devices such as Negative Capacitance FET (NC-FET) [29], NEM-FET (Nano-Electromechanical FETs) [1.30] etc can achieve lower SS.
ii. The factor "b" can be made less than (kT/q)ln10, by using different carrier injection mechanisms in the channel, like the band-to-band (B2B/BTBT) tunneling mechanism in Tunnel Field Effect Transistors (TFETs) [1.31], Impact Ionization in Impact Ionization FETs (IFETs). Such devices are also capable of achieving less than 60mV/decade SS, unlike the MOSFETs.

The thesis presented here has concentrated on the Band-to-band tunneling device, the Tunneling Field Effect Transistors (TFETs). It emerging as one of such promising preferences over MOSFET offering lower OFF-state leakage current, reliable functionalities, improved potential to combat the adverse SCEs, and achieving a SS below the limiting value of 60mV/decade. Moreover, the structural similarity between TFET and MOSFET (with the only dissimilarity in the type of dopants of source and drain regions) ensures integration of TFET fabrication facile and feasible with existing MOSFET process technology. However, in spite of the above-mentioned benefits, TFET includes its low ON current with respect to MOSFET

where thermionic emission of carriers controls the driving current of the device and its ambipolar conduction restricts the applications of TFETs to complementary digital applications.

1.2 Literature Review

Some of the research outcomes also suggest improvement in the ON current of TFET device by compromising the leakage under OFF state conditions [1.32-1.36]. Hence, several improvisations over conventional TFET structure are required either by some structural modifications or incorporating popular schemes of gate material and lateral channel engineering as described previously to make the device appropriate for future generation VLSI circuit applications. A number of research works have also been presented by several authors emphasizing the enhancement of functional efficiency of TFET devices along with overcoming the major bottlenecks associated with TFET. As a possible solution to surmount the problem of low ON-state current conduction of TFET devices, Verhulst et. al. [1.37] developed an analytical model-based performance assessment of single gate, double gate, and gate all-around TFET structures demonstrating effective improvement in I_{ON} current due to enhancement of the gate control over the channel. Later, Wang et al. [1.38] investigated the theoretical characterization of GaAsBi/GaAsN Type-II Staggered Heterojunction TFETs showing increased tunneling probability and improved device current. Novel Ge1−xSnx /Ge1−ySny heterojunction-enhanced n-TFET architecture by Liu et al. [1.39] and GeSn/SiGeSn type-II staggered heterojunction TFET by Wang et al. [1.40] contribute to the significantly enhanced BTBT and tunneling current in the hetero-n- TFET. The perception of gate material engineering and hetero gate dielectric in TFET is also explored analytically by Sanjay Kumar et al. [1.41] by compounding together the dual benefits of the dual material gate and SiO2/HfO2 high-k gate stack in double gate TFET. The dual material concept helps to modulate the barrier at the source-channel junction and channel/drain end with the simultaneous benefit of improved ON current and suppressed ambipolar conduction of TFET. Another significant feature of this derived model is that it included the source/drain depletion regions and made this analytical model suitable for application for other materials like SiGe (indirect bandgap) and InAs channel-based TFET structures in addition to conventional silicon-based channels. Triple Metal DG TFET structure is presented by Bagga et al. [1.32] exhibiting admirable device performance. The concept of gate function engineering is improvised to a further extent by

incorporating the innovative concept of "linearly graded binary metal work functioned gate electrode" by Sarkhel et al. [1.42] revealing the effectiveness of the structure in potential distribution and superior current drivability. Another interesting structure proposed by Abdi and Kumar [1.36] is overlapping gate-on-drain TFET to curb the ambipolar leakage current of TFET. Work demonstrated that due to the presence of overlapped gate in the drain region, effect of reversed gate voltage is identical on both the channel and the overlapped drain region. This reduces the possibility of n+ drain/channel tunneling barrier narrowing and hence controls the device ambipolarity effectively. Recently, a dielectric pocket-induced double gate TFET (DP DG-TFET) structure is also proposed by Upasana et al. [1.43] where the simulated results show improved current driving capability, high I_{ON}/I_{OFF}, and reduced ambipolar conduction, making the architecture suitable for low power applications. Apart from these theoretical analyses of different derived analytical models and their validation with simulation results, several experimental results are also reported for various fabricated TFET structures which always pose a significant influence in research fields. Zhijiong Luo et al. [1.44] successfully fabricated a novel tunnel dielectric-based Tunnel FET that achieved a steeper subthreshold slope of 55mV/dec with reduced ambipolar leakage and low OFF-state current. Han et al. [1.45] reported that a higher I_{ON}/I_{OFF} ratio and improved subthreshold slopes of TFET devices can be achieved by experimentally growing GeSn quantum well (QW) PTFETs on Si (111). Mookerjea et al. [1.46] reported an experimental demonstration of channel length 100 nm In0.53Ga0.47As-based Vertical Inter-band TFETs for SRAM applications. N-channel In0.53Ga0.47As TFETs were fabricated using MBE grown epitaxial structure on semi-insulating InP substrate and implemented in 6T SRAM cell. Results showed excellent noise margin down to 0.3V supply voltage making narrow gap III-V TFET an alternating architecture for ultra-low power digital applications. Thus, from the above illustration, it can be inferred that there exist enormous scopes and opportunities for researchers to explore the domain of semiconductor devices and develop innovative alternate device architectures that can efficiently curtail the adverse effects of SCEs without degrading the performance. A solution to the future nanodevices with low power consumption, high operating speed, and minimum cost are required to stay shoulder to shoulder with the ever-increasing technological demand of modern society.

A two-dimensional numerical standard for threshold voltage (Vth) has been reported in [1.47] including its dependence on back gate bias. Worley [1.48] presented an analytical calculation-based threshold voltage model for an SOS (silicon on sapphire) MOSFET considering the coupling of induced charges between the front and the back gates. Recently several nonconventional MOS geometries have been studied experimentally as well as theoretically to investigate various short-channel issues. Silicon On Insulator (SOI) structure has been trapped by most researchers due to its compatibility with bulk MOSFET, superior electrical characteristics, and easier fabrication feasibility [1.49]. In 1988, Susan Edwards and Kevin Yallup studied the floating region of SOI MOSFET employing two-dimensional numerical simulations. The floating region, formed in the bulk silicon film, was highlighted in their simulation work. Usually, there is no direct electrical connection between this region and any external electrode. Thus, they can act as a trap for charge generated by avalanche ionization. The trapped charges inside the floating body now influence the device output characteristic, the phenomenon so tagged is called the kink effect [1.50]. Srinivasa R. Banna et. al. derived a short channel SOI model to study threshold voltage variation by using a quasi-two-dimensional approach [1.51] illustrating the Threshold Voltage Roll-Off (TVRO) mechanism. This model has not included a priori charge partitioning or constant surface potential making it suitable for application in circuit simulation. The threshold voltage shift was found to be identical to that of its bulk MOSFET equivalent. With the effective channel length being fixed, threshold voltage roll-off in FDSOI was evidently reduced than its bulk counterpart. For short-channel SOI/SON MOSFET Bibhas Manna, et. al.[1.52] derived a binary metal alloy gate electrode. Saheli Sarkhel et. al [1.53] showed that cylindrical junctionless MOSFET has improved short channel performance [1.54]. Linearly graded binary metal alloy gate electrode for enhanced performance has been explored by Navjeet Bagga et. al. [1.55] for a DGMOSFET. For Improved I_{ON} , Tripty Kumari et. al.[1.56] proposed dual gate material hetero-dielectric strained PNPN TFET.

Another improved physical I-V model for a fully depleted SOI MOSFET was developed by Yuhua Cheng et. al. having a channel length comparable to the deep sub-micrometer range [1.57]. The model has claimed taking account various SCEs such as velocity saturation, Drain Induced Barrier Lowering (DIBL), Drain Induced Conductivity Enhancement

(DICE), Channel Length Modulation (CLM), gate bias dependent mobility, and floating body effect to establish its accuracy. J. B. Roldán et. al. formulated an analytical current-voltage model for ultra-short channel SOI MOSFET intended for circuit simulation. This model includes the velocity overshoot, series resistance, and self-heating effects [1.58]. M. Youssef Hammad et. al. proposed an analytical model for a partially-depleted (PD) SOI-MOSFET employing front-back interface coupling with all the possibilities of accumulated, neutral, and depleted back interface [1.59] above the threshold. Later that year, Keunwoo Kim and Jerry G. Fossum [1.60] experimented on an asymmetrical DG-CMOS utilizing n+ and p+ polysilicon gates. Guruprasad Katti et. al. have derived a three-dimensional Poisson's equation solution which is based on an analytical V_{th} model for a mesa-isolated FD SOI MOSFET [1.61]. The model depicts accurate analytical expressions for the threshold voltages of front and back gates enabling the model to predict short channel behaviour along with narrow width effects.

1.3 Organization of the Thesis

The present dissertation has been organized into different chapters containing some non-conventional FET structures for ameliorated device performance along with a brief overview of nanoscale devices followed by a relevant literature survey and ends with a concluding chapter.

Chapter 2: This chapter describes some of the basic MOSFET device structures relevant to the thesis where some drawbacks of the basis of MOSFET are highlighted, thereby making the path for the introduction of new device structures to overcome those flows.

Chapter 3: A 2D analytical model for the potential distribution of a drain doping engineered tunneling field-effect transistor (TFET) with a split drain structure has been performed. The tunneling drain current is derived using potential distribution. Further, analyses are made to observe the influence of drain doping engineering on all characteristics and parameters of a TFET model. The splitted drain structure exhibits a major reduction in ambipolar conduction due to an increase in the tunneling width at the channel-drain junction. Simulation of four different structures of the device consisting of splitted drain region with relative location and doping concentration is executed. The structures are named according to the relative position of the drain: Splitted-Drain Single-Gate TFET (SD-SG TFET: total drain is splitted), Top-Splitted-Drain Single-Gate TFET (TSD-SG TFET: splitted-drain in upper location), Mesial-

Splitted-Drain Single-Gate TFET (MSD-SG TFET: splitted-drain in middle location), Basal-Splitted-Drain Single-Gate TFET (BSD-SG TFET: splitted-drain in bottom location). All the fundamental device characteristics and parameters are analyzed for all four structures considered here and their merits and drawback are recorded for optimal valuation and detection of better structure. All the proposed structures show improved performance with suppressed gate leakage and ambipolarity than conventional planar TFET. All the simulations are done in Silvaco, Atlas.

Chapter 4: A novel Double Trench Gate Covered Source Channel TFET (DTG-CSC-TFET) has been proposed and its analytical current model has been derived. The extended source region of the proposed structure maximizes the tunneling area. Two tunneling mechanisms- line tunneling and point tunneling jointly contribute to a high ON-current. The model has been validated through SILCACO, Atlas simulations. The device operates at V_{DS}=0.1V and exhibits excellent Subthreshold Swing (SS) of 23mV/decade and high I_{ON}/I_{OFF} of 10^{12}. The Quantum confinement effect has been studied for the proposed DTG-CSC-TFET using the Schrödinger-Poisson model in the simulations. Finally, the applications of DTG-CSC-TFET inverter design have been demonstrated. SPICE calibration is executed for DC and transient responses of the DTG-CSC-TFET inverter have been analyzed. The DTG-CSC-TFET has excellent performance characteristics and is viable for low-power applications.

Chapter 5: A 2D TFET with centrally aligned source pocket doping TFET (CA-PNPN-DG TFET) and a two symmetric pockets at Source Region TFET (TB-PNPN-DG TFET)has been executed and its performance metrics have been explored through simulations.. This structural modification improves source tunneling, resulting in a higher I_{ON}/I_{OFF} ratio and reduced ambipolarity, as compared to conventional planar TFETs. In order to study the performance characteristics, the gate metal length has been varied-24nm, 14nm, and 7nm. HfO_2 has been used as the gate oxide material. The three resulting structural variations are compared to obtain the most optimized structure. Furthermore, the frequency analysis is performed to find out the transconductance generation factor and the transconductance frequency product. An inverter is implemented using the CA-PNPN-DG TFET. CA-PNPN-DG TFET has excellent performance characteristics and is viable for low-power applications.

Chapter 6: Asymmetrical double source SOI TFET (DSS-TFET) of both n and p-type has been proposed, and the impact of different parameters on the device's efficiency and low power capabilities has been carefully investigated. By suppressing the ambipolar current, the suggested DSS-TFET may achieve complementing performance. For various channel lengths, the DSS-TFET has almost equivalent SS. As a result, in circuit design, a 13nm n-DSS-TFET can be utilized with a 5nm p-DSS-TFET, resulting in a decrease in chip area. Ambipolar conduction has improved as a result of the incorporation of SOI architecture, resulting in a higher I_{ON}/I_{OFF} ratio of 10^{13} and 10^{12} for both n and p-type TFETs, respectively. To investigate the circuit level performance of the proposed TFET, NOT, NAND and NOR logic gates have been designed and their performance has been studied. The voltage transfer characteristic (VTC) of the inverter composed of these n and p-type DSS-TFETs were analyzed at various V_{DD}. It has been observed that the proposed inverter is behaving almost like an ideal CMOS inverter at the V_{DD} of 0.2V. Power consumption (Pd) and delay (Td) of the proposed logic gates have been compared with the existing TFET-based logic gates to justify the low power circuit application. For simulation, SILVACO Atlas has been incorporated.

Chapter 7: An alternative SOI TFET structure precisely GCES SOI TFET has been proposed and studied in this paper by modifying its gate length for three different values. An analytical model of the proposed structure considering point and line tunneling has been derived and validated by simulation. The device is optimized to a suitable V_{DS} of 0.1V, extended source alignment with the center position of the gate, and optimum drain contact position. The transfer characteristics, band diagrams, electric field, and potential distributions are examined as the device performance parameter. The results distinctly exhibit that the device performs best when the gate length is 10nm having SS as low as 19.8mV/dec and a ratio of ON/OFF current as 10^{15}. SS increases and ON current decreases by a negligible scale when quantum confinement has been taken into account due to the discrete energy band at the source-channel interface using the Schrödinger-Poisson model. The simulations are performed using Silvaco, Atlas. Moreover, the GCES SOI TFET inverter is characterized by SPICE calibration, and provides a higher gain of 16 at lower V_{DD}=0.2V.

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Chapter:2

CHAPTER – 2: Basics of Semiconductor Devices

2.1 Introduction to Semiconductor Devices....23
2.1.1 Overview of Metal Oxide Semiconductor Field Effect Transistor (MOSFET)....24
2.1.2 Types of MOSFET 26
2.1.3 Operational regions of MOSFET 28
2.1.4 Complementary Metal Oxide Semiconductor (CMOS).... 31
2.1.5 Power Dissipation in CMOS....32
2.1.6 Issues with Scaling and Moor's law....34
2.1.7 Short Channel Effects in MOSFET....36
2.1.8 Evolution of advanced MOSFET structures....41
2.2 Introduction to Tunnelling....46
2.2.1 A Brief Introduction to Band-to-Band Tunnelling 47
2.2.2 Band-to-Band Tunnelling Models....48
2.2.3 Basic Construction of TFET 50
2.2.4 Working Principle of TFET in Brief....50
2.2.5 Transfer characteristics of traditional TFET structures....52
2.3 A Brief Literature Review on various TFET Designs for Performance Enhancement 57
References....67

2.1 Introduction to Semiconductor Devices

The last few decades have witnessed phenomenal growth in the microelectronics industry being obsessed by the continuous shrinking of device dimensions to increase the device integration density with subsequent reduction in manufacturing cost. The future of VLSI as predicted by Moore in 1965 with proportional device downscaling also portrays its progress through high operating speed VLSI circuits and minimum power consumption [2.1]. However, aggressive downscaling of conventional MOS technology suffers the limitations of complex fabrication techniques and the associated cost. Moreover, ultra-nanoscale device physics also requires a lucid concept of quantum mechanical laws [2.2]. Such small-scaled devices when integrated on a single chip may lose their functional competency and degrade the overall circuit operation. These challenges are driving the researcher community to investigate nonconventional MOS structures that can circumvent the scaling limitations and allow further miniaturization without compromising the device performance. While some of these devices employ the principle of quantum mechanical phenomena and are referred to as revolutionary nano-electronic devices (quantum well, quantum wire, quantum dot-based devices e.g. HEMT,

Spintronics, SET, etc.), the other group of scaled devices with geometrical modifications and improvisation in material properties in existing technology fall under the category of evolutionary nano-devices (e.g. Carbon Nanotube FETs, heterojunction based FETs, Nanowire FETs, Ge channel devices, strained channel FETs, structurally refined FETs, etc.). Incessant research exploration in pursuit of such non-conventional devices can satisfy Moore's scaling trend and realize superior functionality by suppressing inevitable short channel effects in terms of DIBL, V_{th} roll-off, and hot carrier effect, to mention a few [2.3]. The architecture, operating principles, and analytical modelling approaches of such devices are quite different from conventional ones and have been focused on in the present thesis highlighting the available options of further scaling and proper device optimization.

2.1.1 Overview 0f Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has earned commendable popularity since the 1970s owing to its simple architecture, reduced fabrication cost, minimized power consumption, inherent high input impedance, and momentous speed of operation and improved noise immunity. Superior scalability of MOSFET device for incremented transistor count per chip as predicted by Moore's law has marked the evolution of the semiconductor industry from the era of sub-micron to the present sub-nano regime. The fundamental principle of MOSFET was proposed by Julius Edgar Lilienfeld in the year 1925 which performs the basic operations of amplification and switching of electronic signals. The name MOSFET itself gives a clue to the MOS capacitor-based working principle of the device

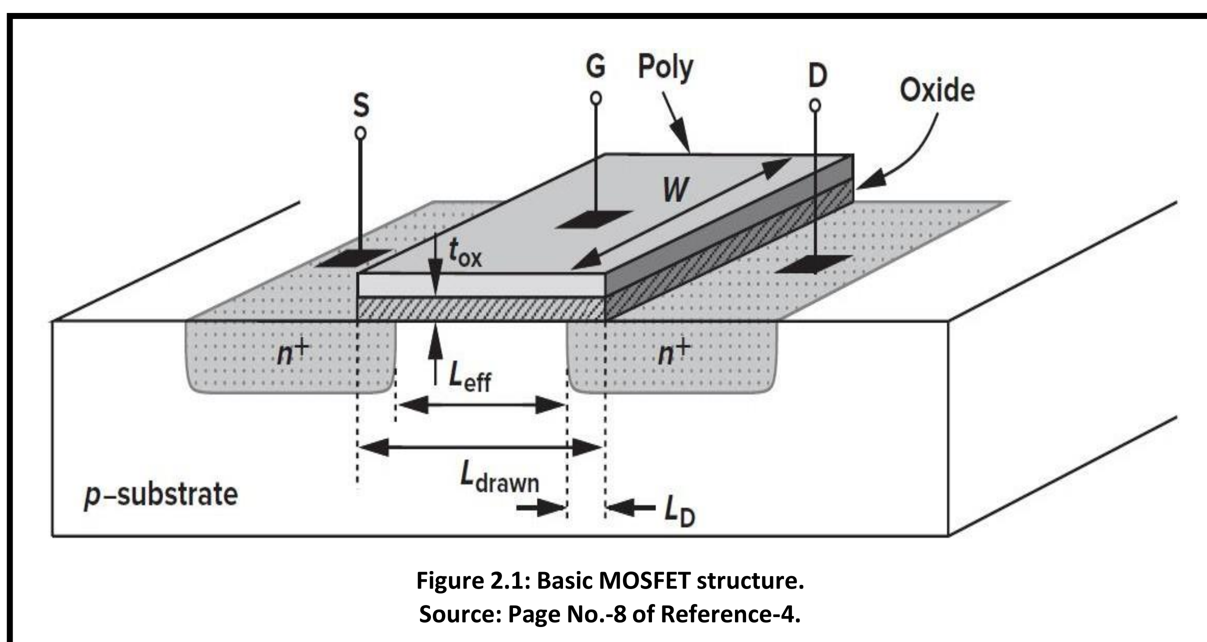


Figure 2.1: Basic MOSFET structure.
Source: Page No.-8 of Reference-4.

with the silicon dioxide (SiO_2) dielectric layer being sandwiched between the metal gate electrode and bulk silicon substrate that act as terminals/plates of the capacitor. The schematic of the basic MOSFET structure is shown in figure 2.1. MOSFET has four terminals depicted as the heavily doped source and drains, metal gate and lightly doped silicon body.

Depending on the dopants type at the source and drain regions determines the type of MOSFET, which can be categorized as p-channel and n-channel. p-type substrate and heavily doped source/drain with n+ impurities realize n-channel MOSFET where electrons act as majority carriers in the induced channel. Similarly, for p-type MOSFET, holes act as the majority carriers within the induced p-channel where the n-type substrate and p+ source/drain forms the basic structure. The conducting channel is actually a layer of inversion charge formed at the interface of oxide-semiconductor and bears the flow of carriers from the source towards the drain region on the application of suitable drain biasing. An n-channel MOSFET with heavily doped n+ source and drain regions being diffused into the lightly doped silicon substrate is presented in figure 2.2. SiO_2 dielectric layer is grown over the silicon body between the source and drain regions followed by metal gate deposition to dielectrically insulate the gate electrode from the device. This isolation ensures high input impedance of MOSFET in order of Mega ohms or approximately infinite preventing the flow of carriers from the gate to the device itself. MOSFET has also termed the gate-controlled resistor where the induced channel and its conductivity depend upon the gate potential and its variation respectively. The device is symmetrical with respect to source and drain which is doped with the same dopants and can be interchanged easily depending upon the direction of current flow within the device as per the externally applied bias. However, the high input impedance of the device induces considerable

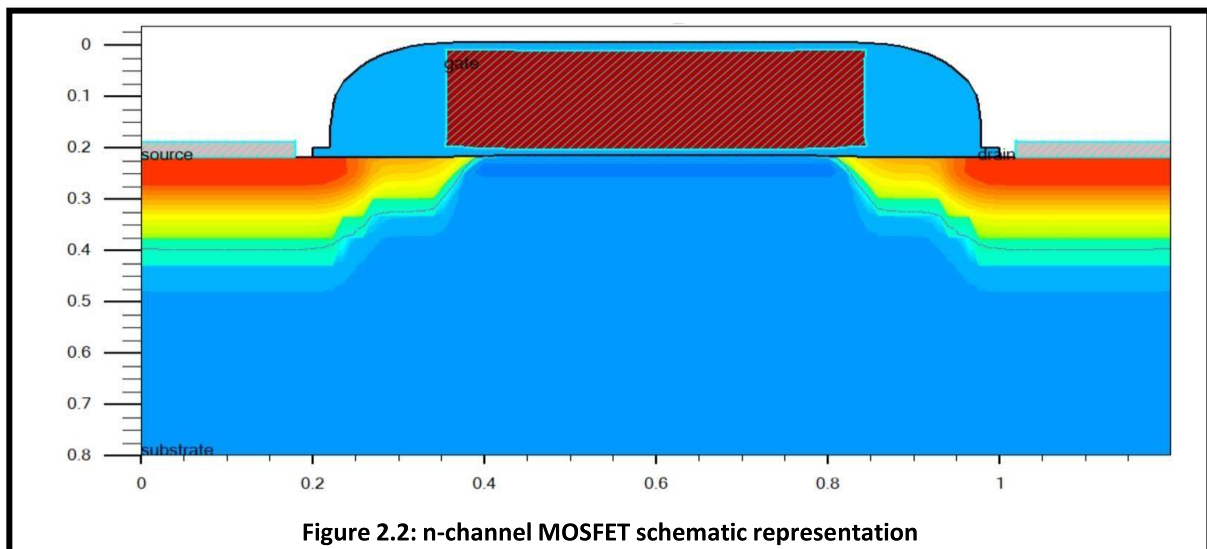


Figure 2.2: n-channel MOSFET schematic representation

static charges that may hamper the functionality of MOSFET unless taken care of or handled cautiously [2.3],[2.5]

2.1.2 Types of MOSFET

From the principle of the channel formation process, MOSFET can be limited to two types

- Enhancement mode or e-MOSFET.
- Depletion mode or d-MOSFET [2.4],[2.6].

2.1.2.1 Enhancement mode MOSFET (e-MOSFET)

Figure 2.3 (a). show the basic structure of an n-channel Enhancement mode MOSFET, its undoped channel region that remains non-conductive under zero bias gate conditions. Figure 2.3 (b) shows the transfer characteristics (I_{DS} vs V_{GS}) of n-channel e-MOSFET. It is evident that until the V_{GS} exceeds the value of V_{th}, the current through the device is zero. This is because of the non-existence of channel for the source to drain. Even an increase in V_{DS} will not result in any current flow called the cut-off region of e-MOSFET. Once V_{GS} crosses V_{th}, the current I_{DS}

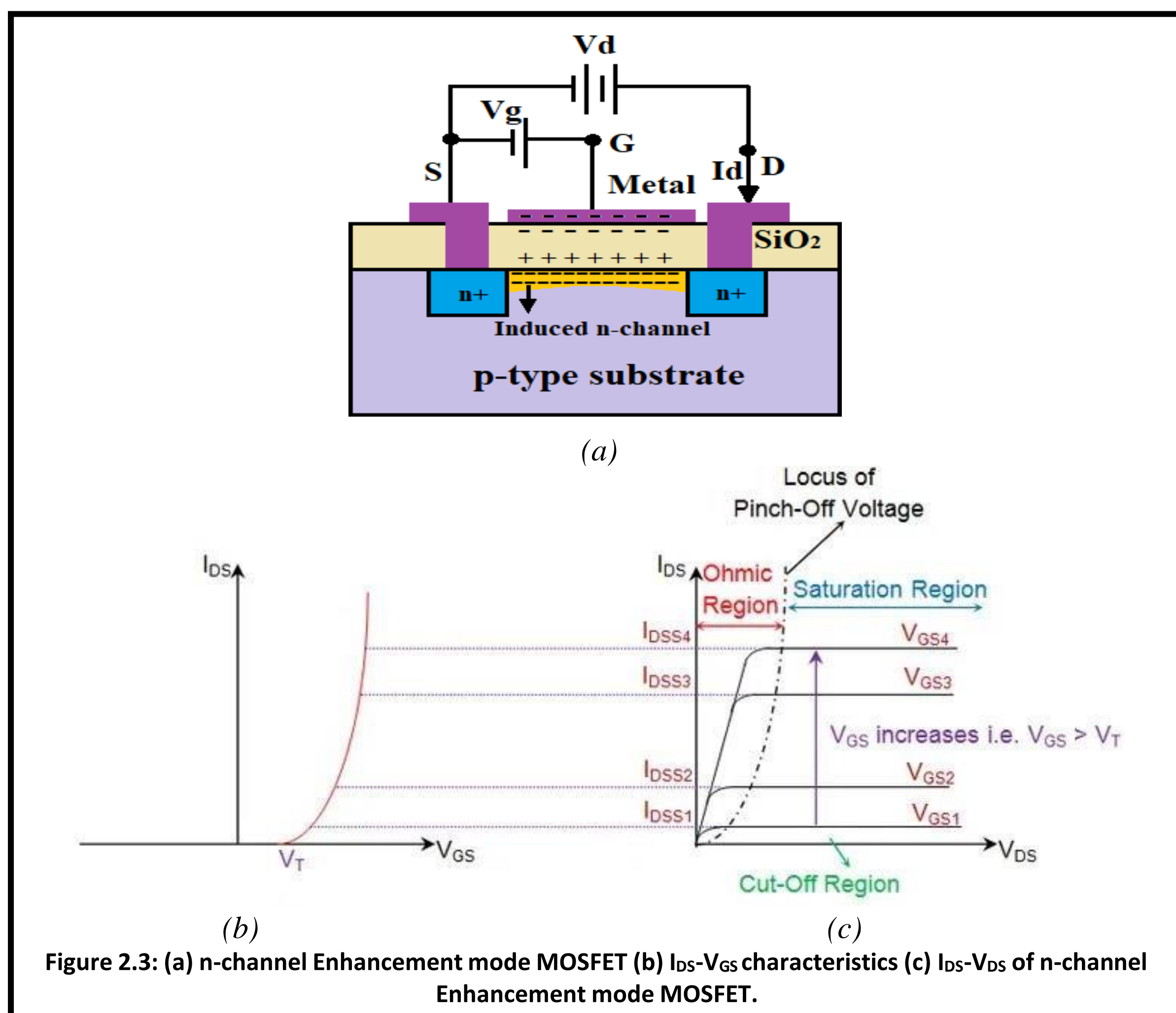


Figure 2.3: (a) n-channel Enhancement mode MOSFET (b) I_{DS}-V_{GS} characteristics (c) I_{DS}-V_{DS} of n-channel Enhancement mode MOSFET.

starts to flowing (Ohmic region) and then get saturates (saturation region of operation). Figure 2.3 (c) shows that where I_{DSS2} is greater than I_{DSS1} as $V_{GS2} > V_{GS1}$, $I_{DSS3} > I_{DSS2}$ as $V_{GS3} > V_{GS2}$ and so on.

2.1.2.2 Depletion mode MOSFET or d-MOSFET

The existence of the small same type of doped region as like source and drain below the gate connecting the source and drain regions makes depletion-mode MOSFET or d-MOSFET. It acts as a ‘normally switched on’ device and a suitable gate voltage is required to switch the device to the OFF-state condition as shown in figure 2.4 (a). The transfer characteristics shown in figure 2.4 (c) indicate that even though V_{GS} is 0V there is current flowing. This indicates that the device conducts even though the gate is left unbiased. The current through the MOSFET increases with an increase of V_{DS} (Ohmic region) until V_{DS} becomes equal to the pinch-off voltage (V_P), I_{DS} will get saturated to a particular level I_{DSS}. Further, the locus of the V_P shows that V_P increases with an increase in V_{GS}. The conduction through the device will stop as it gets deprived of its n-type channel if then V_{GS} must be negative and equal to -V_T, shown in figure 2.4. (b).

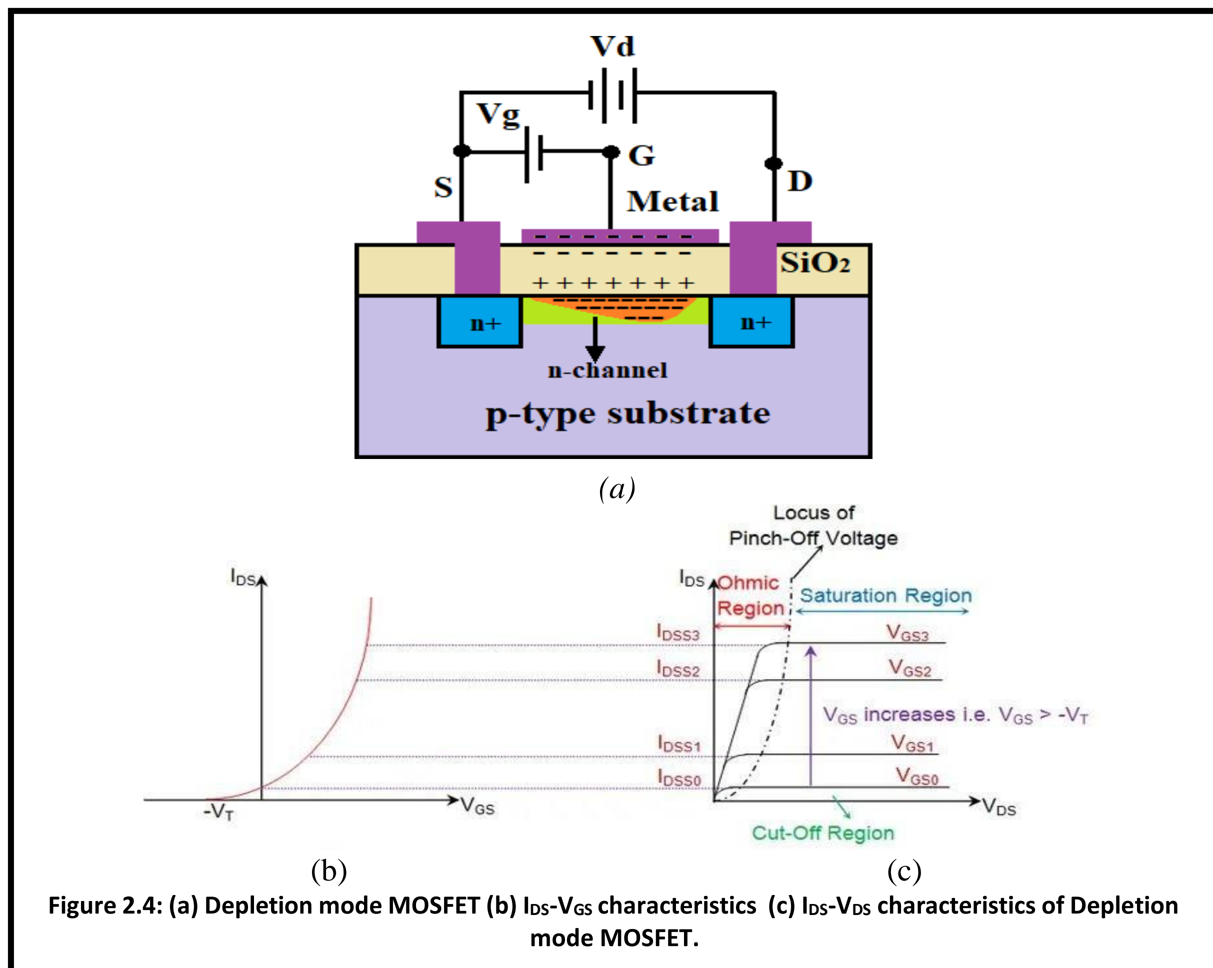


Figure 2.4: (a) Depletion mode MOSFET (b) I_{DS}-V_{GS} characteristics (c) I_{DS}-V_{DS} characteristics of Depletion mode MOSFET.

The opposite behaviour is exhibited by p-channel d- MOSFET. This type of device bears a close resemblance to JFET with a low resistance channel extending between the source and drain and pre-doped with electrons and holes for n-channel and p-channel devices respectively. However, the conductivity of d-MOSFET is much less relative to the enhancement mode counterpart.

The explanation provided above can be visualised in the following table 2.1.

Kind of MOSFET	Region of Operation		
	Cut-Off	**Ohmic/Linear**	**Saturation**
n-channel Enhancement-type	$V_{GS} < V_T$	$V_{GS} > V_T$ & $V_{DS} < V_P$	$V_{GS} > V_T$ & $V_{DS} > V_P$
p-channel Enhancement-type	$V_{GS} > -V_T$	$V_{GS} < -V_T$ & $V_{DS} > -V_P$	$V_{GS} < -V_T$ & $V_{DS} < -V_P$
n-channel Depletion-type	$V_{GS} < -V_T$	$V_{GS} > -V_T$ & $V_{DS} < V_P$	$V_{GS} > -V_T$ & $V_{DS} > V_P$

TABLE 2.1: MOSFET REGION OF OPERATION

2.1.3 Operational regions of MOSFET

The operation of MOSFET can be explained by the theory of MOS capacitor [2.6]. Considering n-channel Enhancement MOSFET shown in figure 2.5 (a), a positive gate voltage will induce positive charges, being accumulated at the gate surface acting as one plate while corresponding negative charges are induced in the opposite plate of the p-type substrate at the oxide/semiconductor interface as shown in figure 2.5 (b). The negative charges are due to the minority carriers (electrons) and are dependent on the gate bias. Hence, with an increase in gate voltage, a greater number of minority carriers are attracted thereby decreasing the hole density below the gate region. As V_G increases, the width of the depletion region, as well the potential at the oxide-silicon interface, also increases. The structure resembles a voltage divider consisting of a gate oxide capacitor and a depletion-region capacitor as shown in figure 2.6 (c).

The condition of 'channel inversion' is achieved on further increase in gate bias where the presence of a large number of free electron carriers decreases the effective channel resistance and contributes to devise current with appropriate drain bias shown in figure 2.5 (d). The MOSFET operational regions depending upon the applied gate voltage are enlisted below and also illustrated in figure 2.6.

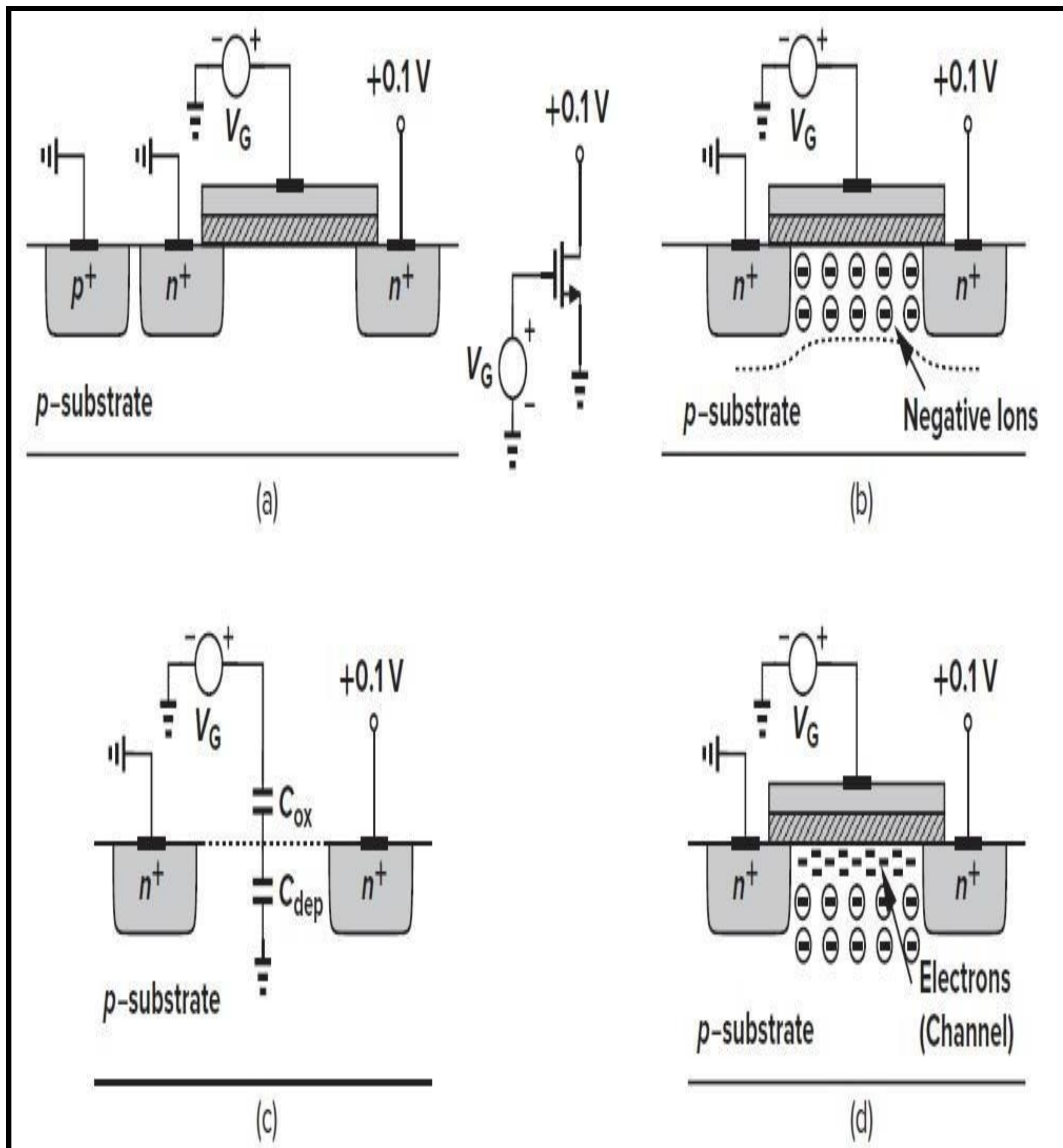


Figure 2.5:(a) MOSFET driven by a gate voltage (b) depletion region formation (c) onset of inversion; (d) formation of the inversion layer

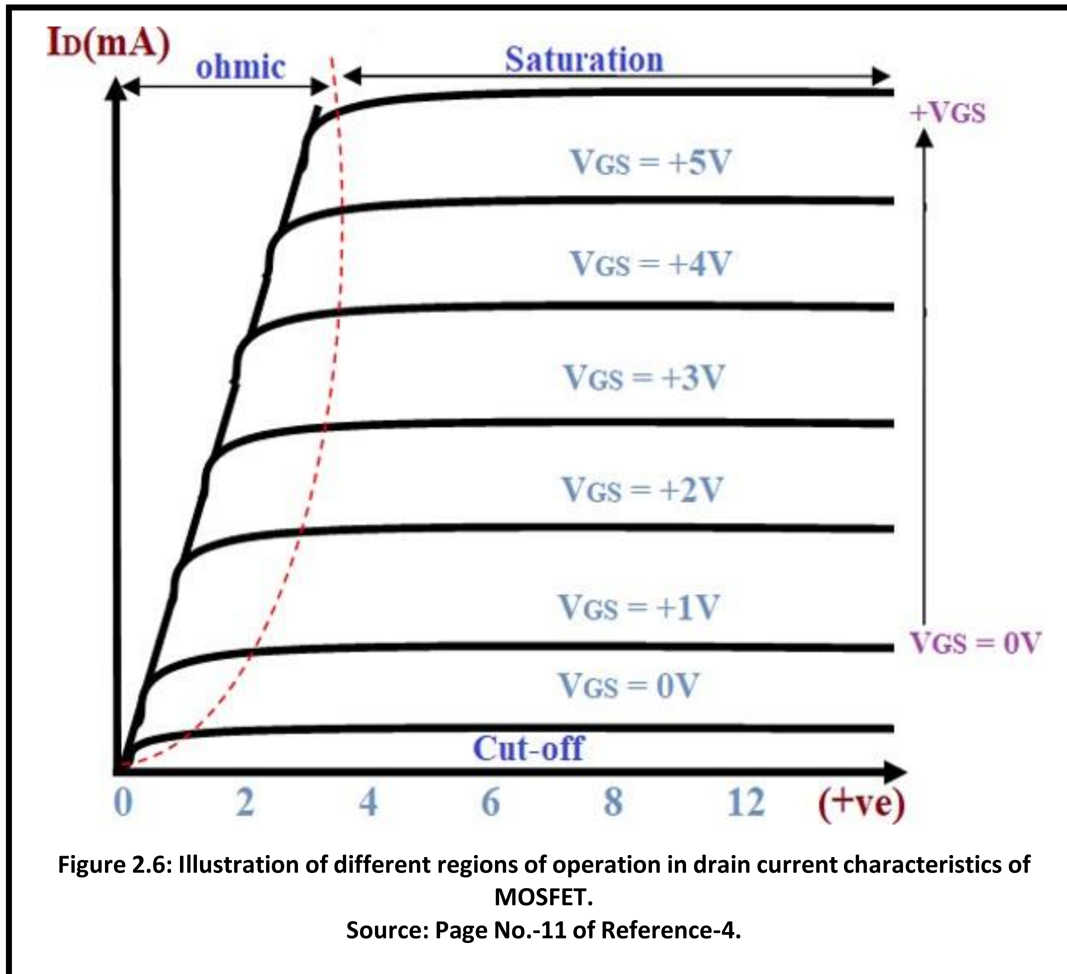


Figure 2.6: Illustration of different regions of operation in drain current characteristics of MOSFET.
Source: Page No.-11 of Reference-4.

a. **Cut-off region**: MOSFET will be in the OFF state, there will be any current flow in this region. MOSFET acts as an open switch and can be used whenever to function as electronic switch.

b. **Ohmic or linear region:** MOSFETs can be used as an amplifier in this region where the current I_{DS} increases with an increase in of V_{DS}.

c. **Saturation region:** In this region I_{DS} is constant. If increase in V_{DS} and once V_{DS} exceeds the value of V_P the device will act like a closed switch and a contend I_{DS} will flow. Whenever performing switching operations required this region is considered.

2 .1.4 Complementary Metal Oxide Semiconductor (CMOS)

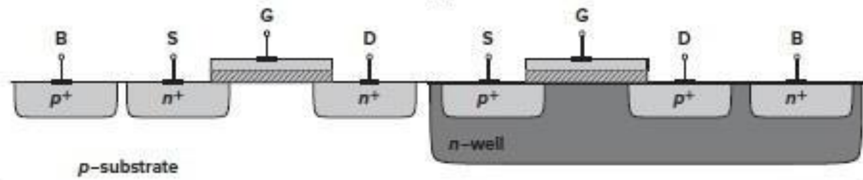


Figure2.7: Representation of Complementary Metal Oxide Semiconductor (CMOS)

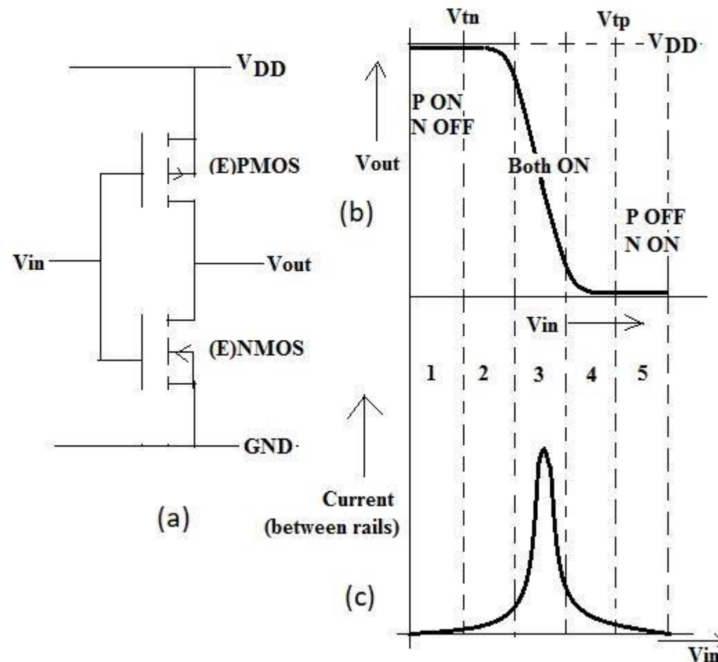


Figure 2.8: Representation of (a) CMOS Circuit Configuration (b) Transfer Characteristic (c) CMOS inverter current vs Vin

One hybrid device that can be constructed incorporating both P-MOSFET and N-MOSFET in complementary mode results in CMOS (Complementary metal-oxide-semiconductor) is represented in Figure 2.7. Since the input is applied at the node connecting both the gates, only one MOS is ON at a time. Such complementary nature of the MOSFET makes OFF-state leakage current loss effective for steady-state. Figure 2.8 represents the (a)CMOS Circuit Configuration (b) Transfer Characteristic (c) CMOS inverter current vs Vin. Added features e.g., low static power consumption and noise immunity make CMOS more popular for an integrated circuit. Low dc power dissipation is the key feature behind the popularity of CMOS circuits in complex digital computation ICs making them a natural choice in portable applications where battery life is an important factor. Moreover, low power dissipation is very much desired in highly dense circuitry. Several transistors are

conglomerated on a single chip to realize complex circuits. Under such circumstances, total IC power dissipation is very critical to maintaining room-temperature operating conditions. As the

temperature increase, silicon becomes intrinsic! Thus, instead of depending on the doping condition (as expected from extrinsic silicon), the free carrier concentration within the conduction band is hugely contributed by the inter-band thermal generation resulting in device oversight. Even utilizing extensive heat-sinking techniques, it is hardly possible to dissipate entire waste heat. This leads to inviting CMOS to establish low power dissipation-based circuit for proper thermal management.

2.1.5 Power Dissipation in CMOS

Power Dissipation is a prime factor in the semiconductor industry. As we know that the energy cannot be destroyed, it does lose through work or dissipated as heat. Therefore, it is important to know how much electrical power does a device consumes? Power dissipation by any semiconductor device is classified into two types – dynamic power and static power. From figure 2.9 it can be justified that for a device having channel length is smaller than 90nm, static power (leakage power) is the dominant factor, whereas for larger geometries, dynamic power (switching power) is the dominant factor [2.7] . Figure 2.10 shows that the total power is the combination of switching activity, capacitance, voltage, and the transistor structure.

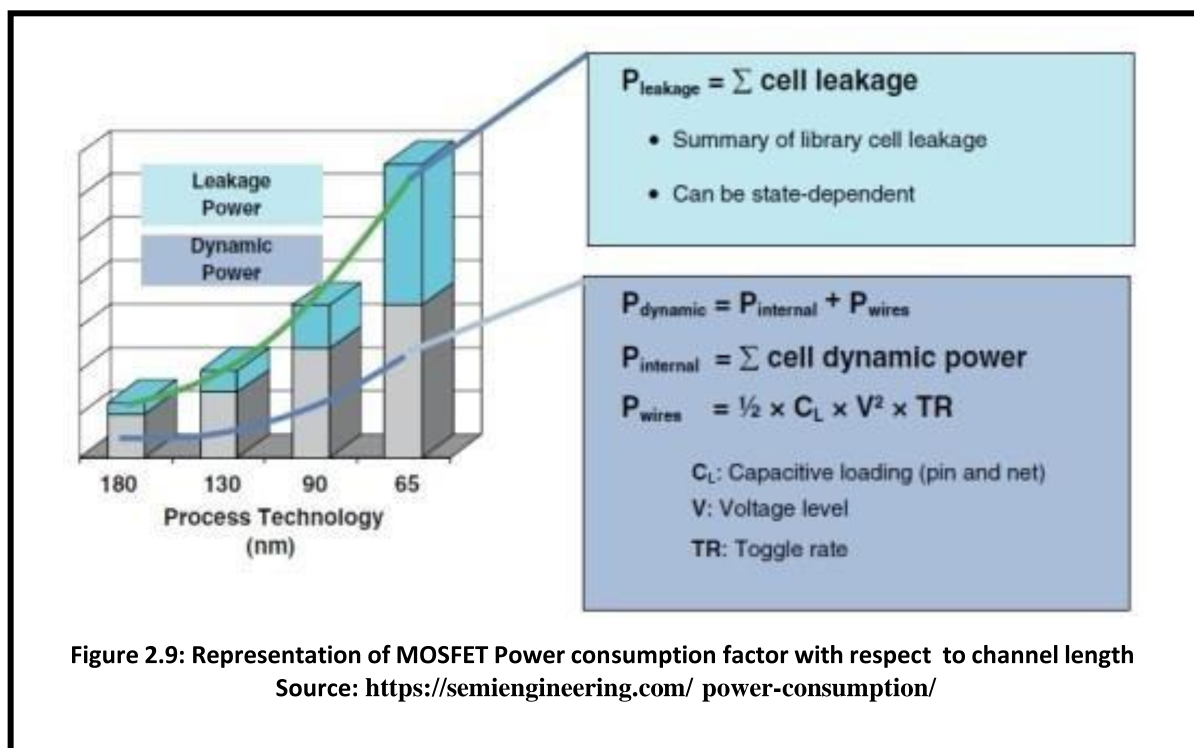


Figure 2.9: Representation of MOSFET Power consumption factor with respect to channel length
Source: https://semiengineering.com/ power-consumption/

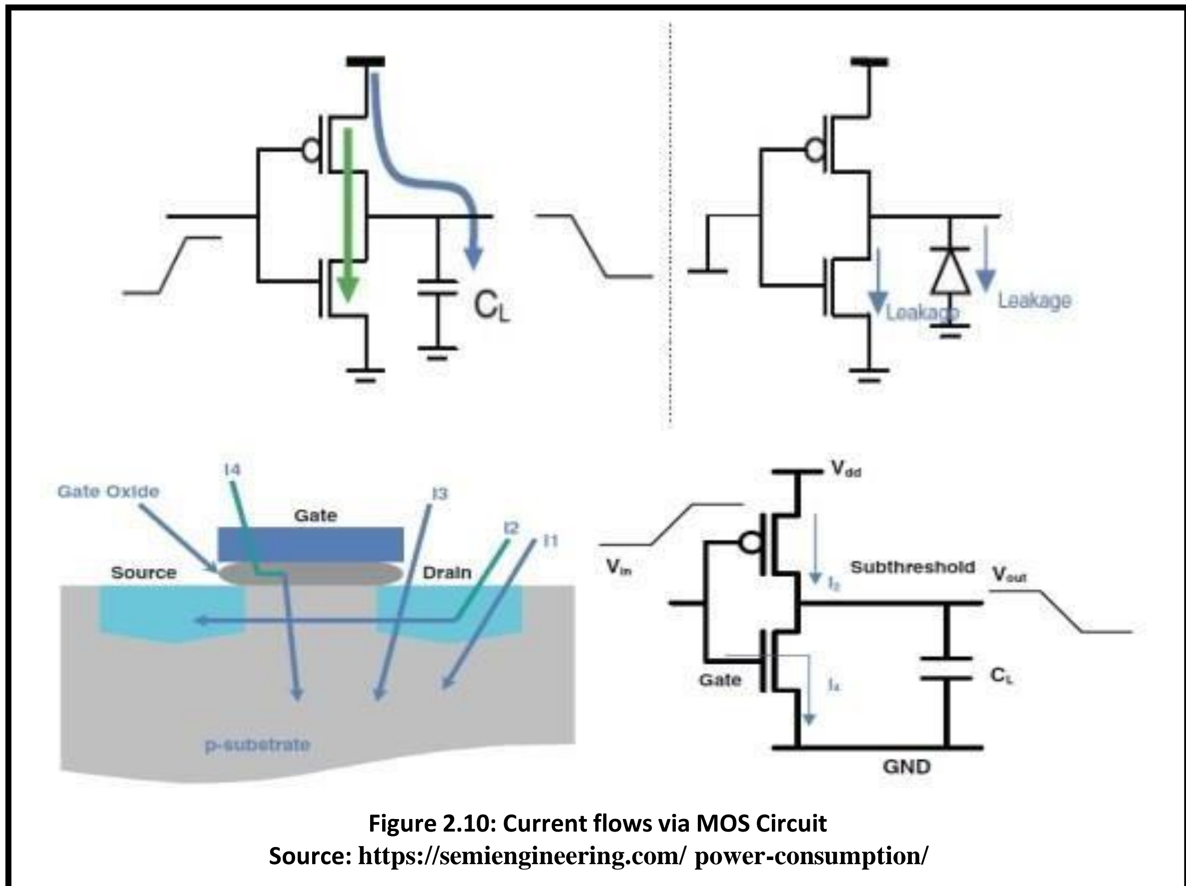


Figure 2.10: Current flows via MOS Circuit
Source: https://semiengineering.com/ power-consumption/

The summation of both the dynamic and static power is non but the total power consumption and can be represented as

$P_{Total} = P_{Dynamic} + S_{tatic}$

Where $P_{Dynamic} = P_{switching} + P_{short\text{-}circuit}$

$P_{switching} = \alpha . f\, C_{eff}\, V_{dd}^2$

where α = switching activity

f = switching frequency

C_{eff} = the effective capacitance

V_{dd} = the supply voltage.

$P_{short\text{-}circuit} = I_{sc} . V_{dd} . f$

Where I_{sc} = the short-circuit current during switching,

V_{dd} = the supply voltage and

f = switching frequency.

$P_{Static} = f\,(V_{dd}, V_{th}, W/L)$ is a function of the supply voltage V_{dd}, V_{th} and transistor size.

2.1.6: Issues with Scaling and Moor's law

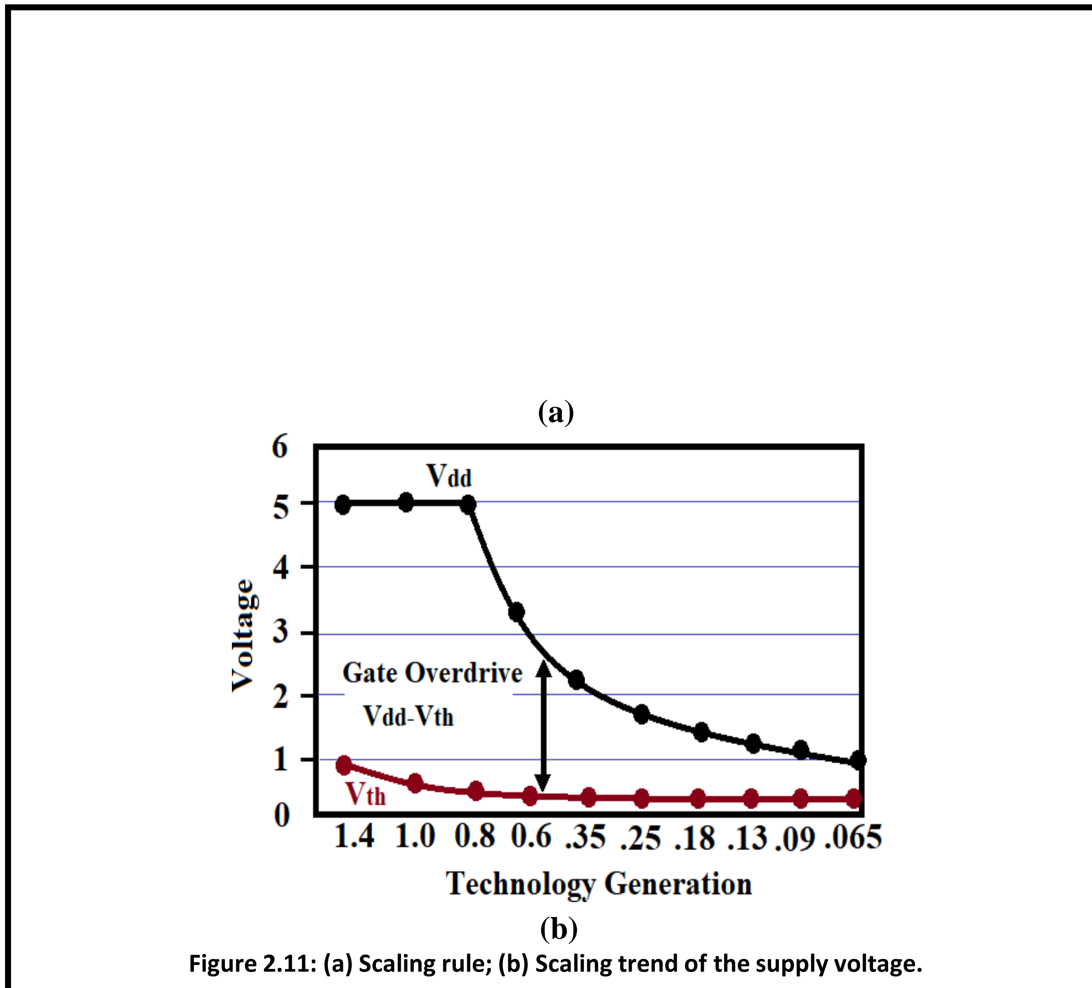


Figure 2.11: (a) Scaling rule; (b) Scaling trend of the supply voltage.

As per the scaling rule of MOSFET published by Dennard [8], the scaling parameter α is used along with a multiplying factor of 1/α. While the doping concentrations are scaled by the factor α, the voltages are multiplied by 1/α to maintain the internal electric field unaffected. Again the speed of the circuit gets boosted by the factor α with consequent lowering of power dissipation by α2. Figure 2.11 (a) depicted the scaling law and the technology trend with scaling are illustrated in figure 2.11 (b). This shows that the threshold voltage reduction does not follow Dennard's Rule because of the gate overdrive. To keep pace with the scaling trend, the device feature size is scaled every year and the number of transistors on the chip gets doubled every two years as predicted by Moore's law. This is reflected in the evolution of nanotechnology and nano-electronics from micro-regime as transistor feature size is scaled from micrometre to 100nm orders. However, the major hindrance related to this high integration density is enhanced power consumption. Researchers are continuously trying to adopt alternative methods to reduce power consumption. But every method has its own pros and cons.

The increase in clock speed creates a thermodynamic challenge that makes it hard to cool flat dense ICs using a fan. In 2000, Intel's Pentium 4 had a power density of 46 watts/cm^2 [9]. Shrinking the feature size or increased chip performance and faster IC. But by 2005 increases in clock speed came to a halt can be seen in figure 2.12. As the device industry was forced to limit the clock speed as it is unable to cool the estimated 200W/cm2 of power or twice that of a reactor. So thus, the industry has shifted its focus on larger caches and multi-core parallelism, allowing an IC to execute more instructions per clock cycle [2.10].

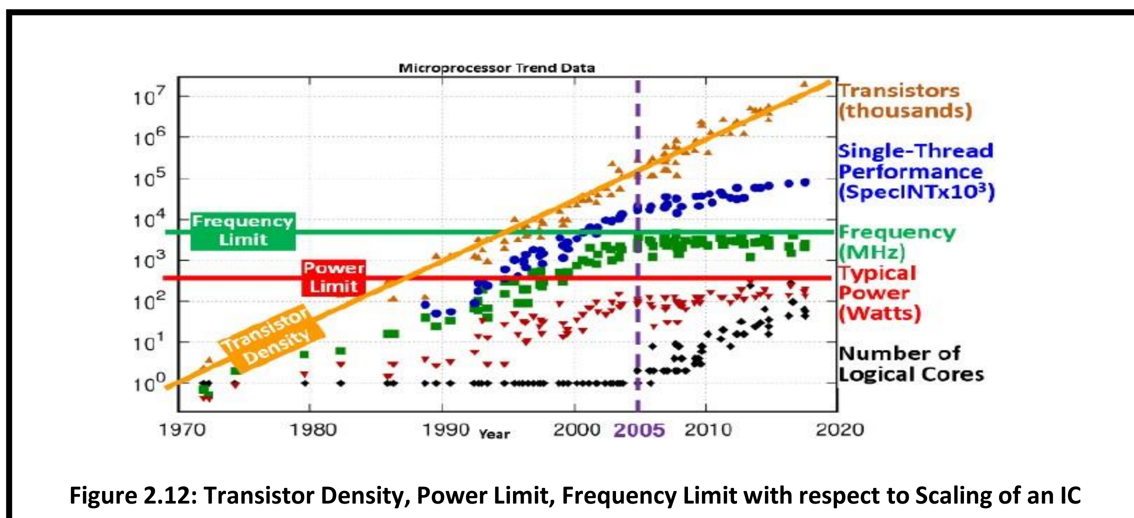


Figure 2.12: Transistor Density, Power Limit, Frequency Limit with respect to Scaling of an IC

It is certain to pay some price to reap the revolutionary benefits (development of device scaling through various technology nodes and the associated advantages) realizing high speed and higher package density integrated circuits. Figure 2.13 gives a glimpse of the Logic device and Shrinking roadmap for the futuristic devices. The gate electrode gradually loses its sole control over the channel region [2.11-2.12] with the adoption of aggressive scaling giving rise to the charge sharing phenomenon between the source and drain regions. As an effect of this, the drain field (the horizontal one) dominates the vertical field making the threshold voltage and sub-threshold slope functions of channel length. Some of the salient short channel effects can be summarized as the Drain Induced Barrier Lowering (DIBL), Threshold Voltage Roll-Off (TVRO), random doping fluctuations and high field-induced Hot Carrier Effects (HCEs). Contemporary research in the field of nanodevices is mainly dominated by the urge to discover innovative strategies to prevent these short channel effects. At the same time, true fabrication and manufacture of such immoderately miniaturized devices have stood as practical challenges to realize the progress of the scaling trend. Further, formidable challenges are also encountered in the design, testing and packaging of integrated circuits containing billions of transistors. In

spite of these difficulties in miniaturization, progress may still be kept unhindered through progressive refinements in IC technology (CMOS technology) with simultaneous fabrication feasibility to stand with these scaled devices for real-time application.

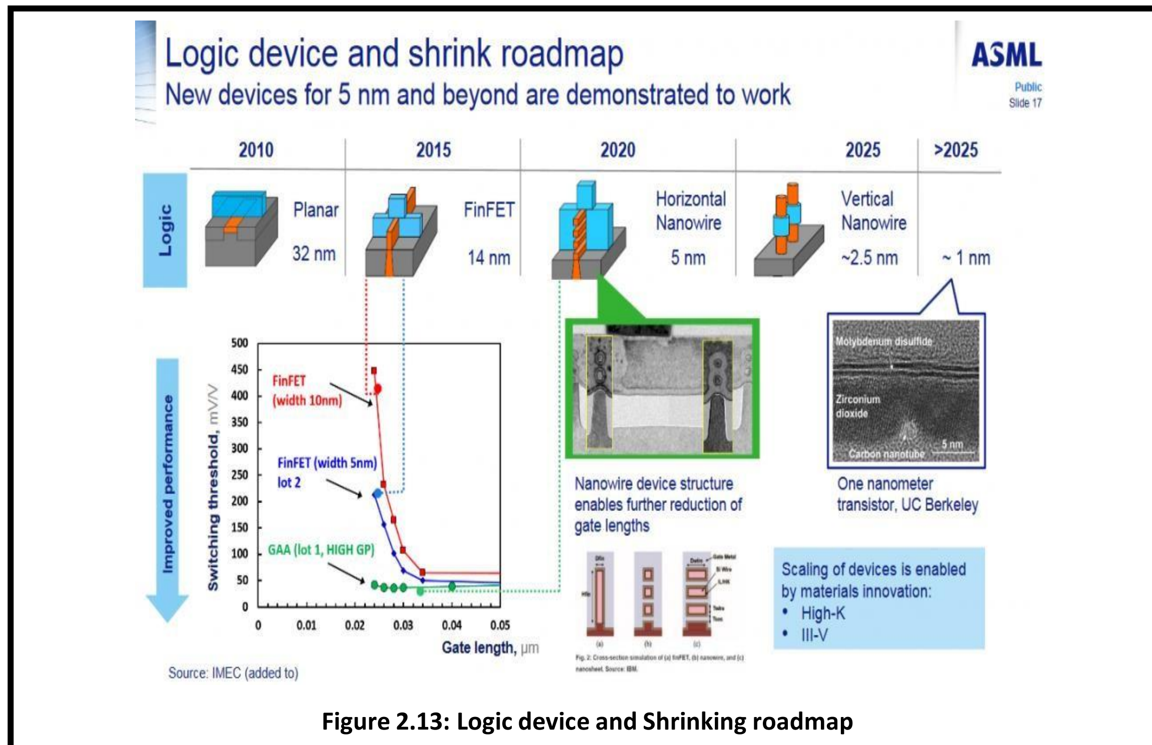


Figure 2.13: Logic device and Shrinking roadmap

2.1.7 Short Channel Effects in MOSFET

Short channel phenomena associated with FET devices arise with the dimension of effective channel length (L_{eff}) approaching source and drain junction depths. Thus, a number of undesirable effects [2.13] crop up which negatively impact device performance in the short channel domain. Usually, for a long channel device, the dominant field is the vertical electric field due to enhanced gate control on the electrostatic of the channel. But, in a short channel device, the transport of charge carriers in the channel between the source and the drain gets affected by both vertical and horizontal (due to the application of drain voltage) electric fields, thus reducing its transconductance value. This also restricts the realization of the simple one-dimensional Gradual Channel Approximation (GCA) technique to account for device characteristics. The physical significance of these two-dimensional electric fields, termed as SCEs, is now being discussed vividly as follows:

2.1.7.1 Drain Induced Barrier Lowering and Threshold voltage roll-off

It is observed a sharp decrease in the device threshold voltage as a function of drain voltage with a corresponding decrease in channel length for short-channel MOSFETs. The

effect is called DIBL [2.14] which manifests as threshold voltage roll-off (TVRO). The source and drain depletion regions approach closer with an incessant reduction in channel length. As the device continues to undergo aggressive scaling, at one point, the gate voltage loses its sole control over the total channel charge. Naturally, a lower gate voltage is enough to cause 'channel inversion' condition establishing a threshold state. This makes clear that there is a considerable reduction in the device threshold voltage with a lowering of the potential between source and channel due to higher drain bias induction. This physical phenomenon of sub-threshold conduction becomes one of the major short channel effects and is explained in Figure. 2.14. The bottom line is the injection of a large number of carriers into the channel resulting in enhanced OFF-state current.

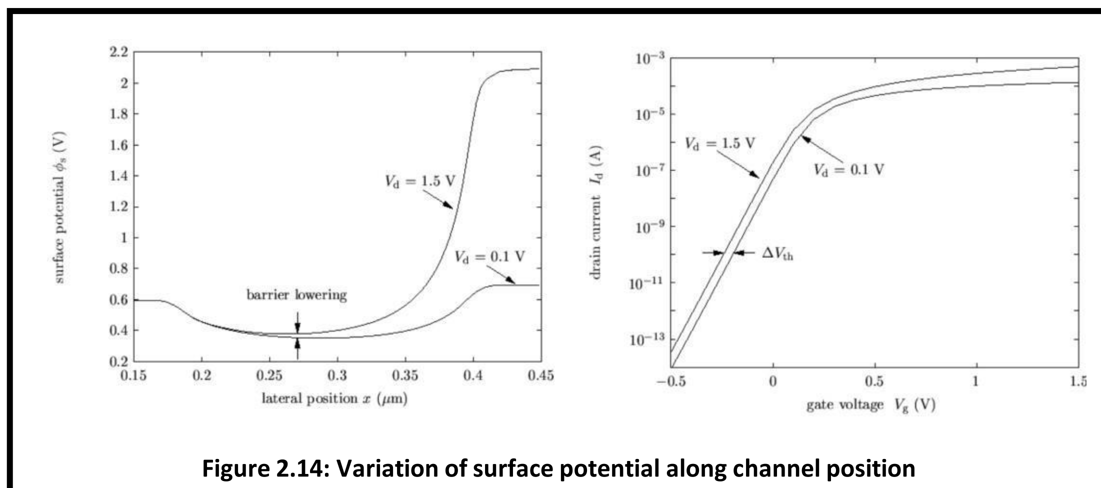


Figure 2.14: Variation of surface potential along channel position

2.1.7.2 Mobility Degradation (Surface Scattering) and Velocity Saturation

The velocity of charge carriers through the inverted channel obeys the relation indicating a strong dependence on the channel electric field. In short channel devices, the electric field within the channel increases considerably with the gradual decrease of the channel due to induced optical phonon emission causing a scattering phenomenon. As a result, the length. This linear relation between carrier velocity and an electric field may no longer exist transit time required by these carriers to move through the channel increases significantly. Drift velocities of both electron and hole saturate with the applied electric field above100 kV/cm. In short-channel devices, the electric field near the drain attains excessive value, close to 400 kV/cm. The ongoing scaling trend not only reduces the channel length, but also decreases the gate oxide thickness. As the gate oxide thickness is scaled down proportionally, the vertical

electric field (due to gate bias directed towards the silicon channel) increases making the transverse electric field dominant. Thus, the carriers flowing in the channel from source to drain gain sufficient energy from this strong transverse electric field, suffer collision and get accelerated towards the oxide-substrate interface. It establishes a surface scattering process resulting in a measurable reduction in carrier mobility.

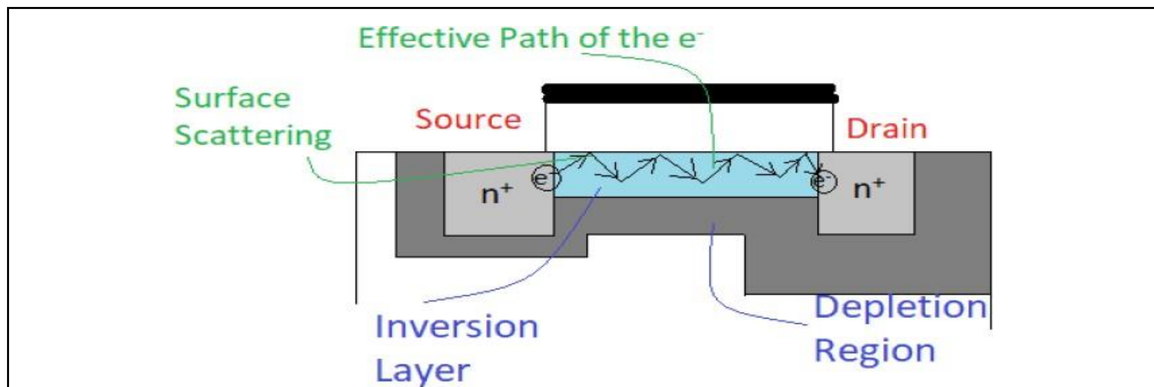


Figure 2.15: Electrons effective path due to surface scattering
Source: https://technobyte.org/non-ideal-iv-characteristics-mosfet-second-order-effects/

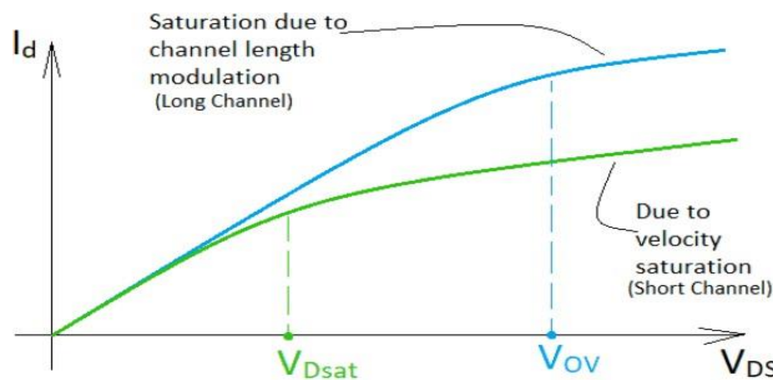


Figure 2.16: Comparison of in short-channel and long-channel device at the onset of saturation
Source: https://technobyte.org/non-ideal-iv-characteristics-mosfet-second-order-effects/

2.1.7.3 Impact Ionization

As discussed earlier, the effect of higher drain bias for low dimensional devices continues to result in another adverse performance called impact ionization promoting SCE. Carriers moving through the channel from source to drain under the effect of the higher electric field at the drain end, gain sufficient kinetic energy to tear out an electron from its bound state in the valence band. This free electron moves into a higher energy state in the conduction band, forming an electron-hole pair. For an ultra-scaled MOSFET, considering the occurrence of electron-induced impact ionization under the dominant channel electric field, most of the electrons get accelerated towards the drain terminal due to the high positive drain bias, while the positive holes reach the substrate to contribute to the parasitic substrate current.

Accumulation of holes generated due to impact ionization in the substrate region causes a voltage drop sufficient to forward bias the normally reverse-biased substrate-source junction. This, in turn, results in the injection of a large number of electrons from the n-type source into the channel eventually increasing the leakage as shown in figure 2.17. These newly injected electrons again come under the influence of a higher electric field near the drain and acquire sufficient kinetic energy to break covalent bonds forming additional electron-hole pairs, thus the process becomes cumulative increasing leakage current and power consumption, thereby further degrading device performance [2.16].

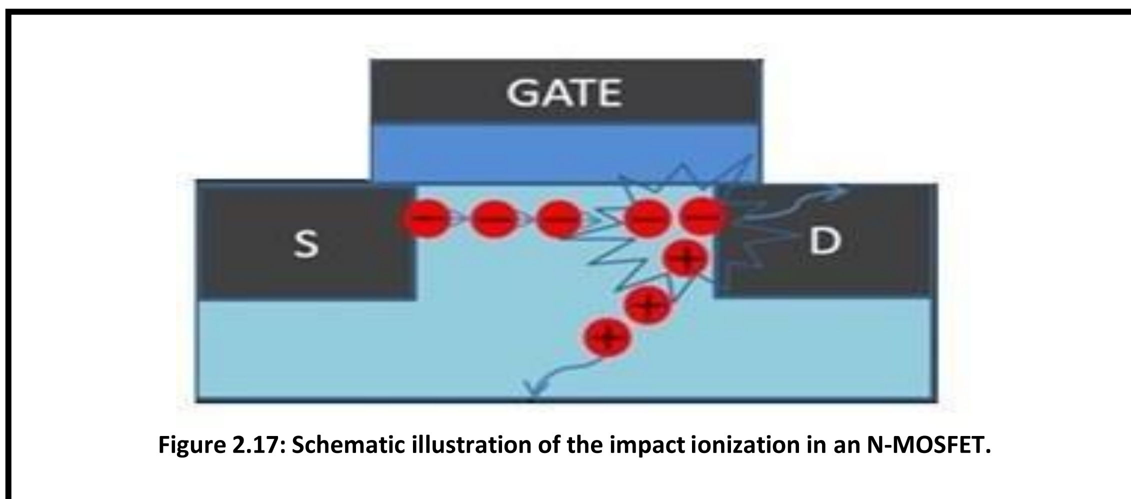


Figure 2.17: Schematic illustration of the impact ionization in an N-MOSFET.

2.1.7.4 Hot carrier effect

The carriers near the drain end become hot enough to penetrate into the gate or substrate under the influence of a strong horizontal electric field (due to higher drain bias) contributing to greater leakage, shown in figure 2.18. It adversely affects mobility. The term 'hot-electron effect' was first explained by Conwell [2.17] to elucidate the behaviour of non-equilibrium electrons in a semiconductor crystal.

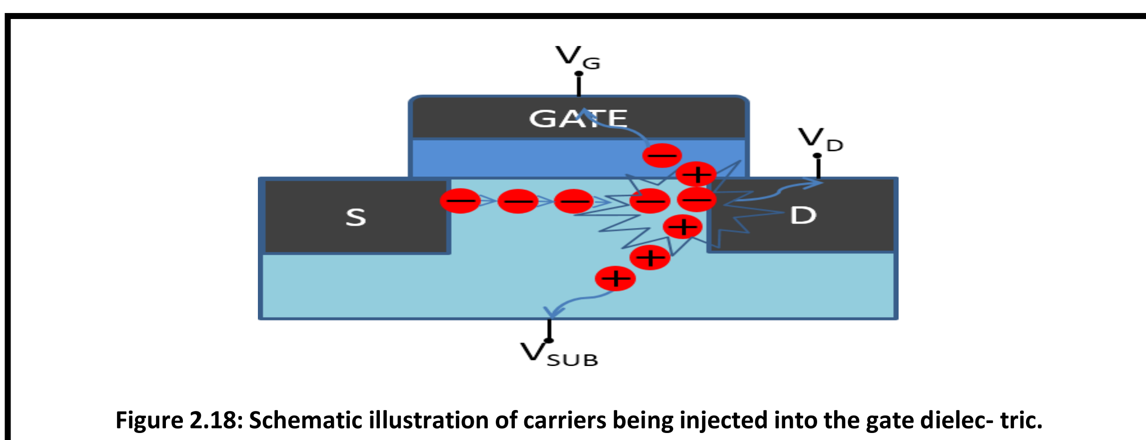


Figure 2.18: Schematic illustration of carriers being injected into the gate dielec- tric.

2.1.7.5 Channel Length Modulation

With higher drain bias for a short channel MOSFET, the depletion region at the drain side widens. Finally, it intrudes into the silicon channel causing a significant reduction in effective channel length. It approximately equals the actual or metallurgical channel length minus the depletion region width at the source and drain junctions. The channel-length modulation (CLM) is a very common short channel effect causing the current beyond saturation to affect the drain or output characteristics of short channel devices. Figure.2.19 clearly illustrates the phenomenon which is more prolific in small devices with low doped substrates. An extreme situation of the above effect on the continuous increase of the applied drain bias widens the drain side depletion region more and more where the source and drain depletion regions seem to touch each other such that the effective channel length almost reduces to zero. This phenomenon is termed punch through. It makes the channel region underneath the gate a function of drain voltage and causes an undesirable rapid increase in the drain current degrading further the device performance.

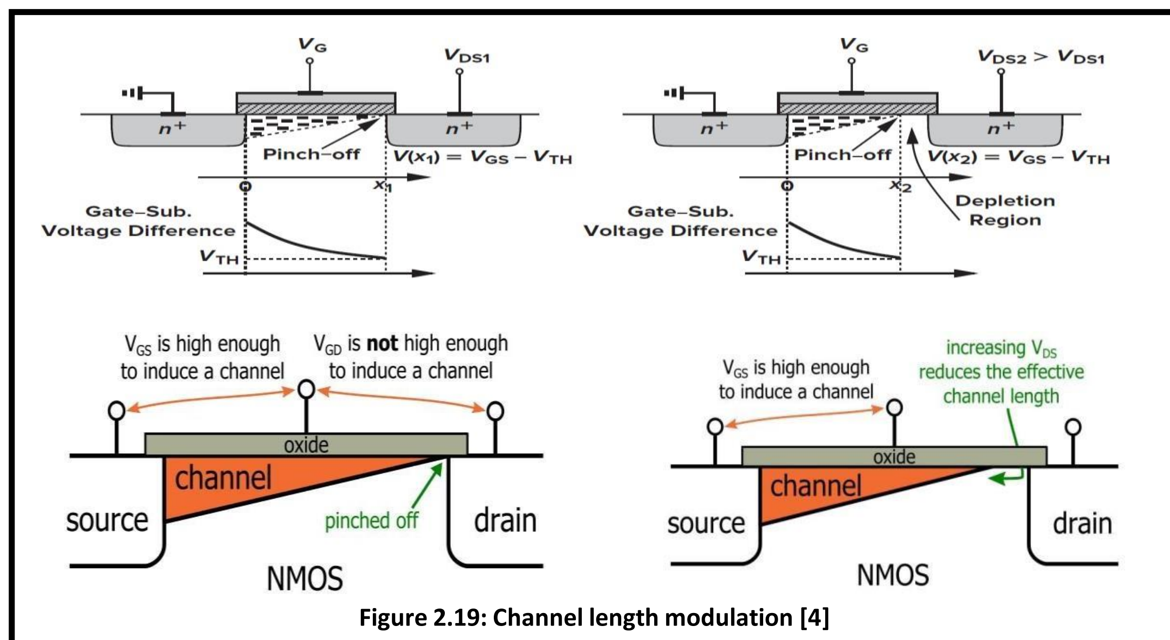


Figure 2.19: Channel length modulation [4]

2.1.7.6 Body Effect (Back Gate Effect)

The Body or the bulk of a MOS is considered to be always grounded (V_B=0) as shown in figure 2.20. If the V_B<0 then there requires lesser V_G for the MOSFET to get saturation compared to conventional conditions. This effect of change in threshold voltage is called the "Body Effect" or the "Back Gate Effect" [2.4].

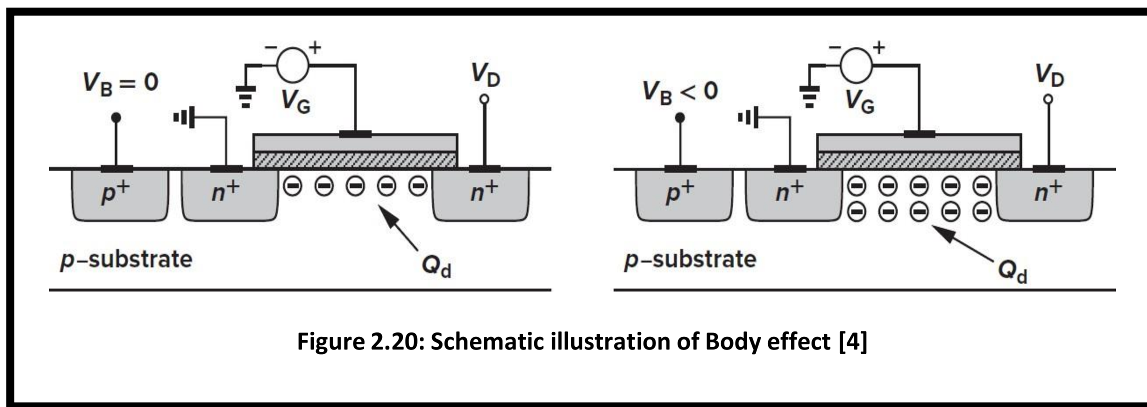


Figure 2.20: Schematic illustration of Body effect [4]

2.1.7.7 Gate Tunneling

Current going into the drain terminal is equal to the current coming out of the source is a MOSFET. As the oxide layer is an insulating material, there can't be current flow into the channel from the gate terminal. This is indeed true for having large oxide thickness. Due to scaling, there is also a need of shrinking the oxide layer. Thus, the probability of an electron tunnelling through the oxide layer and entering the inversion channel arise. So, there is a limit on the minimum thickness of the oxide layer [2.18].

2.1.8. Evolution of advanced MOSFET structures

The aggressive downscaling of planar MOSFET structures suffer from several SCEs which sought the evolution of non-conventional device architectures to keep pace with the scaling trend specified by ITRS. Fabrication complexities and functional limitations of traditional MOS at low dimensions make it unsuitable for implementation in nano-scaled integrated circuits. Further diminution of MOSFET feature size faces various challenging issues in terms of saturation current while lowering the leakage conduction, reducing the power supply and achieving uniform device parameters within the chip. Hence new alternative devices referred to as "non-classical CMOS" with newer structural designs and materials pave a new path toward the explosive growth in the microelectronics industry.

Here, some advanced MOSFET architectures and their structural benefits are described below:

2.1.8.1 Silicon on Insulator (SOI) MOSFET

The main inspiration to switch from conventional MOS to Silicon on Insulator (SOI) MOSFET technology is to widen the scalability of CMOS with enhanced device performance so that they can override the future silicon technology. Like MOSFET, it also maintains silicon

as the starting material for the fabrication of integrated circuits owing to the low cost of silicon and its ability to form a good quality oxide with a smooth interface over the device channel. The exclusive feature of SOI structure is the existence of a thick layer of silicon dioxide (orders of 100 nm) embedded between a thin layer of silicon channel (orders of 10 nm) and the silicon substrate. The thick oxide layer referred to as the buried oxide layer (BOX) can be grown by oxidation or by implantation of oxygen into the silicon wafer. The thin silicon film over the BOX layer is the 'silicon channel' while the relatively thicker silicon layer below the BOX is the 'SOI body'. The cross-sectional view of SOI MOSFET is shown in figure 2.21.

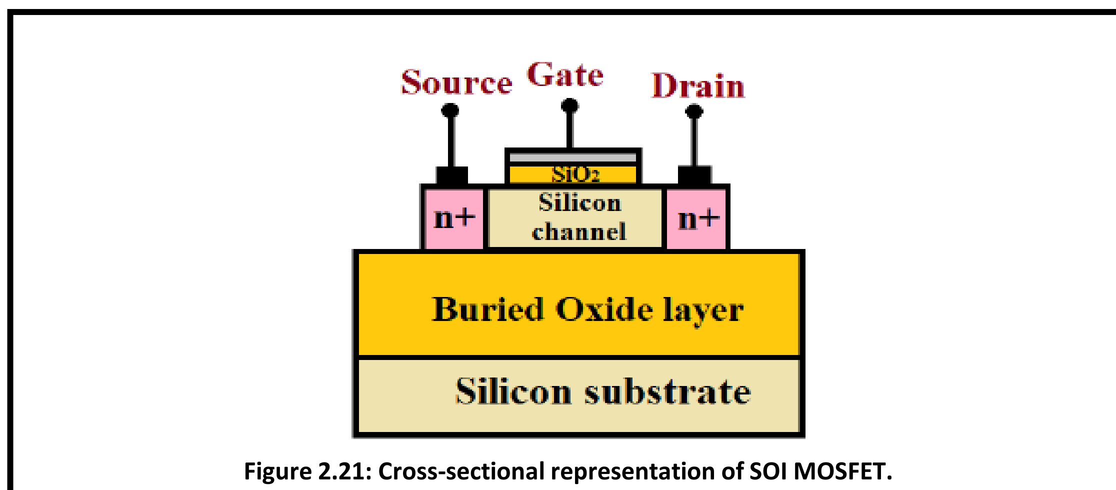


Figure 2.21: Cross-sectional representation of SOI MOSFET.

Depending upon the thickness of the silicon channel, SOI MOSFET can be operated either in the partially depleted (PD) or fully depleted (FD) mode of the regime as shown in figure 2.21. In a partially depleted SOI structure, the depletion region does not fully cover the silicon film hence leaving an undepleted neutral silicon layer even when the device is operating under inversion conditions on the application of suitable bias voltage. Thus, the thickness of the silicon film exceeds the maximum gate depletion width and this undepleted region at the back interface acts as a floating body in PD SOI MOSFET. In contrast to this, in FD SOI MOSFET, the silicon film with a thickness less than the gate depletion width causes the entire silicon channel to be depleted even before achieving the threshold condition. The relatively thinner silicon film eliminates the floating body effects while the presence of very thick buried oxide reduces the junction capacitance in FD SOI. Some of the notable advantages of SOI MOSFET are reduction in source-substrate and drain substrate parasitic capacitance with momentous improvement in speed, power consumption and performance gain of the circuits, additional isolation between adjacent SOI devices due to the existence of a thick BOX layer which in turn facilitates higher package density, prevention in latch-up and latch-up induced

device breakdown, reduction in p-n junction leakage current due to the thin silicon film and its reduced source/drain junction depths, high immunity to SCEs and highly energized radioactive elements being blocked by the thick BOX layer. However, ultra-low dimensional SOI MOSFET performance is also limited by some challenging issues that degrade the short channel characteristics of the device. PD SOI MOSFET exhibits the 'Kink effect' resulting in drain current overshoot in DC circuits due to the combined action of floating body effect and parasitic bipolar effects which are very difficult to suppress. Again, the fabrication of ultra-thin films of FD SOI requires complicated design processing and also excellent interface quality is needed at the BOX/channel interface to reduce scattering. SOI is further subjected to the self-heating phenomenon due to the lower thermal conductivity of silicon dioxide of BOX which has a serious impact on device reliability and performance [2.19-2.25].

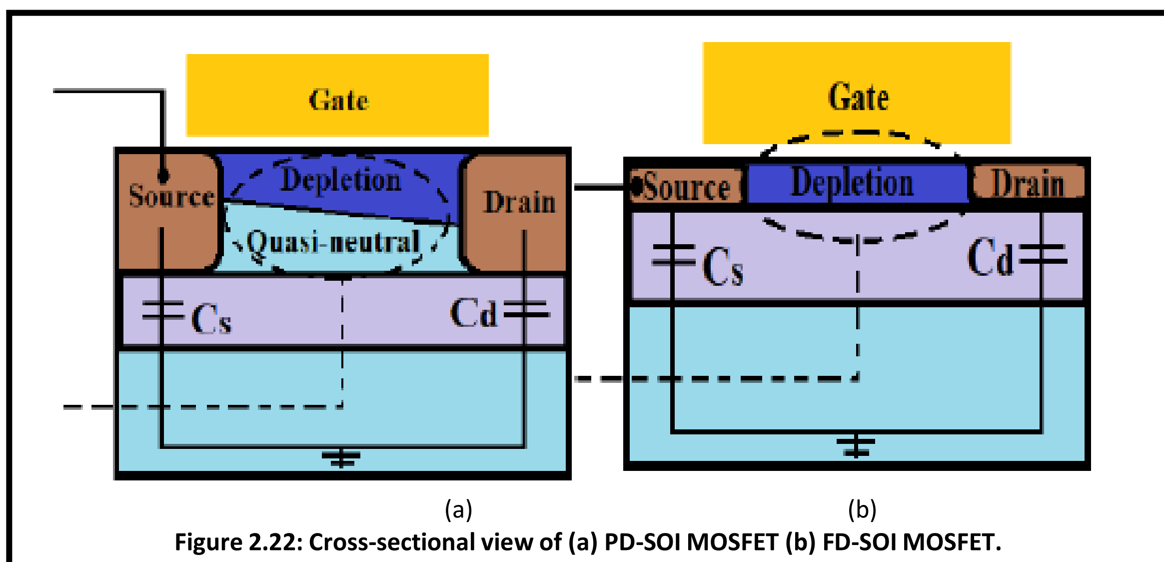


Figure 2.22: Cross-sectional view of (a) PD-SOI MOSFET (b) FD-SOI MOSFET.

2.1.8.2 Silicon on Nothing (SON) MOSFET

Silicon On Nothing (SON) is considered an improvised alternative to SOI MOSFET with enhanced scalability based on the concept of buried layer engineering. In contrast to SOI, the buried oxide layer in SON MOSFET is replaced by an air gap beneath the silicon channel as shown in figure 2.22. Such structure has been proved to provide excellent imperviousness to short channel effects with improved electrical characteristics thereby satisfying the aggressive scaling requirements of ITRS. Figure 2.23 Schematic of Silicon on Nothing (SON) MOSFET. Researchers have explored SON technology both experimentally and analytically as a lucrative option for future low power applications. The lower dielectric permittivity of the buried 'air' layer reduces the parasitic junction capacitance across the source/substrate and drain/substrate junction resulting high speed operating devices. It also offers the highest

electrostatic isolation from undesirable field line penetration to the active channel region. Electrostatic coupling is also reduced through the lower dielectric air layer relaxing the requisite of the ultra-thin silicon film. Additional inherent features of SON include reduced power consumption, immunity to radioactive elements, improved scalability, low noise performance and faster switching performance at a reduced cost [26-31].

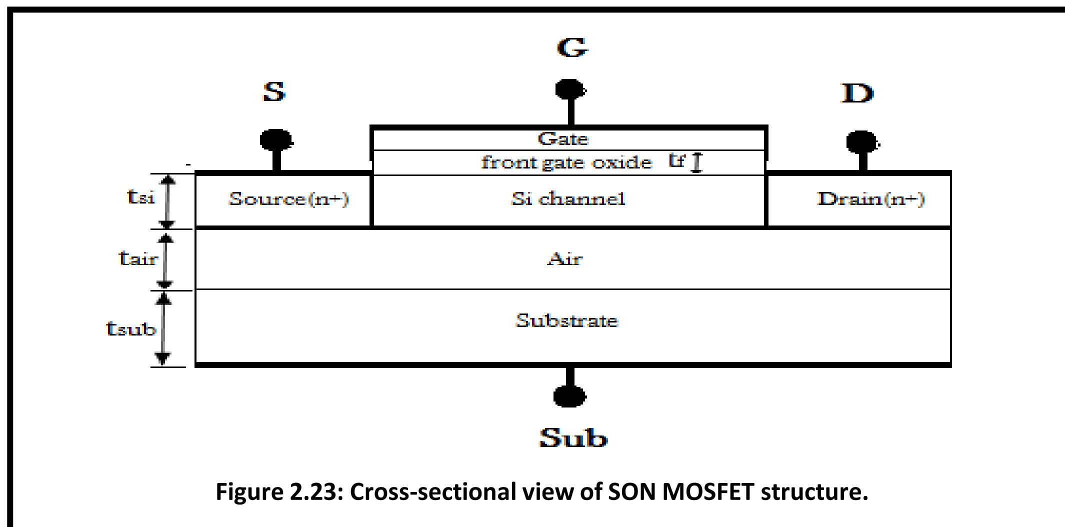


Figure 2.23: Cross-sectional view of SON MOSFET structure.

2.1.8.3 Multi-gate MOSFET

As already discussed, unlike long channel MOSFETs where current conduction is dominated by gate induced electric field, short channel MOSFETs experience two-dimensional charge sharing with gate and drain electric field lines controlling the channel charge. Thus, the sole gate controllability over the device channel is suppressed leading to several inevitable short channel effects. Recently, multi-gate MOSFET structures are emerging as a potential solution to prevent the intrusion of drain side electric field lines into the channel and control the SCEs effectively. The existence of more than one gate increases the driving current capability of the device, improves the subthreshold characteristics and hence enhances the device scalability. Double-gate, tri-gate, FinFET, quadruple gate, and gate all around are some of the special multi-gate configurations of MOSFET structures [2.32-2.39]. The double gate geometry is suggested in 1984 by Hayashi [2.40] to achieve high transconductance and improved subthreshold slope with enhanced gate control. Double gate structures can be operated either as a tied or independent gate. In tied gate mode, both the front and back gates are biased with the same voltage whereas, in independent gate mode, the gate electrodes are independently connected to separate bias voltages. Hence, in independent mode, the front gate threshold voltage is controlled using back gate bias in contrast to tied gate mode, where the

channel charge is controlled by both the gates simultaneously. Although the experimental demonstration of double-gate structures has been reported in the literature, the existence of silicon film between the front and back gates with thickness less than the physical gate length involves complicated fabrication processes and hence commercially not so popular [2.41]. Trigate MOSFET is another popular structure where the active channel is wrapped by the gate on all three sides: the two side surfaces with height H and the top surface with width W. The three surfaces in trigate configuration thus control the channel charge conduction while its corners where the side surfaces meet the top one act as a critical contributor towards device operation. In FinFET, the top surface is covered by a thick layer of oxide and hence does not contribute to the conduction of the channel. FinFET has an aspect ratio higher than tri-gate with 'fin width' being determined by the height and width and 'fin height' being defined by the thickness of the active channel. Such gate structure modulation is further extended to gate all around configuration with gate electrode encircling the channel on all sides. Due to its unique device geometry of gate wrapped channel, the gate electrostatic control and subthreshold behaviour of the device is highly improved with consequent suppression of undesirable short channel effects in comparison to single and double gate counterparts.

2.1.8.4. Gate work function engineering: The emerging performance-boosting technique of scaled devices

It is quite evident from the previous discussion that downscaling of device feature size for progressive growth of the VLSI industry faces the unavoidable detrimental SCEs and associated bottlenecks that are constantly degrading the overall performance of the devices. Hence, to improve the device functional competence, novel device architectures with the modulated material property are being propounded by device engineers and researchers satisfying the aggressive specifications of ITRS requirements. Gate work function engineering is another possible solution to combat the adverse SCEs while enhancing the device performance effectively thereby opening a new research avenue to explore. Recently, metal gates are replacing the standard polysilicon gates and emerging as a suitable alternative to suppress the undesirable SCEs, polysilicon depletion effects, boron penetration, etc. [2.42]. However, metal gates have some inherent limitations including thermal or chemical instability with a high-k gate dielectric, annealing needed to passivate the interface charges trapped unintentionally, problems related to plasma layer damage due to cross-contamination, deposition of material and reactive ion etching (RIE) and adequacy in the availability of metal work-functions [2.43]. In short channel devices, both the horizontal and vertical fields

constitute the resultant electric field at any point of the device. The gate electrodes with two or three metals having dissimilar work functions placed adjacently modulate the vertical electric field at any point in the device channel, thereby controlling the total channel electric field. This popular concept of 'gate material engineering' is termed a dual /triple material gate. The fascinating feature of such gate workfunction engineering lies in the presence of abrupt steps in the potential profile at the interface of the two/three gate metals. The step profile in channel potential aids in lowering the DIBL effect by shielding the potential minima across the source side from any drain bias fluctuations and thus makes the device highly immune to SCEs. The concept of gate material engineering is further extended to the binary metal alloy gate electrode for MOSFET applications as introduced by the research group led by Tsui [2.44]. Recently, ZnCdSSe alloy nanowire with continuous mole fraction adjustment has been fabricated by Pan et al. [45] Another research outcome as reported by Christen et al. has demonstrated the fabrication of continuous compositional spread (CCS) thin film by applying pulsed laser deposition (PLD) and have verified the compositions at each position of the film with analytical values. Several experimental demonstrations of fabricated metal alloy in due course of time establish the feasibility of binary metal alloy as a gate electrode of MOSFET in near future [2.46-2.48]. Deb et al. further explored the idea of spatial composition graded gate electrode in SOI MOSFET where the lateral variation of workfunctions of individual constituent metals has been applied to adjust the overall electric field of the system and to reduce the short channel surface potential asymmetry consequently [2.24]. Since then, several research accomplishments have been reported exploiting the popular scheme of linearly graded binary metal gate electrodes in innovative short channel device architectures to suppress the DIBL effect and boost the nano-scaled device performance [2.49-2.53].

2.2 Introduction to Tunnelling

Tunnelling is a quantum effect in which a particle will pass a potential barrier despite the fact that it lacks the energy to do so. In the case of classical particles, such behaviour is not detected [2.54]. As a result, any conventional analogy used to describe QMT will be inherently incorrect. Rather than using a conventional analogy, it would be more advantageous to imagine the quantum particle as a wave and draw a connection between quantum mechanical behaviour and wave behaviour.

The conductor's free electrons move when an EMW strikes it. The wave loses energy as the electrons gain it, resulting in an energy transition. As a result, as seen in figure: 2.24(a), the wave's amplitude declines exponentially within the substance and soon becomes insignificant. But the wave's amplitude does not degrade to marginal values like previous if a very thin conductor is considered. On the other side of the conductor, as seen in figure: 2.24(b), EMWs of very small amplitude can be observed. If the EMW is replaced by QPs and the conductor with a potential barrier, then a remarkably close condition to QMT can be achieved. A QMP collides with a potential barrier that it lacks the energy to cross, even after that there is a non-zero chance that the particle can be observed on the other side. If the particle can be seen on the other side, then it is said that the particle has "tunnelled" across the barrier, and this effect is referred to as QMT.

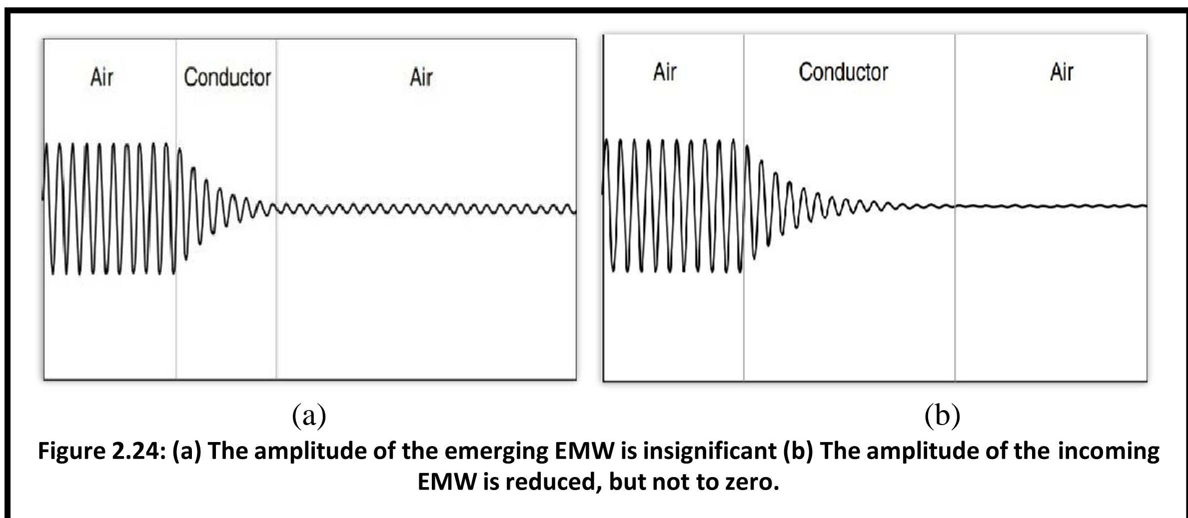


Figure 2.24: (a) The amplitude of the emerging EMW is insignificant (b) The amplitude of the incoming EMW is reduced, but not to zero.

2.2.1 A Brief Introduction to Band-to-Band Tunnelling

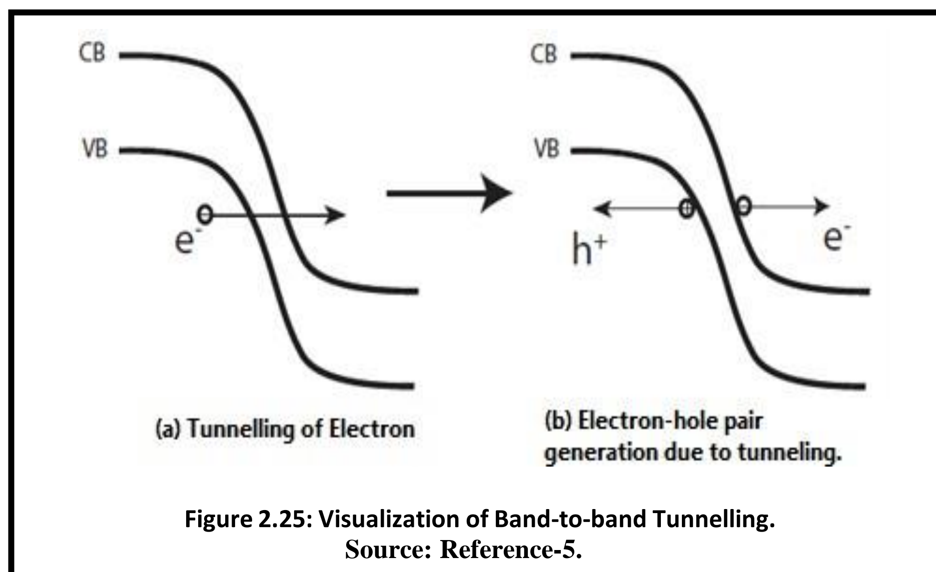


Figure 2.25: Visualization of Band-to-band Tunnelling.
Source: Reference-5.

Now, that we have established a basic understanding of how the tunnelling through a general barrier can be predicted, we can concentrate on how the tunnelling is useful in the view of TFETs. In simple words, the band-to-band tunnelling occurs when electrons from the valence band tunnel across the energy band gap to the conduction band. The band-gap is considered the equivalent to the potential barrier. The band-to-band tunnelling can be shown in figure:2.25. The tunnelling can be direct or indirect in nature.

Direct Tunnelling: This occurs in direct band-gap semiconductors, where the maxima of the valence band are aligned with the minima of the conduction band at the same 'k' value. The tunnelling phenomenon does not require the help of phonon (or photon depending on the case) or traps to occur. Also, the tunnelling does not cause a change in momentum, especially in the direction perpendicular to the direction of tunnelling. This type of tunnelling can be seen in Gallium Arsenide (GaAs) and not in Silicon (Si) and Germanium (Ge).

Indirect Tunnelling: This is observed in semiconductors like Silicon and Germanium, where the top of the valence band doesn't align with the bottom of the conduction band at the same 'k'. The tunnelling process requires a change in momentum, which is achieved by absorbing and releasing phonons (or photons depending on the case).

2.2.2 Band-to-Band Tunnelling Models

The band-to-band tunnelling models can be broadly classified into two types: i. Non-Local Tunnelling models and ii. Local Tunnelling models.

Non-local Tunnelling Models: In these models, Schrödinger's equation (S.E.) is solved with respect to the spatial dependence of the parameters. When external voltage/ bias is applied in semiconductors, the shape of the potential barrier is varied, and the variation might not be simple. Thus, in the case of Non-local models, the solutions might not always end up in a closed-form. The band structure of the semiconductor must be included with the potential ($V(x)$) while solving for S.E. All these spatial complications makes the analytical solution to the S.E. almost impossible, hence these types of model are highly dependent on the Numerical Solutions. Hence, such models are mostly used in simulators for accurate results.

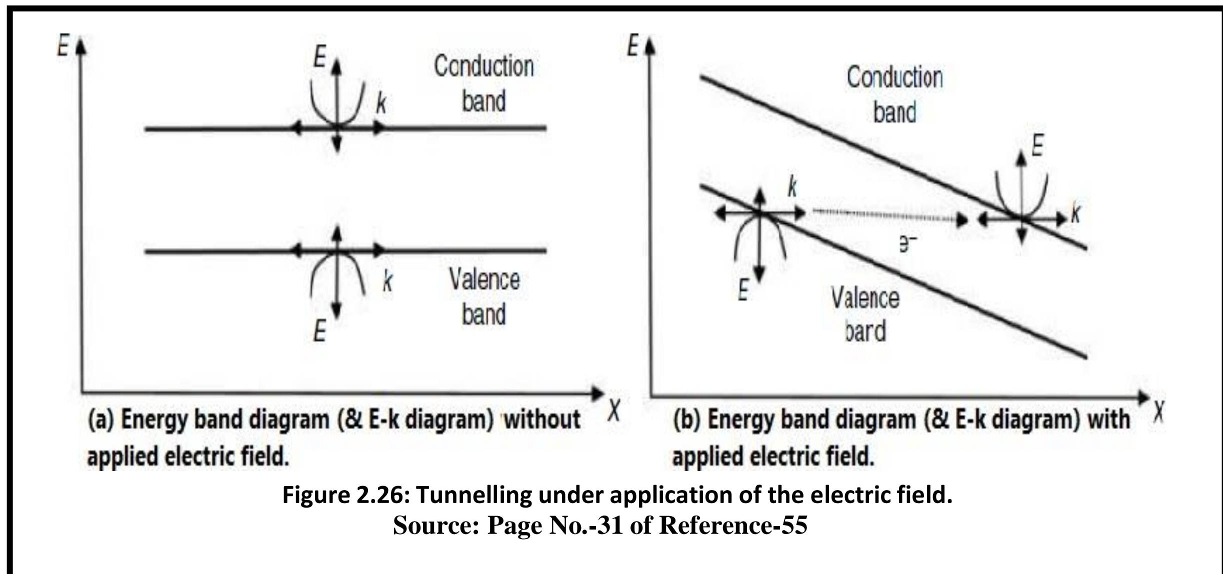
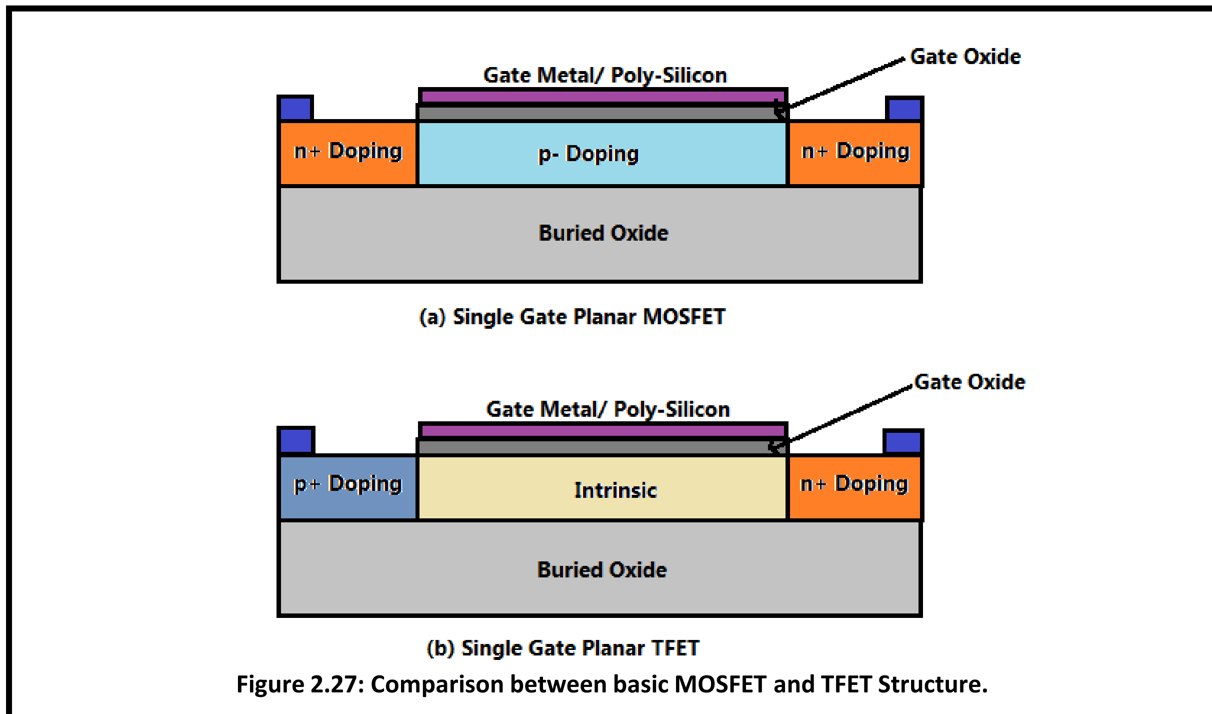


Figure 2.26: Tunnelling under application of the electric field.
Source: Page No.-31 of Reference-55

Local Tunnelling Models: The band structure in semiconductors is a product of the proximity periodic arrangement of the atoms in the crystal lattice. The energy bands can be viewed in the E-k diagram with the bands representing allowed energy states in which the electrons can reside. The bandgap separates the valence and conduction bands, acting as a potential barrier. It requires a large amount of energy for an electron to tunnel through this energy gap, in equilibrium conditions. If a strong enough electric field is applied, the band structure/ shape would be modified in such a way that the electrons can tunnel through much easier. The application of electric field aligns the filled valence bands with empty conduction band states in such a way that the potential barrier is thin enough for the electrons to tunnel through, as in figure 2.26. If the tunnelling probability is sufficiently large, we can get an appreciable amount of current flow. While deriving the expressions for the local tunnelling models, one of the most important approximations that we have to consider is that the electric field is constant near the region of tunnelling, which is not always true practically. Hence, the local tunnelling model can arrive at an analytical or closed-form expression, the current predicted by such model can vary in accuracy, depending on how cautiously the model is applied to the device under consideration [2.56]. In these models, the generation and recombination of carriers are not considered, hence the entire tunnelling current is assumed to be dependent on the rate of tunnelling or the tunnelling probability.

2.2.3. Basic Construction of TFET



(a) Single Gate Planar MOSFET

(b) Single Gate Planar TFET

Figure 2.27: Comparison between basic MOSFET and TFET Structure.

The most important reason for the popularity of TFET as a replacement for MOSFET is the similarity in construction. If the doping in the source region of a MOSFET is reversed, we obtain a basic TFET. Also, the channel region in TFET is made intrinsic or very lightly doped in nature, unlike MOSFET, where the channel is mostly lightly doped. The basic single MOSFET and TFET structures are shown in figure 2.27. For an n-channel TFET, the source is p-type doped and the drain is n-type doped. The doping is just reversed for p-channel TFET. A similar construction is followed for the Double gate structure[57-58]. Almost all of the MOSFET structures [59-60] can be converted to TFET, just by alternating the source doping.

2.2.4 Working Principle of TFET in Brief

The Tunnel Field Effect Transistor (TFET) belongs to a section known as steep sub-threshold devices. The basic working principle of TFET is based on quantum mechanical tunnelling. The carriers tunnel through the band-gap, which acts as a potential barrier in the source channel junction. Due to the fundamental difference in carrier generation/ transport phenomenon from the MOSFET [2.61], the TFETs can achieve SS lower than 60mV/decade. The TFETs can be visualized as gated PIN diodes. The potential at the gate is used to control the tunnelling barrier height, thus effectively controlling the device current. The device has an extremely low OFF-state current, as the leakage current is mostly due to a reverse-biased diode. The ON current of the device is comparatively lower than MOSFET, but the situation can be

improved by using high-k dielectrics and a method called line-tunnelling. In the TFET structure presented in figure 2.26 and also in similar double gate structures, the band-to-band generation is confined to a small circular region or a point at the source-channel interface, near the gate oxide-semiconductor interface only. Thus, the volume over which the carrier generation takes place is small, leading to small ON currents. Such type of tunnelling is aptly called Point tunnelling.

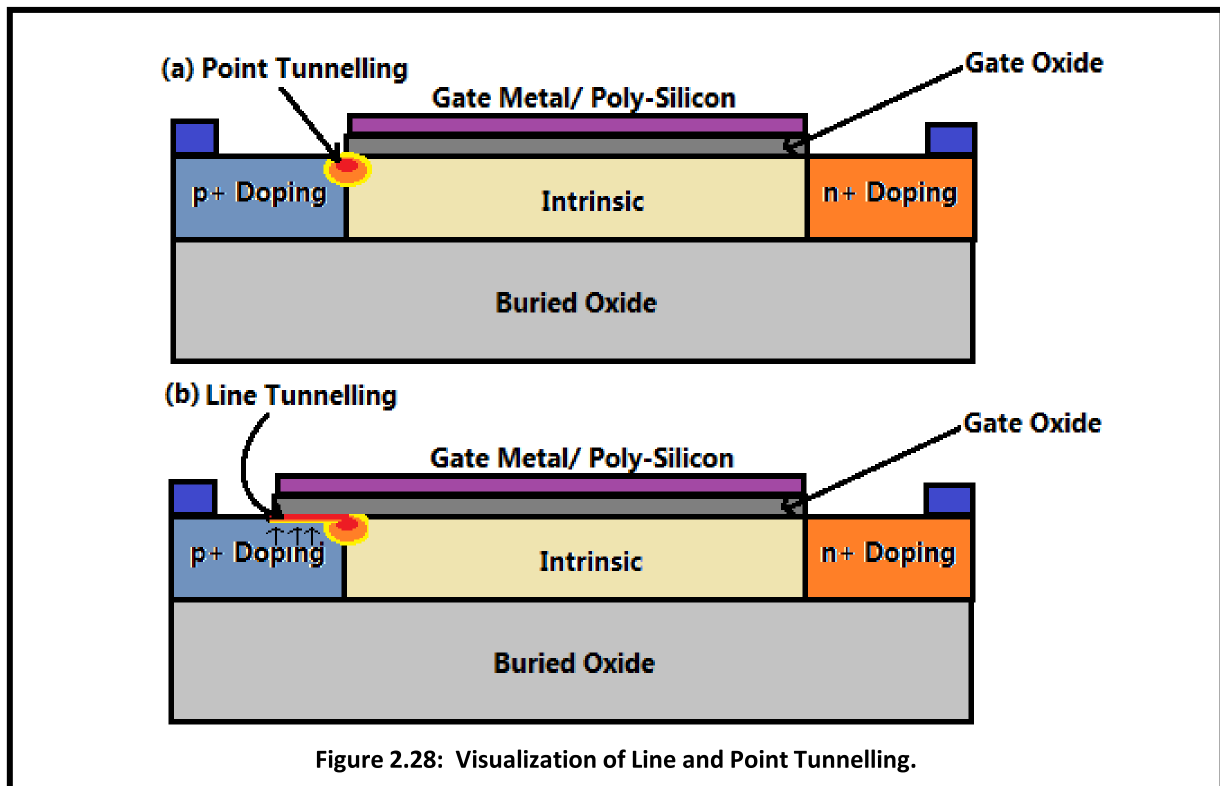


Figure 2.28: Visualization of Line and Point Tunnelling.

Line Tunnelling: In order to increase the ON current in TFET, often the method of line tunnelling is applied. Here a gate overlap is created over the source region [2.62]. The electric field thus formed has to be in a direction that aids tunnelling. The electrons from the inner parts of the source tunnel to the inversion region formed near the surface of the source (for n-TFET). The carrier generation takes place in a line, near the source-gate oxide interface, hence the name. Since the carrier generation, area/ dimension is larger than point tunnelling, the ON current increases. The phenomenon of point and line tunnelling is illustrated in figure 2.28(b).

Point Tunnelling: This is the most common type of carrier generation method. The maximum carrier generation rate is almost confined to a point [2.63]. The barrier in the OFF state is too large for the electrons to overcome or tunnel. But as the gate potential is increased (assuming n-TFET), the CB in the channel region aligns with the VB of the source region. The

valence of the p-type source is full of electrons but the intrinsic channels conduction band has no free states for the electrons to the tunnel. With sufficient drain voltage, the conduction band at the channel starts to get free states and hence the electrons now can tunnel and contribute as device current as shown in figure 2.28(a). Thus, unlike MOSFETs, there is no ON state without current flow. Also, the TFET has two threshold voltages, one for the gate bias and another for drain bias. Figure 2.29 shows the energy band structure for n-TFET in the ON and OFF state.

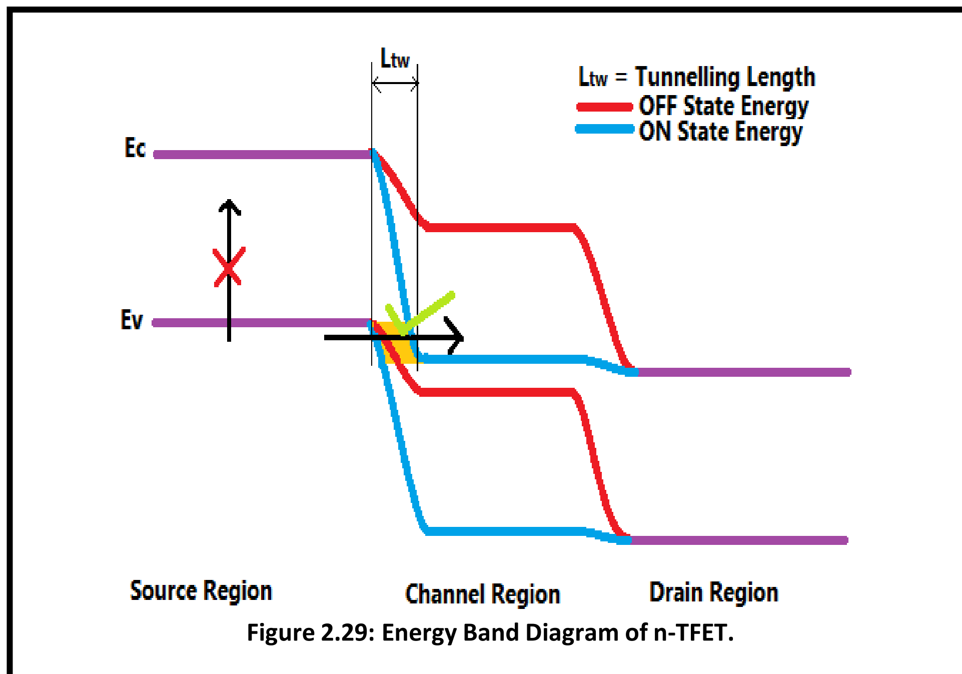


Figure 2.29: Energy Band Diagram of n-TFET.

2.2.5 Transfer characteristics of traditional TFET structures

2.2.5.1 Without any external bias

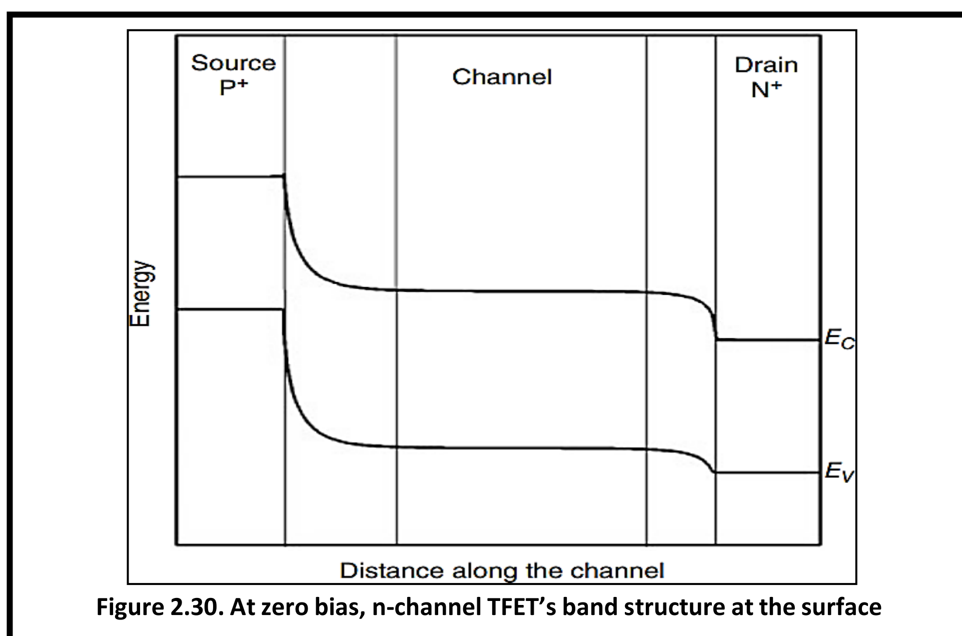


Figure 2.30. At zero bias, n-channel TFET's band structure at the surface

Figure 2.30 shows the thermal equilibrium band diagram of a TFET when no external bias ($V_{GS} = V_{DS} = 0$) is applied. The depletion regions are formed at the source–channel and channel–drain junction, respectively.

2.2.5.2 OFF State

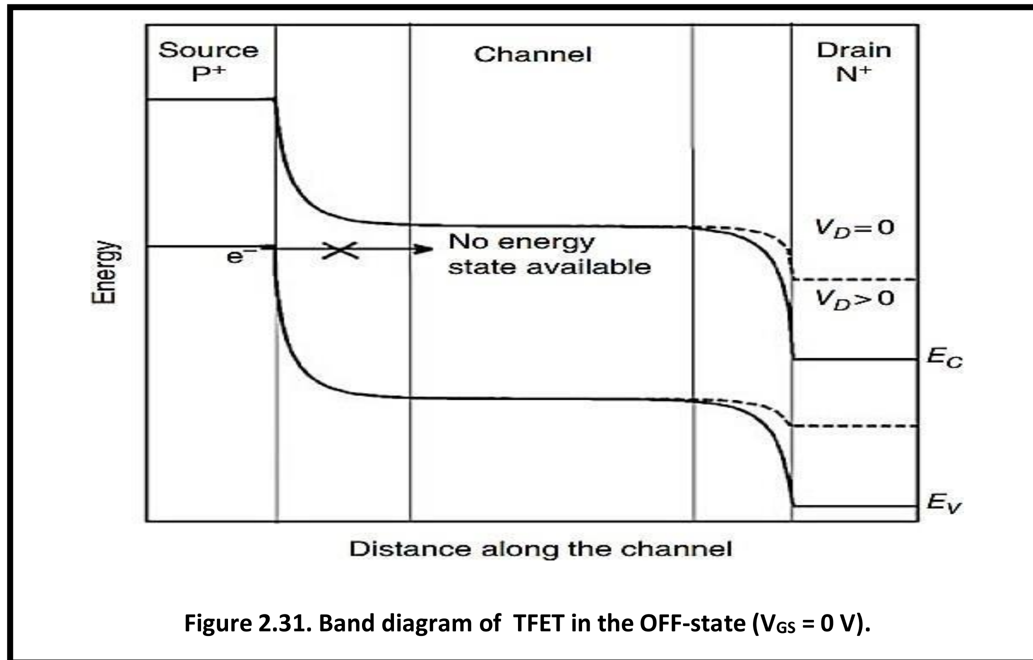


Figure 2.31. Band diagram of TFET in the OFF-state (V_{GS} = 0 V).

The TFET is in the OFF-state, which is equivalent to the OFF-state of a MOSFET when $V_{DS} > 0$ and $V_{GS} = 0$. The band diagram for this situation is shown in Figure 2.31. Any charge carriers present in the CB of the channel will begin to migrate to the drain in the OFF-state of the TFET, generating a current. However, since the source is p-type, there are very few free electrons in its CB, which means that only a small number of electrons can be pushed into the channel. The source of a MOSFET is n-type and the CB contains free electrons. A few of these electrons would be pumped into the channel through thermionic emission, crossing the potential wall at the source-channel junction. Hence, the I_{OFF} in a MOSFET is higher than in a TFET.

2.2.5.2 In ON State

Charge carriers must be pumped into the CB of the channel for current to flow in the device. Since there are few free electrons in the p-type source's CB, these charge carriers emerge in the VB of the source in TFETs. The EBs in the channel change with respect to the source as the V_{GS} is increased, as seen in figure 2.32. The VB in the source aligns with the CB in the channel at a certain V_{GS}, as seen in figure 2.32. (a). In the OFF-state of the

system, the electrons in the VB of the source had no available energy state in the channel through which they might tunnel. Since the source's VB and the channel's CB are now aligned, electrons will tunnel from the former to the latter through the EG (dashed line in figure 2.32(a)). The beginning of the ON-state of the TFET is the V_{GS} at which the source's VB and the channel's CB are aligned. If the V_{GS} is raised figure 2.8(a)), the energy of the bands in the channel area decreases, allowing electrons from the VB edge of the source $E_{V,Source}$ to the CB edge of the channel $E_{C,Channel}$ to tunnel to the channel's CB. As a result, the current rises dramatically.

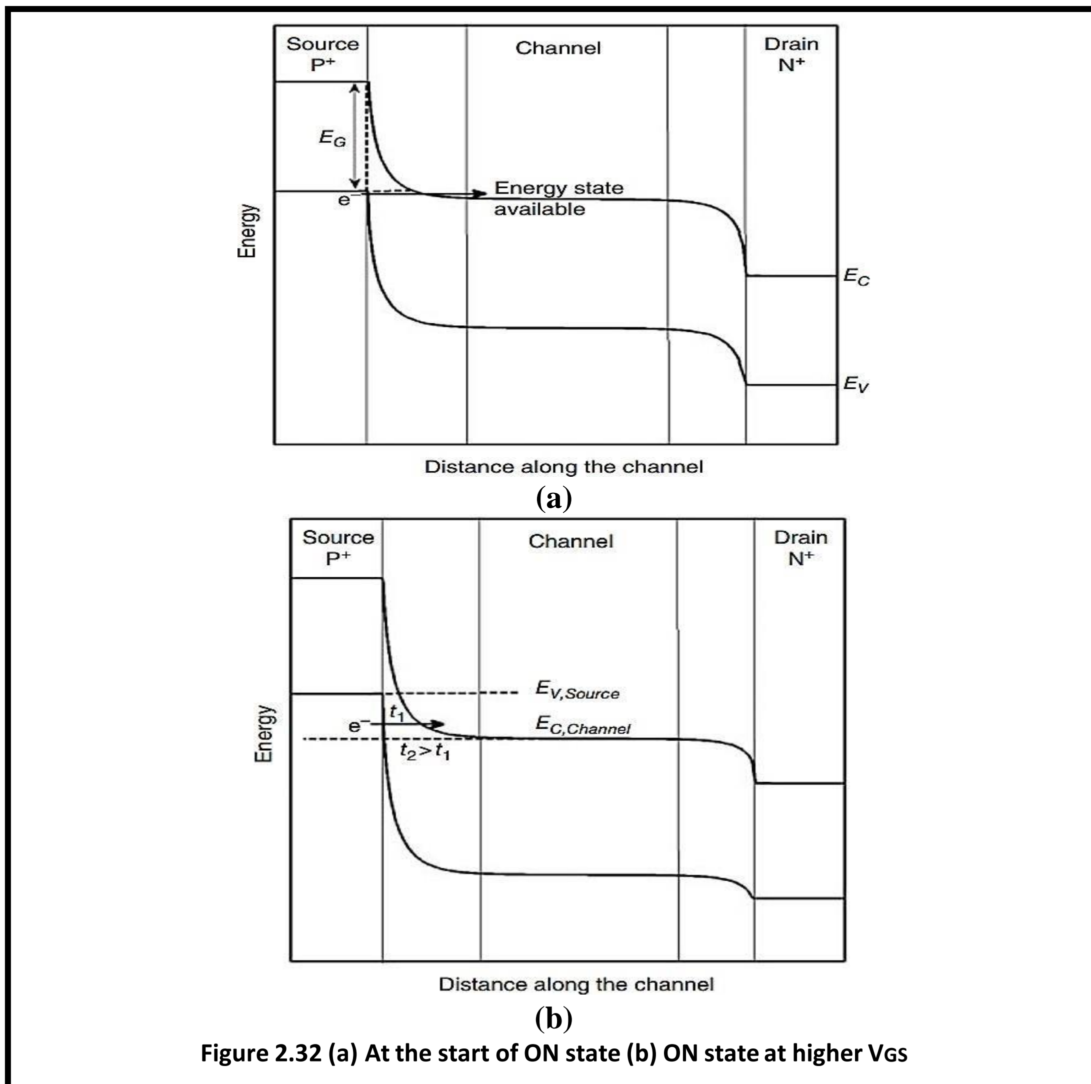


Figure 2.32 (a) At the start of ON state (b) ON state at higher V_{GS}

Furthermore, increasing the gate bias reduces the length of the tunnelling barrier or length, which raises the current even more. Let's look at the possible obstacle that an electron on the source's VB edge would overcome to meet the channel's CB withboth a low (Figure 2.32(a)) and a strong (Figure 2.32(b)) V_{GS}. As can be shown, the barrier height is the same in both situations – it is the E_G. However, in the case of a stronger V_{GS}, the

tunnelling length is reduced due to a larger EF. As a result, when the V_{GS} is increased, the chance of tunnelling increases, resulting in a higher current.

Let us equate the tunnelling possibility of an electron at the VB edge of the source withthat of an electron occupying the lowest energy from which tunnelling will occur inthe case of a high V_{GS} (Figure 2.32(b)). The likelihood of tunnelling is determined bythe height and length of the potential wall. The material bandgap determines the height of the potential barrier at all energy levels. The potential wall thickness is determined by the slope of the EBs (i.e., the EF), the steeper slope makes the tunnellinglength shorter. The slope of the EBs is greatest at the junction of p and n-type regions, according to our understanding of the p–n junction diode. Since the sourceis highly doped in comparison to the channel, this junction is almost at the edge of the source in TFETs. As a result, the electron at the source side, which is in the energy level $E_{V,Source}$, tunnels through a potential wall with a shorter tunnelling width(L_{T1}) than the electron at the energy $E_{C,Channel}$ (L_{T2}). As a result, the electron at energy $E_{C,Channel}$ has a lower tunnelling likelihood than the electron at the VB edge $E_{V,Source}$.Thus, for lower energy levels in the source VB, the overall current reduces, and forvery low energy states in the source VB, it is zero. As a result, at a sufficiently highV_{GS}, the increase in I_D with rising V_{GS} is almost entirely due to a reduction in tunnelling length.

2.2.5.4 Pinning of Channel Potential

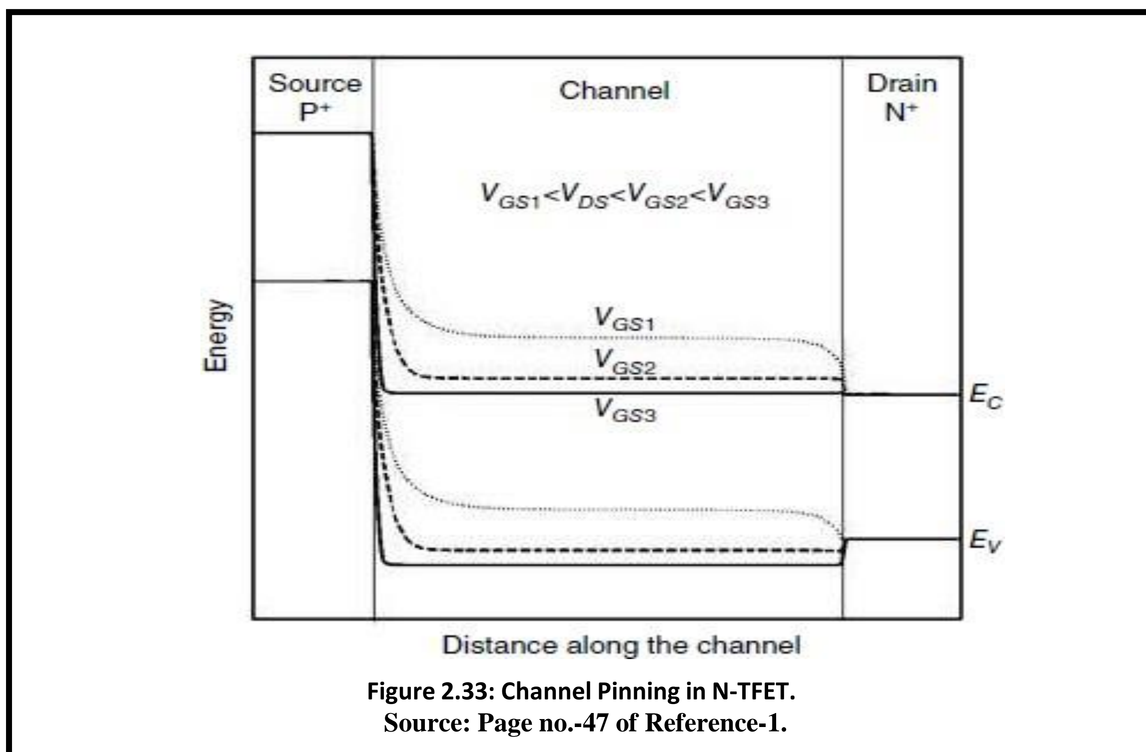


Figure 2.33: Channel Pinning in N-TFET.
Source: Page no.-47 of Reference-1.

As discussed earlier, the gate bias causes the energy band in the channel to modulate, thus enabling or disabling the tunnelling of carriers. However, for very high gate voltages ($V_{GS} > V_{DS}$), the inversion charges generated at the semiconductor-gate oxide interface becomes comparable to the electron density in the n-type drain region (assuming n-TFET). In such case the channel can be considered to be effectively shorted or pinned to the drain, this phenomenon is known as channel pinning. The pinning of the channel potential does not occur precisely at $V_{GS} = V_{DS}$, but near to that value, as the inversion charge varies constantly. Due to pinning, the drain current becomes less responsive to the change in applied gate voltage. After a certain value of gate voltage, the increase in drain current, corresponding to the change in gate voltage reduces. The reduction in drain current is due to the fact that the conduction band does not dip further to place more unoccupied states for electrons to tunnel from the valence band in source region. The pinning of channel potential is demonstrated in figure.2.33.

2.2.5.5 Ambipolarity in TFETs

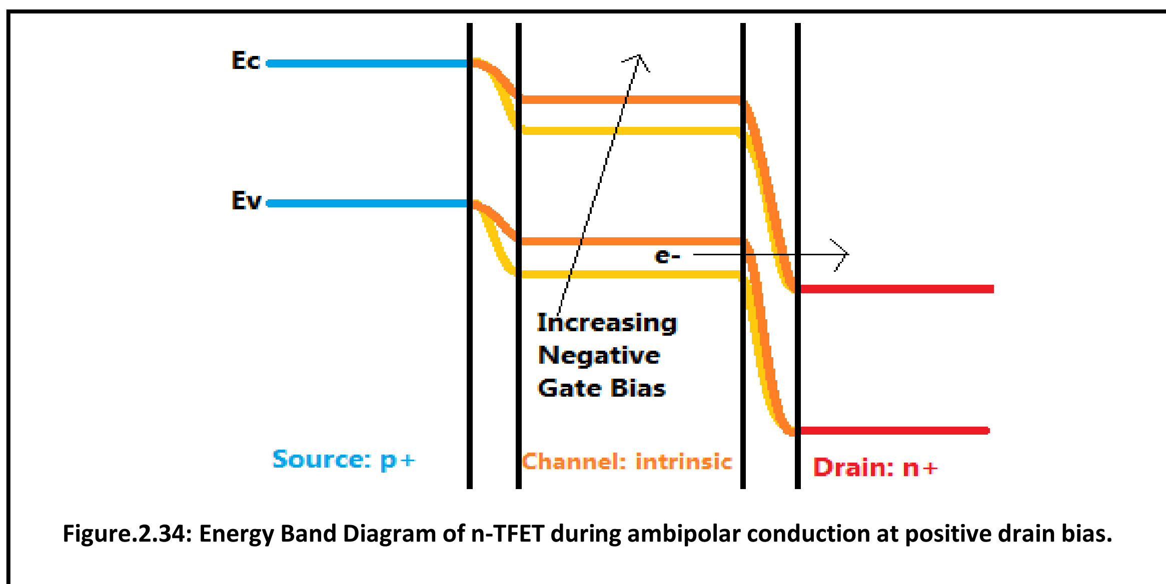


Figure.2.34: Energy Band Diagram of n-TFET during ambipolar conduction at positive drain bias.

The characteristic curve of a basic TFET reveals that they conduct negative values of gate voltage in the case of n-TFET and vice-versa for p-TFET. The energy band diagram in the case of ambipolar conduction is illustrated in figure2.34 With a certain amount of negative gate bias the valence band in the channel region starts to align with the conduction band in the drain region. The positive drain bias causes the electrons to tunnel across the channel-drain junction, which results in drain current conduction. This behaviour is known as ambipolarity in TFET. The problem with ambipolarity is that it degrades performance when TFETs are used in digital circuit applications. The reverse conducting behaviour of TFETs makes to them harder to use

in applications running on bi-polar or even unipolar power supplies. Any amount of reverse voltage on the gate during the supposedly OFF state of the device will make it conduct and increase leakage and affect the voltage level of the logic circuit. Thus a plethora of solutions for reducing the ambipolar nature of the TFET has been proposed with varying degrees of success. A few of the solutions/ modifications done to the TFET structure for the reduction of reverse conduction are discussed in the upcoming section. Finally, figure.2.35 represents the transfer characteristic of n-TFET, showing all the above-mentioned conditions of operation.

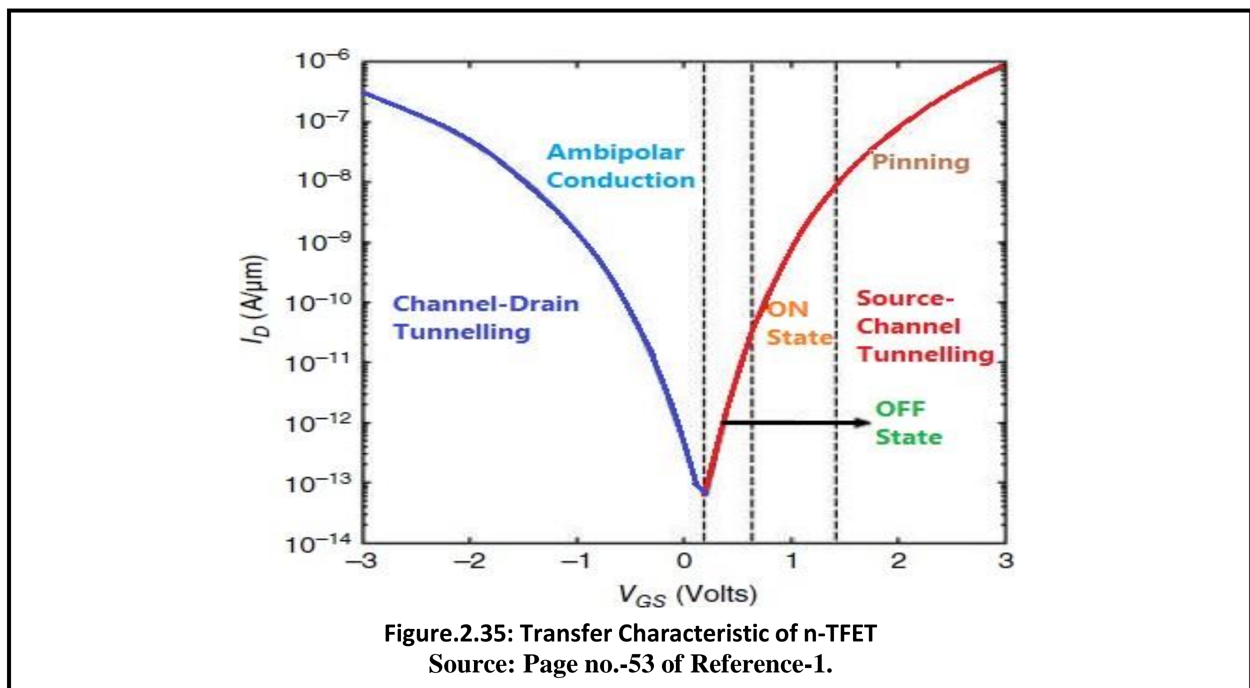


Figure.2.35: Transfer Characteristic of n-TFET
Source: Page no.-53 of Reference-1.

2.3 A Brief Literature Review on various TFET Designs for Performance Enhancement

2.3.1. Using multiple Gate Oxide Materials

The use of high-k dielectric is desirable in TFETs as their ON current is inherently smaller than MOSFETs. With high-k dielectrics, the gate to source electric field can be enhanced, leading higher band-to-band generation rate and hence, higher ON currents. Unfortunately, the same is also true for the channel-drain junction, thus the reverse conduction current also increases with the use of high-k dielectric. The solution to this problem is to use separate dielectrics near the source-channel and channel-drain junctions. The high-k gate oxide should be placed near the source and the low-k dielectric towards the drain, in order to maintain the high I_{ON} and reduce the reverse gate voltage current. The device structure is available in

[2.65]. The single gate structures are mostly outdated and currently, only Double Gate TFETs are of interest in research.

The lengths of the high-k and low-k dielectrics can be optimized to obtain the least ambipolar nature and highest I_{ON}. The optimization for high-k dielectric length for the dual material gate oxide structure has been performed in the work of R. Narang et al [2.65] where it is referred to as the hetero-gate (HG) TFET. The result thus obtained can also be found on page no.-5 of reference-2. The doping at source are p+ and drain are n+ respectively with a concentration of 10^{20} cm^{-3}. The high-k dielectric is HfO_2 with $k=21\varepsilon_0$ and the low-k is SiO_2 with $k=3.9\varepsilon_0$. The channel length is kept at 45nm, with silicon thickness of 10nm and oxide thickness of 3nm. It is observed that the I_{ON} degrades for both the extreme case of high-k dielectric length [2.65]. The ambipolarity and gate capacitance increases with the increasing length of the high-k dielectric. To achieve the best possible I_{ON}, least ambipolarity and minimum miller capacitance due to the gate oxide, an L_1 value of 10nm was chosen.

2.3.2. Using Multiple Materials as Gate Metal

To enhance the drain current and make it comparable to MOSFET and at the same time subdue the inherent ambipolar nature of the TFET, two different materials can be used over the channel with different work functions [66]. Basically, the variation in work function is made such that there is an increase in the electric field at the source-channel junction so as to effectively increase the tunnelling of carriers, and at the same time, just the opposite at the drain end is achieved. Thus, there is a boost in the I_{ON} and a reduction in ambipolar current. If looked closely, the principle is very similar to dual material gate oxide implementation. The construction of Dual Material Gate Metal TFET is shown on page no.-2 of reference-65. The length of the auxiliary gate and tunnelling gate can be optimized to obtain the highest possible ON currents and lowest possible ambipolar current. The gate length optimization curves are presented on page no.-3 of [66]. All the data presented here are borrowed from the work of S. Saurabh et al [66].

The basic idea for such a device (n-TFET) is to place the metal with lower work-function near the source-channel interface and metal with higher work-function at the channel-drain interface. The work function of the tunnelling gate can also be optimized, given the metal with the required work function is available and compatible with the fabrication procedure.

From the work-function variation curve on page no.-3 of [2.66]., it is clear that the ON current increases with lower work functions. Finally, we need to compare the Dual metal gate with our conventional single metal gate TFET. The comparison is again performed by S.

Saurabh et al [66] and is available on page no.-3 of [2.66]. The comparison between conventional and dual metal gate TFET clearly shows that the DMG DGTFET is better than SMG DGTFET with the lowest leakage currents and comparable ON currents.

The improvement over the Dual Metal Gate TFET was proposed by N. Bagga et al [2.67]. The renovated device is provided with triple metal at the gate, instead of two. The gate work-function engineering possibilities are greater with more metals, as the effectiveness of work-function control over the channel improves due to more spatial resolution. The paper under consideration [2.67], also includes analytical modelling of the device, but here we will only concentrate on the qualitative behaviour of the device. The transfer characteristics of the TM-DGTFET for varying silicon film thickness are shown on page no.-6 of [2.67].. The oxide thickness for the device is 2nm, with a channel length of 60nm with L_1, L_2, and L_3 values of 10nm, 20nm and 30nm respectively. The doping concentrations are $2x10^{20}$ cm^{-3} p-type at the source and n-type at the drain.

2.3.3 PNPN or NPNP TFET Structure

One way of increasing the drain current is to introduce a small but highly doped region near the source of the opposite doping type to that of the source. The pocket doping causes an augmented dip in the CB near the VB in the source (considering the PNPN device) even at V_{GS}=0V. This increases the tunnelling probability as the number of aligned states for electrons to tunnel increases. Due to such doping, the lateral electric field also increases, meaning more current due to higher band-to-band generation. According to [2.68], the optimum pocket doping length is around 4nm. If the pocket doping created is too long, the region might not be fully depleted causing the device to lose Gate control, thus curtailing the sub-threshold swing. Also, fabricating devices with very narrow pocket doping is difficult. Even if by implantation thin doping is introduced, the dopants diffuse during other high-temperature fabrication steps and thus increasing the overall pocket doping length. For a basic PNPN structure, the Source is p+-doped, a pocket doping of n+ type is introduced, followed by a very light p-type doped channel, ending with an n+ doped Drain region.

2.3.4 Raised Germanium Source Structure

The band-to-band generation rate increases with use of lower band gap materials, as Germanium (Ge) [7]. Thus, using a lower band gap semiconductor at the source increases the I_{ON}. As an improvement to this concept S.H. Kim, et al [69] proposed the raised germanium source TFET. The proposed structure increases the overlap of the gate with the source, thus

increasing the chance of line tunnelling. The proposed structure is illustrated in page no.-2 of [2.69]. P-type has a concentration of $1x10^{19}$ cm^{-3} doping for the Ge-source region, n-type doped has a concentration of $1x10^{19}$ cm^{-3} for the drain. The silicon thickness is 100nm, with an effective SiO_2 thickness of 1nm. The channel region is moderately doped at $1x10^{18}$ cm^{-3} p-type. The gate length is kept at 30nm and the buried oxide thickness at 200nm. The Germanium layer thickness of 25nm for partially elevated and 65nm thick for fully elevated structure is grown in-situ over the initially present silicon source. The simulation is performed with calibrated TCAD model. The calibration curve and the transfer characteristics are shown on page no.-2 of reference-68. The calibrated local band-to-band tunnelling model's coefficients are: A = 1.46×10^{17} $cm^{-3}s^{-1}$ and B = 3.59×10^{6} Vcm^{-1}. The raised source structures provide a good amount of ON current. The current can further be increased by using pocket doping, as mentioned in the previous section.

2.3.5 Si-Ge Source UTFET

The device structure was proposed by W. Wang et al [2.70]. The device has a U-shaped channel, due to which an effectively longer channel can be contained in a smaller dimension. Because of the longer channel, the leakage current is reduced. On a basic UTFET structure with a p+ doped source followed by a p+ doped Si-Ge layer, an n+ doped delta layer with a doping concentration of $5x10^{19}$ cm^{-3} is introduced. This delta layer reduces the band-to-band tunnelling length, hence effectively increasing the ON current. The basic UTFET structure and the delta-doped structures are presented on page no.-1 of [2.70]. The depth of the TFET gate is 120nm, the length of the gate is 16nm and the oxide thickness is 1.2nm. The U-Gate TFET achieve high I_{ON}/ I_{OFF} with a value of 10^8, as observed from the figure on the page.-2of [2.70]. The mentioned ON/ OFF ratio can be achieved at relatively low voltages, V_{GS}=0.7V and V_{DS}=0.7V. The results are better than similar planar-TFET with 16nm channel length.

2.3.6 L-Shaped TFET (LTFET)

The device fabricated by S.W. Kim et al in the year 2012 [2.71], called L-Shaped TFET because the channel region of the TFET resembles the letter 'L'. The LTFET is fabricated using Mesa etching technology, especially in the elevated source region. The gate oxide is SiO_2 with a thickness of 2nm. High-k dielectric (like HfO_2) is added by Atomic Layer Deposition (ALD) technique for enhanced I_{ON}. The elevated source region makes line tunnelling possible, as the gate region is directly over/ side by side with the source, increasing the region over which the tunnelling is possible. The source, drain and channel regions are doped p+, n+ and p- with

concentrations $1x10^{20}$, $1x10^{18}$ and $1x10^{15}$ cm^{-3} respectively. The device structure is provided on page no.-2 of [2.71]. The transfer characteristic of the LTFET along with its comparison with a planar TFET is shown in the figure on page no.-3 of [70]. Clearly, the LTFET has more I_{ON} and better SS than the planar TFET, as evident from the figure. The main drawback of LTFET is that it suffers from a significant ambipolarity problem. The solution to this problem was provided by C. Li, et al [2.72] in 2018. By introducing a low doping region near the drain, the drain side tunnelling can be arrested, resulting in lower ambipolar conduction. The proposed HGD (Hetero-Gate-Dielectric) and LDD (Lightly Doped Drain) show negligible ambipolarity and good RF performance, according to simulation data. The LDD region reduces ambipolarity without affecting the Drain region doping, which maintains low contact resistance, unlike other device structures where the drain doping is reduced to curb the ambipolarity which results in increased contact resistance.

The paper compares the performance of four different LTFET structures, with combinations of with and without HGD and LDD. It was observed that HGD-LDD-LTFET shows the lowest ambipolar conduction, with a very slight reduction in current. Hence, the HGD-LDD structure is desirable. The transfer characteristics and the device structures of the new proposed structure of LTFET are presented on page no.- 2 of [2.72].

2.3.7 L-Shaped Gate TFET (LG-TFET)

The device structure was proposed by Z. Yang in the year 2016 [2.73]. The device has a gate structure similar to the UTFET, but with an extended region over the source. This extended region helps in increasing the drain current by ~50% over the basic L-Channel TFET. Also, pocket doping is added for the same purpose of increasing the I_{DS}. The device structure is depicted on page no.-1of [2.73]. The transfer characteristic of the LG-TFET is compared with the L-TFET and UTFET structures on page no.-2 of [2.73]. Clearly, the LG-TFET has more I_{ON} and SS than the others. The advantage of this structure is that it combines the merits of both LTFET and UTFET structures. The doping concentrations are: Ns $=1x10^{20}$ cm^{-3}, $N_D=1x10^{20}$ cm^{-3}, $N_C=1x10^{17}$ cm^{-3} and n+ pocket doping $N_P = 1x10^{19}$ cm^{-3} with 5nm thickness. The oxide thickness is kept at 2nm. The height of the Source region (H_s) is 30nm and that of the Drain region (H_d) is 10nm. The depth of the Gate region (H_g) is 40nm with a width (W_g) of 6nm.

2.3.8 Doping-less TFET

The Doping-less TFET [2.74] is built on the concept of charged plasma. With the use of metals with appropriate work functions at the source and drain, the intrinsic semiconductor at

the source and drain region can be made to work as n-type or p-type as per requirement. The absence of doping makes the device exclusive of any high-temperature fabrication steps. Hence, it is suitable for making monocrystalline silicon-based devices on a variety of substrates, especially glass. It should be noted that unlike Schottky diodes, where a junction is formed between metal and semiconductor, in doping-less TFET, the main working junction, i.e. the source-channel junction is still a homo-junction. The device structure is as presented on page no.-1 of [2.74]. The whole device is constructed using intrinsic silicon with an n/p-type doping concentration of $1 x 10^{15}$ cm^{-3}. The carrier concentration at the source and the drain are induced by the respective metal contacts, especially under the overlap regions. The overlap regions are comprised of the Metal-Oxide-Silicon layer. To maintain uniform carrier concentrations over the entirety of the source and drain region, the silicon film thickness is kept lower than the debye length. The debye length is given as $L_D=((V_T\varepsilon_{Si})/(qN))^{0.5}$. The silicon body's doping concentration can be up to$1 x 10^{17}$ cm^{-3} without any significant variation in the result. This is particularly helpful as the device body can be accidentally doped during the fabrication process. The source and drain doping for this TFET is created by the charge plasma concept as in [2.75]. For creating a p+ equivalent source, platinum with work-function 5.93eV is used at the source region. Similarly, Hafnium with work-function 3.9eV was employed at the drain region. The gate metal can be either aluminium or poly-silicon as per requirement. A thin SiO_2 film of 0.5nm was placed between source metal and silicon film at the top, to avoid silicide formation. The oxide thickness at the drain end was kept at 3nm, as little less carrier concentration is desirable at the drain for prevention of ambipolarity, as discussed in earlier sections. The channel is kept at 50nm for the device. The simulated results for the doping-less TFET are obtained using ATLAS Silvaco's non-local tunnelling model. The transfer characteristic of the device and conventional double gate TFET of similar dimensions are compared in the plot on page no.-4 of [2.74]. The comparative plots from [74] reveal that the performance of doping-less TFET is similar to that of the conventional TFET.

2.3.9 III-V Semiconductor Homo and Hetero-Junction TFETs

The work of D.K. Mohata et al [2.76], demonstrates the homo-junction and hetero-junction III-V TFETs. The band engineered III-V TFETs show incredibly large ON currents at moderately low voltages, resembling the ON state of MOSFETs but with a faster turn OFF. The study is based on four different TFET structures. The devices were epitaxially grown using solid source MBE. The $In_{0.53}Ga_{0.47}As$ homo-junction or "Large Eg HomJ" TFET and the $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ lattice-matched hetero-junction or "Moderate HetJ" TFET were

grown layer by layer on lattice-matched InP substrate. On the other hand, the $In_{0.7}Ga_{0.3}As$ homo-junction or "Small Eg HomJ" TFET and the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ lattice-matched hetero-junction or "High HetJ" TFET was also grown by layers, metamorphically on lattice-mismatched Indium-Phosphide substrate, using linearly graded $Al_xIn_{1-x}As$ as a buffer. The device structures under consideration can be illustrated as block diagrams in page no.-2 of [2.76].

The energy band alignment diagrams for the TFET structures under consideration are shown on page no.-2 of [2.76]. With increase in the Indium mole-fraction in $In_xGa_{1-x}As$ (i.e., from x=0.53 to x=0.7), the energy band-gap E_G or the effective tunnelling barrier $E_{B,eff}$ reduces from 0.74eV to 0.58eV. A type-II staggered hetero-structure is formed from the lattice-matched $GaAs_{1-y}Sb_y/In_xGa_{1-x}As$ hetero-interface. Again, with increase in 'In' mole-fractions from x=0.53 to x=0.7 and 'Sb' mole-fractions from y=0.5 to y=0.65 i.e., Moderate HetJ to High HetJ, the effective tunnel barrier $E_{B,eff}$ reduces from 0.5eV to 0.25eV because of the increase in stagger.

The transfer characteristics of the III-V TFET structures, as discussed till now are shown in page no.-3 of [2.76]. All the data presented in these curves are experimental in nature. The "High HetJ" TFET has the highest ON current. The homo-junction TFETs show better I_{ON} to I_{OFF} ratios but lower ON currents than the hetero-junction ones.

2.3.10 Ferroelectric TFETs

The use of ferroelectric material as a dielectric in MOSFET was demonstrated by Salahuddin and Datta [2.77]. The ferroelectric materials are supposed to display negative capacitance behaviour, which can be used to multiply the voltage supplied at the gate of the device. The effect of such voltage multiplication at the gate of any field-controlled device results in very small sub-threshold swings. No direct experimental proof has been found for the existence of negative capacitance. In spite of the lack of evidence for negative capacitance, the use of ferroelectric material, in general, has the advantage of acting like an active capacitor, i.e. with the applied electric field the material permittivity changes. The ferroelectric material is in general stacked with the conventional gate oxide of the device.

The ferroelectric TFET device was proposed by A.M. Ionescu et al [2.78]. The device under consideration is a single gate TFET, but with tri-layer gate oxide. The first layer, above the silicon, is SiO_2, followed by a high-k dielectric (Al_2O_3) and finally the ferroelectric material. The ferroelectric material used is a Fe-copolymer, poly-vinylidene fluoride tri-fluoroethylene [P(VDF-TrFe)]. An effective gate oxide thickness of 14nm was achieved, which implies that

the gate leakage will be negligible. The thermally formed SiO_2 thickness is 2nm, followed by 5nm thick Al_2O_3 formed by ALD (atomic layer deposition) and finally 30nm thick P(VDF-TrFe). The buried oxide thickness is 150nm, formed on a p-type uni-bond silicon substrate of 65nm thickness. The device is simulated using Sentaurus TCAD using Schenk band-to-band tunnelling model. The qualitative transfer characteristic and device structure are shown as a figure on page no.-2 of [2.78].

The experimental and simulated data for channel length and width of 5um and 20um respectively are plotted on page no.-4 of [2.78]. The characteristic curve of Ferroelectric TFET shows a hysteresis of about 1V. This property can be levied for implementing single transistor RAM cells.

2.3.11 Phase Change TFET (PC-TFET)

In recent years the phase change materials have shown promise as good beyond CMOS. The phase change materials are interesting as they exhibit phase transitions with respect to external physical stimulus [2.79-2.80]. The phase transition can cause a large change in electrical conduction properties. Currently, Vanadium Dioxide has gained much attention as a phase change material. It shows metal-to-insulator phase transition (MIT) with temperature. The critical temperature at which the transition happens is 340K for bulk vanadium dioxide. Below the critical temperature, the VaO_2 is in a monoclinic phase, but above the critical temperature, it transitions to a tetragonal rutile structure. The tetragonal phase has an energy bandgap of ~0.6eV at the 3d conduction band, thus it is conducting in nature, unlike the monoclinic phase which behaves as an insulator. The change in conductivity is in order of five decades, which is considerable and can resemble a switch. The only drawback of the VaO_2 based MIT switch is that the $I_{Leakage}$ is not negligible, due to small bandgap in the monoclinic state.

Initially, MOSFETs based on VaO_2, as semiconductors, were designed but the conduction modulation due to the gate voltage was not significant [2.81-2.83]. To solve this problem, electrolyte-based gate MOSFETs were introduced, so that the ionic gate electrolyte and vanadium dioxide interface would increase the effective electric field. This solution to weak conduction modulation served its purpose, but it was found that the electrolytic gate devices were slower than conventional devices [2.84-2.86]. Thus, a new design of transistors, incorporating phase change materials as desired. Here we will be discussing the new PC-TFET device proposed by W.A. Vitale et al [87] in Scientific Reports published by Nature. The qualitative transfer characteristic of the PC-TFET device and other contemporary devices is

illustrated on page no.-2 of the paper [87]. The PC-TFET shows hysteresis behaviour similar to the ferroelectric TFET.

The MIT material when used in the Gate region of the TFET helps combat the leakage as the gate itself is insulated by the presence of the gate oxide. Alternatively, the MIT material can be used in series with the channel, after the Source, where the ON current flow is comparable to the two terminals MIT switch's ON current and will not be hindered. At the same time, the leakage current will be controlled by both the channel and MIT switch's OFF state itself. In the implementation of PC-TFET using an MIT switch at the gate and source, the state transition of the MIT switch is controlled by the V_{GS}. The state transition induces an internal differential amplification ($dV_{GS,int}/dV_{GS} >> 1$) of the voltage drop between the gate and the source ($V_{GS,int}$), which results in very steep rise in the drain current. The experimental transfer characteristics of the PC-TFET for MIT switch at the Gate and MIT switch at the Source are presented on page no-5 and page no.-6 of [2.87] respectively.

The TFET used for implementation with the MIT switch is a Strained Silicon-Gate All Around (GAA) Nanowire (NW) TFET. The cross-section of the Nanowire used in the TFET is $40x5nm^2$. The gate length of the TFET is 350nm. The concept of GAA-TFET is discussed in the upcoming section.

2.3.12 Tri-Gate or Fin-TFET

The Fin-FET or Tri-Gate structure is now commercially in use for MOSFETs [2.88], first introduced by INTEL in its 22nm technology node. Hence, like all the other MOSFET structures/ architecture, this structure has also been translated to TFETs [2.89]. The increased number of gates or the increase in the effective area of the channel under the gate region leads to desirable outcomes due to enhanced Gate control, such as Higher ON currents, steeper sub-threshold swings and lower short channel effects. Since the difference between TFET and MOSFET is mainly on Source doping, it is very likely that the Fin-TFET will come into production, like the Fin-FET.

2.3.13 Gate All Around TFET (GAA-TFET)

The increased gate control, observed in DG-TFET and TG-TFET is further enhanced in GAA-TFET [2.90]. A basic structure of Gate All Around Nanowire TFET is mostly implemented as a cylinder. The structure consists of a silicon nanowire with a diameter in the order of tens of nanometres, which is followed by an oxide layer of a few nanometres in order and finally, the whole structure is wrapped around by the gate metal. Such all-around wrapping

of the gate over the channel provides excellent electrostatic control. The short channel effects are at a minimum because all the electric fields emanating from the drain end at the gate without reaching the source region as there is no path available, unlike double and triple gate TFETs. The geometry increases the tunnelling area, and electric field at the source-channel junction, effectively increasing the ON current. Steeper sub-threshold swings and lower DIBT (drain induced barrier tunnelling) than the Fin-TFET are observed.

2.3.14 Carbon Nanotube and Graphene TFETs

Till now we have discussed mostly silicon TFETs, which due to the existing and matured fabrication technology are easier to manufacture. The main drawback of Silicon TFET is that the ON current is very low, which is in order of 10s to 100s of uA/um. Such ON currents are far cry from the ON currents provided by MOSFET, which makes the TFETs incompatible as CMOS replacement. Using Germanium at the source might alleviate the problem a little bit but the results are far away from ideal requirements. The III-V TFET structures show ON currents comparable to MOSFETs, but their practical realisation is limited by the fabrication technology. Also, the III-V TFETs fail to conserve the steep sub-threshold slopes over a larger span of gate voltages. Thus, recently designing TFETs with different materials has become popular. Two-dimensional materials like Graphene and Carbon Nano-tubes (CNTs) are very promising [2.91].

The advantage of such 2D materials is that they have a very less amount of dangling bonds, which results in exceptionally high gate controls leading to steeper sub-threshold swings. Also, the band-gap in the case of graphene is very low, which leads to higher ON currents. Similarly, in CNTs faster transport of carriers is possible due to high mobility in such materials. Recently Graphene nano-ribbon TFET and CNT-TFET have shown exceptional performances but their difficult fabrication is a trade-off.

In this section, we have discussed various TFET designs for performance enhancements. The list by no means is exhaustive, yet we have qualitatively covered a diverse range of TFET structures. Some other important TFET structures are the split-drain [2.92-2.93], T-shaped channel [2.94] and graded metal gate [2.95-2.97] structures. The split-drain and graded metal alloy gate structures reduce the ambipolar conduction in TFET by drain engineering and by controlling the gate control over the channel (i.e. achieving desired EB diagram in the channel of the device, from source to drain,) respectively. The T-shaped channel design helps increase the device current by the phenomenon of line tunnelling, at the same time the ambipolarity is also curtailed.

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Chapter:3

Chapter-3: Drain Doping Engineered Splitted Drain TFET Structures to Improved Performance in Subduing Ambipolar Effect- An Analytical Modelling and Simulation

3.1 Introduction 79
3.2 Literature Survey 80
3.3 Device structure and Parameters 82
3.4 Analytical Modelling 84
3.4.1 Electric field 84
3.4.2 Potential distribution 85
3.4.3 Drain Current 86
3.5 Simulation Setup 90
3.6 Results and discussions 90
3.6.1 Potential and electric field profile 90
3.6.2 Band Diagram Analysis 94
3.6.3 Optimization of Ambipolar Conductivity 95
3.6.4 Transfer Characteristics 96
3.6.5 Drain Output Characteristics 97
References 99

3.1 Introduction

Continuous miniaturization of the feature size of a conventional MOSFET leads to superior device performance regarding higher speed, lower operating power, and better high-frequency performance [3.1-3.2]. However, some serious issues are encountered in conventional MOSFET, as the scaling of the channel size gone below 50 nm, such as SCEs like DIBL, threshold voltage roll-off, subthreshold leakage current, and SS limitation to 60 mV/decade [3.3-3.5]. These challenges make conventional MOSFET unsuitable for the future design of analog/RF low-power applications [3.6], [3.7]. These issues can only be resolved by the innovation of some type of novel low-power transistor device structures whose fundamental switching mechanisms are different from the conventional MOSFET but the fabrication process is similar to a conventional MOSFET. One of the most promising candidates that could complement or even replace this revolutionary CMOS technology is one other than tunnelling FET (TFET) [3.8].

In a conventional MOSFET, the current transport of carriers depends on thermionic injection over an energy barrier, while, in TFETs, the conduction of carriers relies on band-to-band tunnelling (BTBT), which incorporates carriers transfer from one EB into another. The BTBT operation originated in TFET does not establish a minimum value of SS. Many TFETs with values of SS less than 60 mV/decade have been reported in the thesis [3.9-3.11].

One of the most important features of the TFET is its extremely low I_{OFF} , which is several orders of magnitude less than the I_{OFF} of a conventional MOSFET. Due to this low I_{OFF}, the TFET technology fits best into the Low Standby Power category as reported earlier in ITRS [3.12]. Moreover, TFETs have received significant attention for analog and RF applications due to their low I_{OFF} along with their low SS.

Apart from these, TFETs suffer from two major constraints. The first one is the low I_{ON}, which is lesser than MOSFETs. The other is ambipolar conduction, which originates from the BTBT at the channel–drain junction. These two main drawbacks have adverse effects on the performance of circuits. Various improvements have been investigated to compensate for these limitations faced by TFETs [3.13-3.14]. Still, there is ample space for achieving optimum efficiency in terms of upgraded short channel performances through the exploration of novel ideas as well as improving ON current without enhancing the OFF current as well improving SS.

3.2 Literature Survey

The predominant benefit of TFET is current conduction through modulation of quantum mechanical BTBT, which is a result of finite but non-zero probability of tunnelling through a potential barrier, a process in which electrons tunnel from the VB through the semiconductor bandgap to the CB or vice versa without any trap assistance. This attribute carries forward the advantages over the thermionic injection across an energy barrier for carrier transport in MOSFET. Thus, due to its built-in tunnel barrier, where the channel current in TFET is controlled by the tunnelling mechanism from the source, the TFET device is resistant to SCEs and the SS of a TFET is less than 60mV/decade at room temperature [3.15-3.17], allowing TFETs to have SS as low as 20 mv/decade[18], which is a root cause of designing of low voltage operating devices[3.19],[3.20].In addition, TFETs show a very small leakage current in the range of femto amperes (fA)[3.21] when the device is turned off, making TFET a promising candidate[3.20] for low-power applications[3.22–3.24] along with analogue and RF applications[3.25-3.26]. Other advantages of TFETs compared to other alternative device concepts are simpler fabrication steps and a compatible approach with standard CMOS

processing. TFET can be implemented as a reverse-biased gated *p-i-n* diode. Moreover, TFETs do not rely on high energetic processes like impact ionization, which are counterproductive to reliability issues and are conceded as scalable devices. Further advantages of TFET include no punch-through effect, the tunnelling effect enhances the device operating speed, and have a small V_{TH} as it depends on the band bending tunnel region.

The primary constraints concerning TFET devices are ambipolar conduction [27, 28], which originates from the BTBT at the drain–channel junction and the other is low ON current, which is considerably poorer than MOSFETs. Various improvements have been investigated to compensate for these limitations faced by TFETs [3.29-3.30]. Improved techniques to intensify the ON current without enhancing the OFF current as well improving include SS bandgap engineering [3.31], heterojunction TFETs [3.32] strained silicon [3.33], carbon nanotube TFETs [3.34], double-gate architecture, use of a high-k gate dielectric or a low-k spacer to reduce barrier at the source-channel interface boosting the tunnelling current and keeping the bandgap in other regions large to suppress the OFF current [3.35].

To compensate for the ambipolar conduction, the idea proposed is a gate-drain underlap structure [3.36]-[3.39], which lowers the ambipolar conduction considerably, but reduces the current driving capacity [3.40]. Furthermore, several works have already been reported considering bandgap engineering [3.41-3.43], gate work function engineering [3.44-3.45], dielectric engineering [3.46-3.47], channel engineering [3.48-3.50], graded channel engineering [3.51-3.52], and source/drain material engineering [3.53-3.54] with fitting analytical models (for dual gate, tri gate, gate all around structures [3.55-3.56]) to review TFET performance in terms of revamping drive current and decreased ambipolar conduction for the realization of TFET industry in nanometre domain.

However analytical modeling is pursued a better comprehensive study of device physics for its further improvement and facilitates circuit-level modeling [3.57]. The analytical model of a 2-D TFET device is derived for the potential distribution [3.58] under the subthreshold region. Based on this potential distribution, the drain current is derived. Compared to MOSFET, analytical modeling [3.59] of TFET is more complex and tedious, so the methodology used for obtaining the analytical modeling of the proposed structures is much less complex. Further, the TFET model structure is simulated to analyze the influence of drain doped engineering [3.60].

3.3 Device structure and Parameters

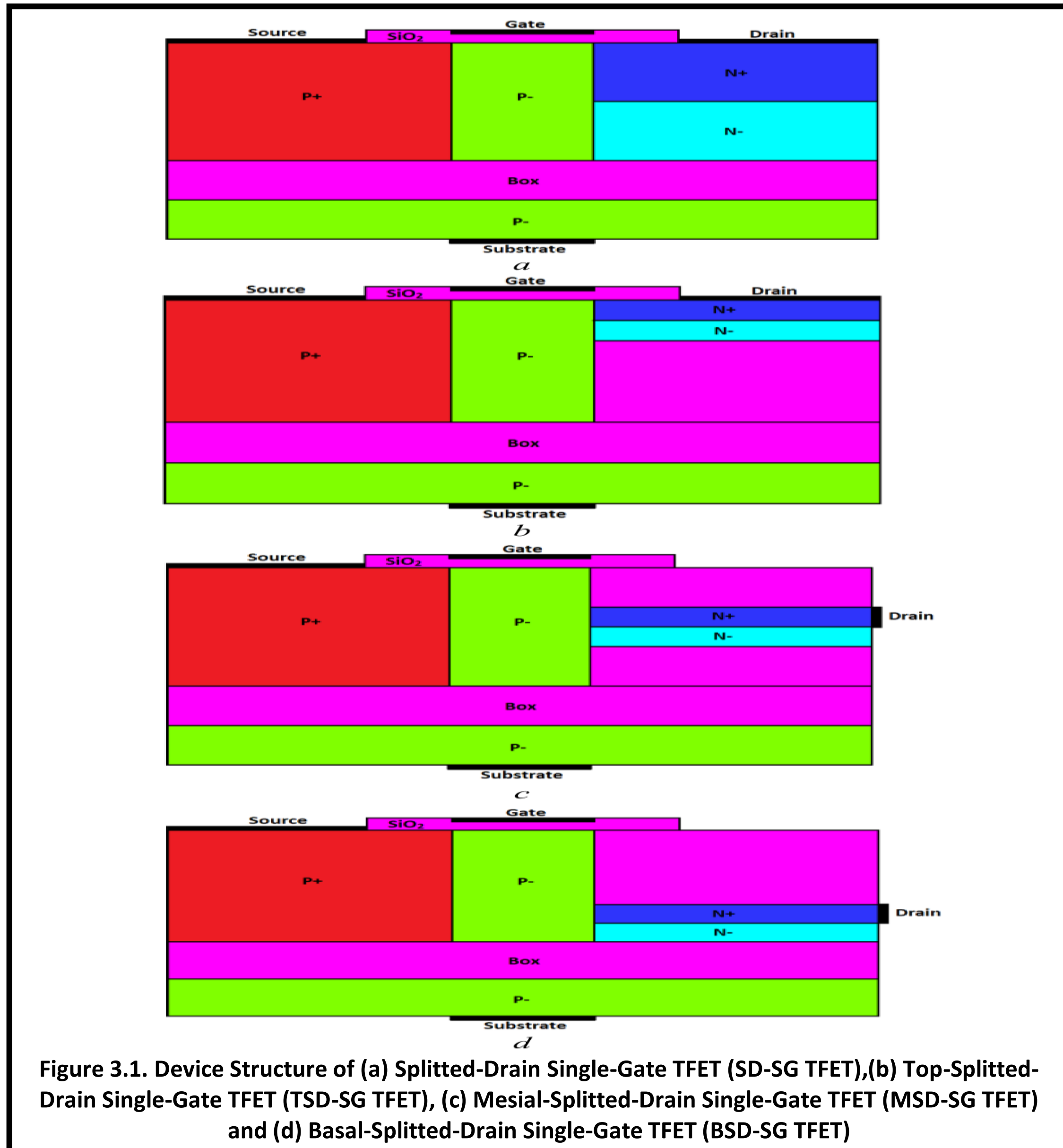

Figure 3.1. Device Structure of (a) Splitted-Drain Single-Gate TFET (SD-SG TFET),(b) Top-Splitted-Drain Single-Gate TFET (TSD-SG TFET), (c) Mesial-Splitted-Drain Single-Gate TFET (MSD-SG TFET) and (d) Basal-Splitted-Drain Single-Gate TFET (BSD-SG TFET)

The 2-D cross-sectional view of the p-channel TFET structures is given in the figure. 1, (a) Splitted-Drain Single-Gate TFET (SD-SG TFET), (b) Top-Splitted-Drain Single-Gate TFET (TSD-SG TFET), (c) Mesial-Splitted-Drain Single-Gate TFET (MSD-SG TFET) and (d) Basal-Splitted-Drain Single-Gate TFET (BSD-SG TFET). The structures contain two separate drain regions of different concentrations instead of a single-doped drain region. The highly-doped drain region is above the lightly doped region. The Doping specification of the TFET models is P^+ type source region ($1\times10^{20}cm^{-3}$) and a P channel region (1×10^{17} cm^{-3}), which are kept constant for all the simulations. Such doping concentration creates a tunnel junction between source and channel where the phenomenon of inter-band tunnelling occurs

for the TFET to conduct in N-mode. The doping specification of the upper N^+ doped drain region is 5×10^{18} cm^{-3}, drain electrode has ohmic contact with this higher doped drain region. The lower N doped drain region is 1×10^{17} cm^{-3}. Both disparate drain regions are variably doped to attain an optimal doping profile after analyzing the simulated graphs of all the characteristics. The device is simulated with lateral dimensions of 70nm, 50nm, and 70nm for source, gate, and drain respectively, and a total device length of 250nm. A 30nm oxide overlapped depletion region is present on both sides of the source and drain, this region is to reduce impact ionization and improve ON current. The vertical dimension of the Si ground plane and SiO_2 spacer is 20 nm each. The length of both parted drain regions D1 and D2 are varied to get the optimal dimensions for better characterizations and in these structures, both drain parts' vertical lengths are 30nm each for SD-SG TFET and 5nm for the other three TSD-SG TFET, MSD-SG TFET, BSD-SG TFET. The dielectric used for the gate electrode is SiO_2, which has a thickness of t_{ox} = 1nm and the dielectric constant is 3.9. Table 3.1 summarizes all the parameters for all the structures. present in a conventional TFET.

Parameters name/unit	Symbol	SD-SG TFET	TSD-SG TFET	MSD-SG TFET	BSD-SG TFET
Source doping (cm^{-3})	N_s	1×10^{20}	1×10^{20}	1×10^{20}	1×10^{20}
Channel doping(cm^{-3})	N_{ch}	1×10^{17}	1×10^{17}	1×10^{17}	1×10^{17}
Drain doping (cm^{-3})	N_{D1}	5×10^{18}	5×10^{18}	5×10^{18}	5×10^{18}
	N_{D2}	1×10^{17}	1×10^{17}	1×10^{17}	1×10^{17}
Substrate doping (cm^{-3})	n_i	1×10^{17}	1×10^{17}	1×10^{17}	1×10^{17}
source length (nm)	X_s	100	100	100	100
Channel Length (nm)	L	50	50	50	50
Effective Channel Length (nm)	L_{eff}	50	50	60	70
Drain Length (nm)	X_d	100	100	100	100
source width (nm)	Y_s	60	60	60	60
Channel width (nm)	W	60	60	60	60
Drain width (nm)	Y_{d1}, Y_{d2}	30, 30	5,5	5,5	5,5
Length of electrical drain (nm)	L_{ED}	70	5	5	5
Silicon body thickness	T_{si}	60	60	60	60
Oxide thickness (nm)	T_{ox}	1	1	1	1
Work function of control gate (eV)	$\emptyset ms$	4.1	4.1	4.1	4.1
Substrate, box thickness (nm)	T_{box}	20	20	20	20

Table 3.1 summarizes all the parameters for all the structures.

3.4 Analytical Modelling

3.4.1 Electric field

The expression for the electric field in the channel region is given by

$$\varepsilon(x) = \frac{1}{\epsilon}\int \Psi dx \qquad (1)$$

Where Ψ is the charge density as given in Fig. 2, which depicts the space charge distribution using rectangular approximation. The channel starts from the origin (0, 0) with gate length L_{ch}, and source and drains depletion length as L_s and L_d respectively.

The electric field equation is obtained using (1) with respect to space charge distribution for structure Splitted-Drain Single-Gate TFET (SD-SG TFET).

For $-L_s \leq x < 0$;

$$\varepsilon(x) = \frac{-qN_s}{\epsilon}(L_s + x) \qquad (2)$$

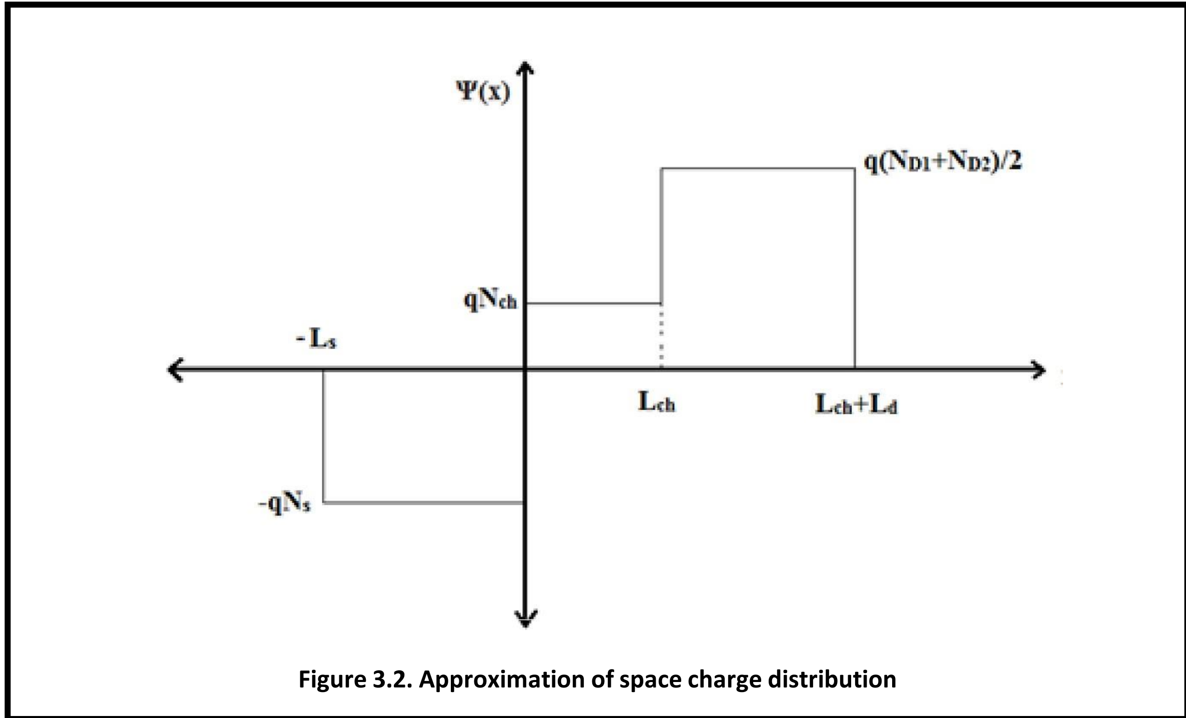

Figure 3.2. Approximation of space charge distribution

For $0 \leq x < L_{ch}$;

$$\varepsilon(x) = \frac{-qN_s}{\epsilon}L_s + \frac{qN_s}{\epsilon}x \qquad (3)$$

For $L_{ch} \leq x < L_{ch} + L_d$;

$$\varepsilon(x) = \frac{-qN_s}{\in} L_s + \frac{qN_{ch}}{\in} L_{ch} + \frac{q(N_{D1} + N_{D2})}{2 \in} (x - L_{ch}) \quad (4)$$

The electric field across source, channel and drain region is given in (2), (3) and (4) respectively and is similar for all the other structures TSD-SG TFET, MSD-SG TFET, BSD-SG TFET as the charge distribution is kept equivalent in every region for all structures. Since the electric field is continuous across Si-SiO_2 interface, the equations are also applicable to all the four structures with discrete width W_{d1} and W_{d2} and discrete doping $N_{D1}$and $N_{D2}$of splitted parts respectively.

3.4.2 Potential distribution

The analytical modelling is based on Fermi-Dirac Distribution instead of Boltzmann approximation, where the total barrier lowering is equal to summation of built-in potential and applied voltage. Thus, the potential distribution along charge distribution is given by (5) and extended equation, see (6).

$$V_{bi} + V_{DS} = -\int_{-L_s}^{L_{ch}+L_d} \varepsilon(x)dx \quad (5)$$

$$V_{bi} + V_{DS} = -\int_{-L_s}^{0} \frac{-qN_s}{\in}(L_s + x)dx - \int_{0}^{L_{ch}} \left(\frac{-qN_s}{\in}L_s + \frac{qN_s}{\in}x\right) dx - \int_{L_{ch}}^{L_{ch}+L_d} \left(\frac{-qN_s}{\in}L_s + \frac{qN_{ch}}{\in}L_{ch} + \frac{q(N_{D1} + N_{D2})}{2 \in}(x - L_{ch})\right) dx \quad (6)$$

The potential can be plot by the quadratic equation from with respect to L_s, L_{ch}, Ld.

Where $V = V_{bi} + V_{DS}$ (7)

V_{bi} is the built-in potential given by (8)

$$V_{bi} = V_T \log\left(\frac{N_s N_{ch}}{n_i^2}\right) \quad (8)$$

Obtaining potential distribution by replacing$L_d$using continuity equation.

$$L_d = \frac{2(N_s L_s - L_{ch} N_{ch})}{N_{D1} + N_{D2}} \quad (9)$$

For source region, potential distribution is given by V1, refer (10). For channel region, potential distribution is given by V2, see (11). For drain region potential distribution is given by V3, replace L_s using continuity equation see (12).

$$V1 = -\frac{q}{2g}[(N_s - \frac{N_s^2}{N_d}) L_s^2 + ((2N_s L_{ch}) + (\frac{2N_s L_{ch} N_{ch}}{N_d})) L_s + (N_{ch} L_{ch}^2) - (\frac{N_{ch}^2 L_{ch}^2}{N_d})] \quad (10)$$

$$V2 = -\frac{q}{2g}[(N_{ch} - \frac{2N_{ch}^2}{N_d} - 2N_{ch}) L_{ch}^2 + ((-2N_s L_s) + (\frac{2N_s L_s N_{ch}}{N_d})) L_{ch} + (N_s L_s^2) - (\frac{N_{ch}^2 L_{ch}^2}{N_d})] \quad (11)$$

$$V3 = -\frac{q}{2g}[(\frac{N_d^2}{N_s} - 2N_d) L_d^2 + ((-2N_d L_{ch}) + (\frac{2N_d L_{ch} N_{ch}}{N_s}) - (2N_d L_{ch} N_{ch}) + (2L_{ch} N_{ch}) + (2N_d)) L_d - (N_{ch} L_{ch}^2) + (\frac{N_{ch}^2 L_{ch}^2}{N_s})] \quad (12)$$

Similarly, potential profile for TSD-SG TFET, MSD-SG TFET can be modelled using space charge distribution method. The lateral potential distribution of TSD-SG TFET, MSD-SG TFET, BSD-SG TFET is similar to Splitted-Drain Single-Gate TFET (SD-SG TFET) given in (10)-(12) for source, channel and drain respectively. Figure 3.3 shows the analytical and simulation graphs obtained for potential distribution of SD-SG TFET. One of the drawbacks of TFET devices are complex analytical modelling compared to MOSFET. Here we have considered the potential distribution of the structure as it appeared to be more convenient because of the doping variation in splitted drain structure. However, our proposed structure has an advantage of similar analytical model for surface potential like conventional p-i-n TFET structure. Thus, the analytical model of surface potential obtained from 2D Poisson equation for TFET can also be considered for our proposed structures by taking the average doping in drain region. This can be justified by Figure.3.4 which show the net absolute doping in the SD-SG TFET device. It validates the dependency of tunnelling approach on the average doping of splitted drain parts.

3.4.3 Drain Current

The band-to-band tunnelling rate is described by the Kane's model. It determines the generation rate (G_{Kane}) per unit volume. The generation rate is the tunnelling of the carrier from the source valence band to channel conduction band and is given by (13) [3.24].

$$G_{Kane} = A_{Kane}\, E^{D} exp(-B_{Kane}\, E_g^{3/2}/\varepsilon) \quad (13)$$

Where $A_{Kane}$and B_{Kane} are material dependent constant, ε is the electric field, $E_g$is the band gap, D is the parameter for direct (D=2) and indirect (D=2.5) tunnelling process. So the BTBT tunnelling rate and current in junction region for 3D surface volume can be gained by [3.23], [3.29].

$$G_{BTBT} = \frac{q^2\sqrt{m_r^*}}{2\pi h^2 Eg^{0.5}} E^2 \exp\left(\frac{-\pi\sqrt{m_r^*}Eg^{1.5}}{2qhE}\right) \Delta\ \varepsilon. \quad (14)$$

$$Ids = q \int G_{BTBT}\, dv \qquad (15)$$

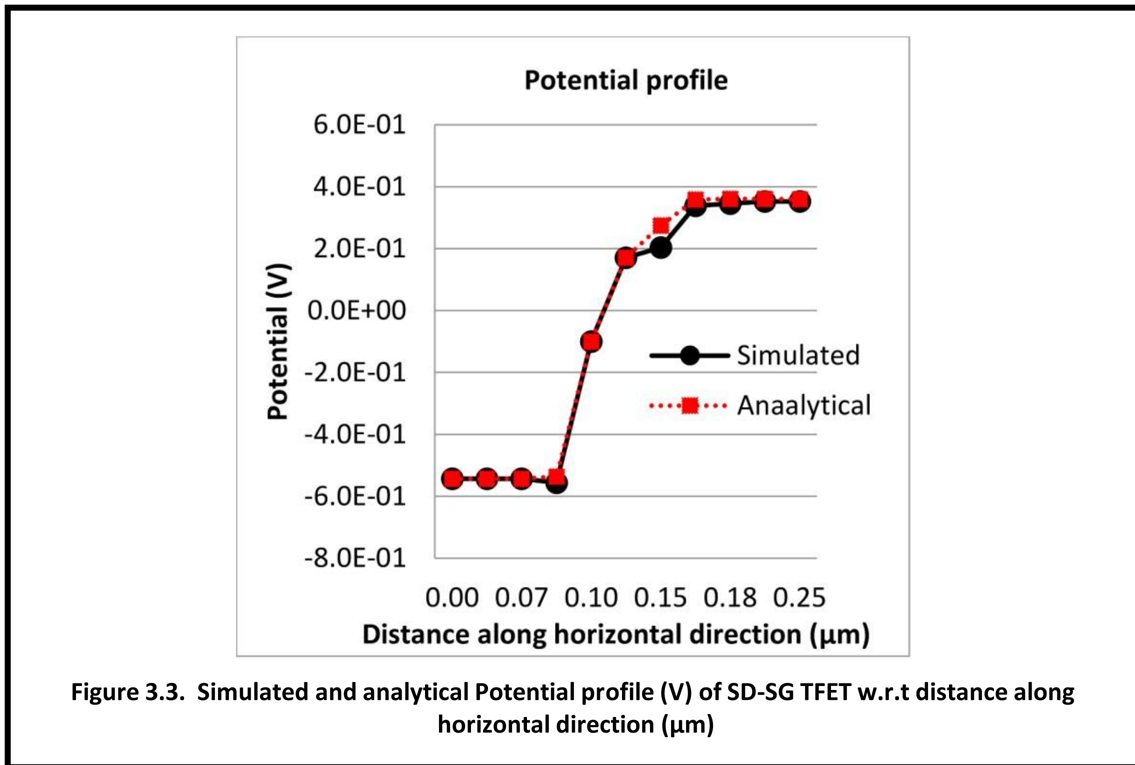

Figure 3.3. Simulated and analytical Potential profile (V) of SD-SG TFET w.r.t distance along horizontal direction (µm)

Where m_r^* is the effective mass, $\frac{1}{m_r^*} = \frac{1}{m_h^*} + \frac{1}{m_e^*}$, $\Delta\varepsilon$ is energy range. The potential distribution is separately calculated for lateral and vertical direction as the lateral electric field and potential is responsible for variation of ON current, however the OFF current depends on vertical parameters as the drain is vertically sub-divided into two parts. The splitted drain is both n type with different doping concentration, so in case of higher Vds, the lower drain region can substitute charge to upper region instead of reverse charge conduction. Due to this charge normalisation, reduction of leakage current subjugates the ambipolarity. type with different doping concentration, so in case of higher Vds, the lower drain region can substitute charge to upper region instead of reverse charge conduction. Due to this charge normalisation, reduction of leakage current subjugates the ambipolarity.

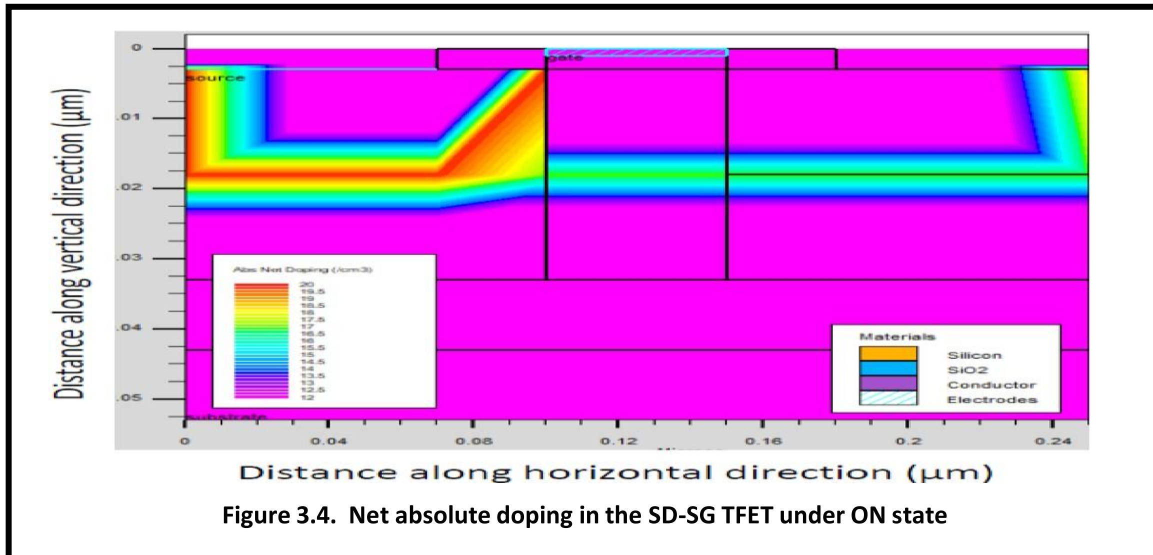

Figure 3.4. Net absolute doping in the SD-SG TFET under ON state

3.5 Simulation Setup

All the simulations are performed using Silvaco Atlas version 5.20.2. R by including appropriate mathematical models such as nonlocal BTBT (BBT.NONLOCAL), Lombardi mobility model (CVT), bandgap narrowing model, Fermi–Dirac statistics and the Shockley–Read–Hall and Auger recombination models and Drift-diffusion carrier transport. The generation rate is calculated by BTBT model by defining the quantum tunnelling region at sourc-channel and drain-channel interface for considering ambipolarity. Fermi–Dirac statistics is carrier model which provides carrier concentration to state the mobility of the field. Shockley Read-Hall recombination model uses SRH parameter and Auger recombination model uses AUGER parameters, which are responsible for including the carrier energy exchange in their surrounding lattice and carrier life time.

3.6 Results and discussions

3.6.1 Potential and Electric Field Profile

Our approach to subdue the ambipolar conduction and improving tunnelling phenomenon by using this novel structure can be analyzed from the graph given below. figure. 3.5 figure. 3.6 exhibit the comparative visual plot of potential distribution profile and electric field distribution profile which indicates that the structure BSD-SG TFET exhibits better tunnelling even at low voltage of 0.5 V. The minimum potential and electric field variation across source channel interface indicate easy carrier tunnelling in BSD-SG TFET. With reference to the work

cited in he paper [13] result follows vertical rise travel path for the carriers instead of a path with minimum resistance and are more crowded in places close to the gate oxide and source/drain contacts. Accordingly, we have modelled these structures validating our model. However, in our developed models the carriers follow the standard path as in normal TFET which can be observed from the result plots shown in figure 3.5 and figure 3.6.

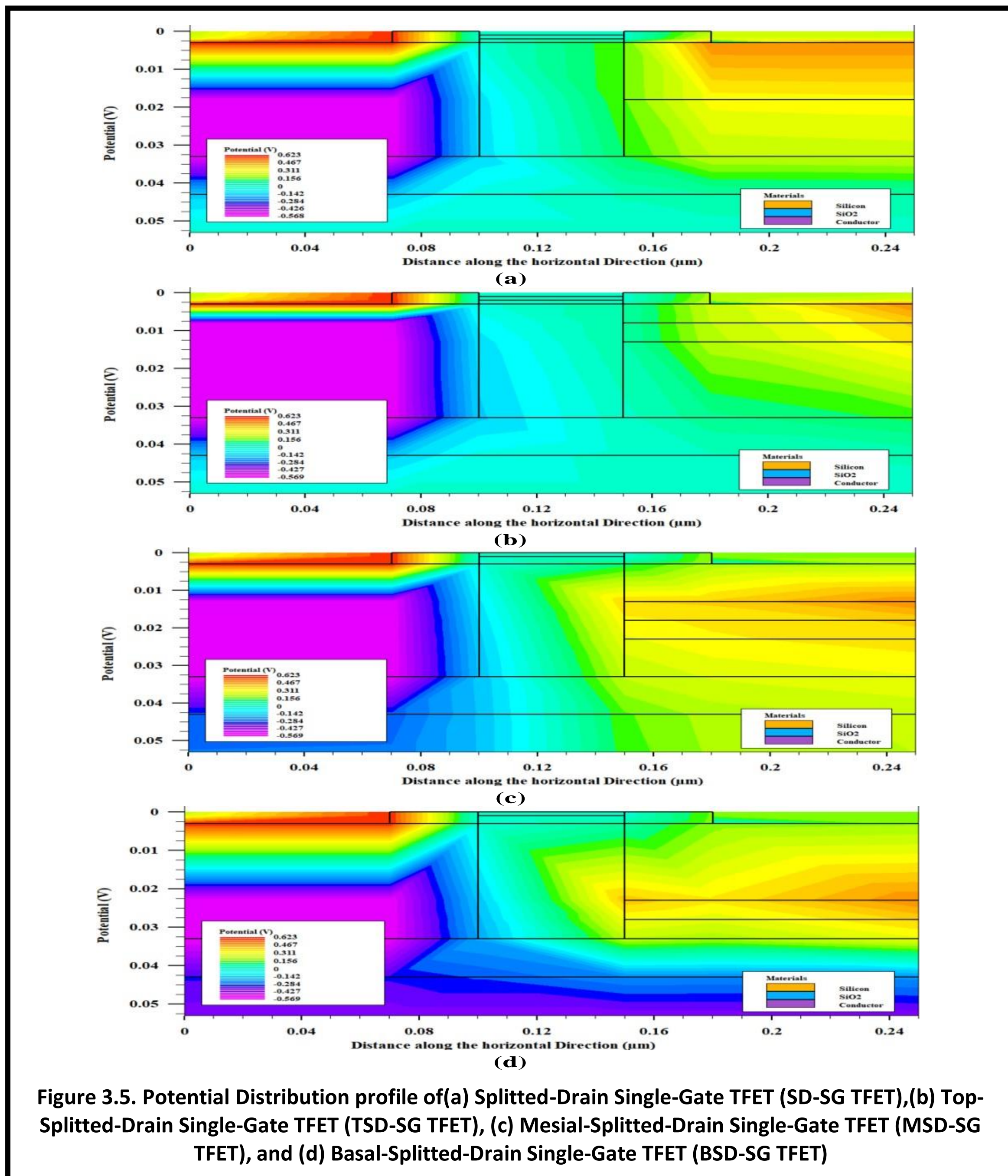

Figure 3.5. Potential Distribution profile of(a) Splitted-Drain Single-Gate TFET (SD-SG TFET),(b) Top-Splitted-Drain Single-Gate TFET (TSD-SG TFET), (c) Mesial-Splitted-Drain Single-Gate TFET (MSD-SG TFET), and (d) Basal-Splitted-Drain Single-Gate TFET (BSD-SG TFET)

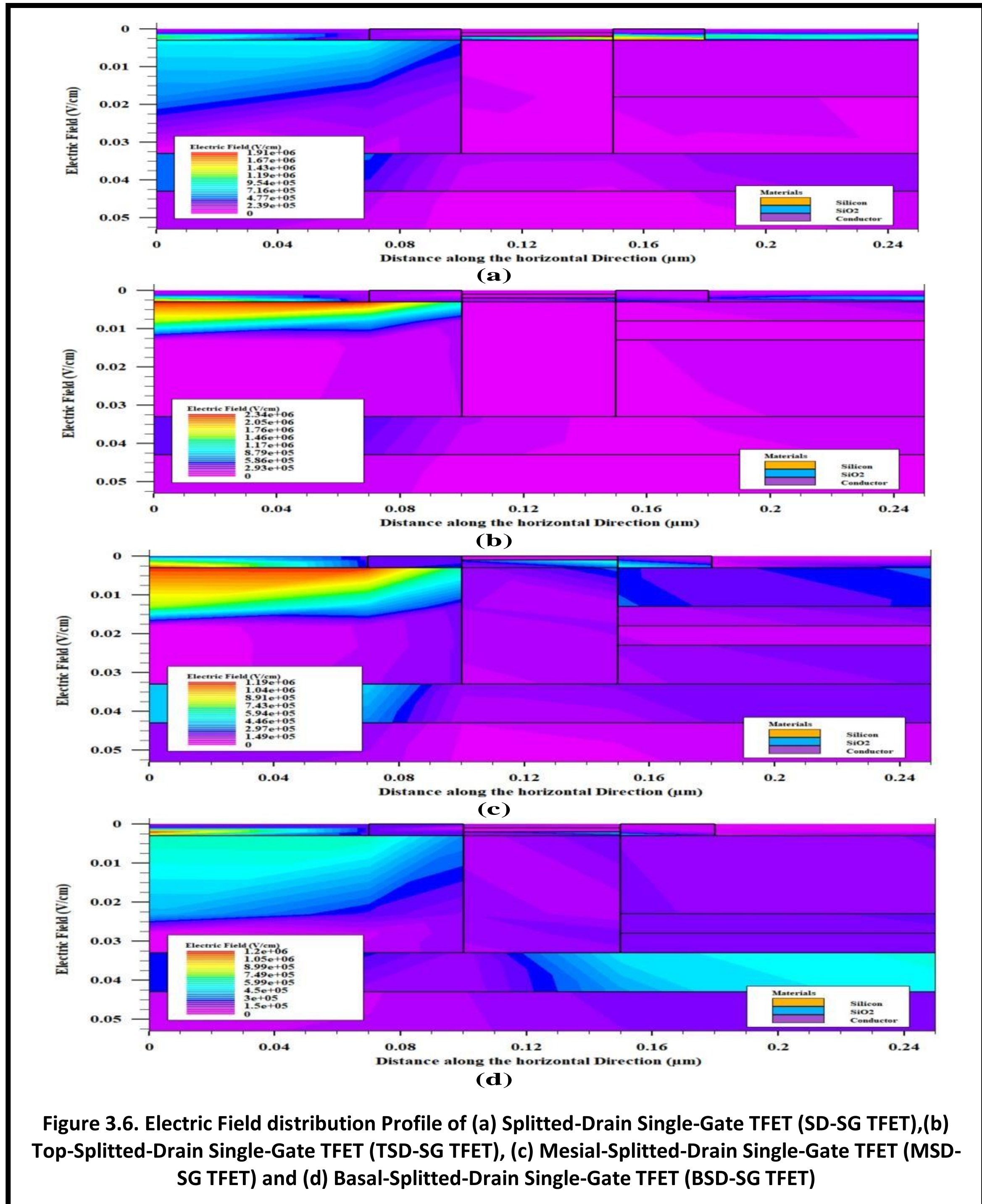

Figure 3.6. Electric Field distribution Profile of (a) Splitted-Drain Single-Gate TFET (SD-SG TFET),(b) Top-Splitted-Drain Single-Gate TFET (TSD-SG TFET), (c) Mesial-Splitted-Drain Single-Gate TFET (MSD-SG TFET) and (d) Basal-Splitted-Drain Single-Gate TFET (BSD-SG TFET)

Figure 3.7 and figure 3.8 indicate comparative analysis of the potential distribution profile and electric field distribution profile for all the four structures. As there is changes the position of the drain in all four different SG-TFET structures, so the potential profile almost looks the same for all types of structural design. Potential profile graph of MSD-SG TFET and BSD-SG TFET in figure 3.7, display overall tunnelling and progressive track from source to drain compared to other two structures.

In electric field graph in figure 3.8, BSD-SG TFET has higher overshoot implying greater degree of tunnelling. An additional peak is observed in the same upward direction towards drain end suggesting immunity to DIBL effect. This makes the proposed structure screened to drain bias and more Gate dependent and the peak at the beginning of the drain indicates that there is a sign of the occurrence ambipolar current. Thus, all the structures exhibit lower electric field at drain side reflecting reduced hot carrier effect.

3.6.2 Band Diagram Analysis

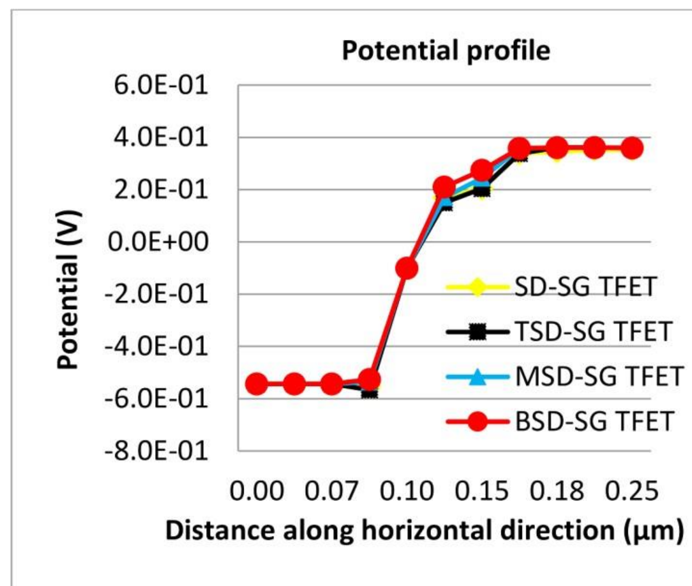

Figure 3.7. Comparative Plot of Potential distribution graph of SD-SG TFET, TSD-SG TFET, MSD-SG TFET and BSD-SG TFET w.r.t distance along horizontal direction (µm)

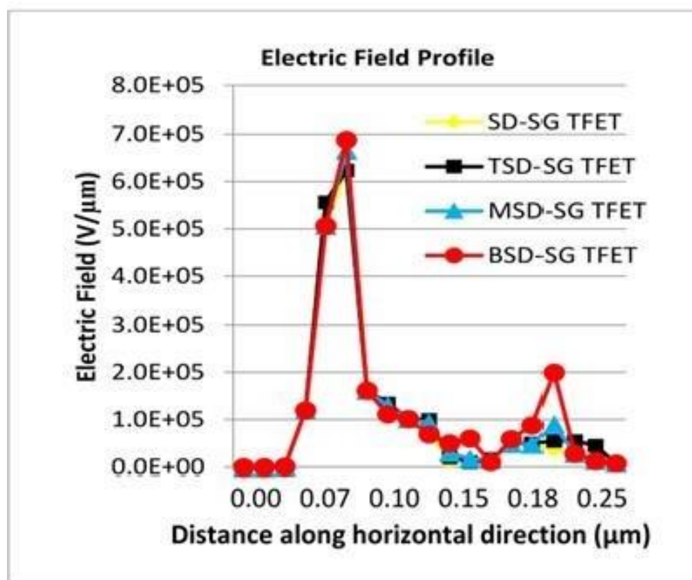

Figure 3.8. Comparative Plot of electric field distribution graph of SD-SG TFET, TSD-SG TFET, MSD-SG TFET and BSD-SG TFET w.r.t distance along horizontal direction (µm)

Figure 3.9 compares the band diagram for all structures Splitted-Drain Single-Gate TFET (SD-SG TFET), Top-Splitted-Drain Single-Gate TFET (TSD-SG TFET), Mesial-Splitted-Drain Single-Gate TFET (MSD-SG TFET) and Basal-Splitted-Drain Single-Gate TFET (BSD-SG TFET) for effective channel length of 50 nm, 50nm, 60nm and 70nm respectively. The band diagram is obtained for Drain voltage V_{ds} of 0.5 V. After analysing the graph below in figure 3.9, it can be observed that all four structures show better tunnelling profile which can be understood from the density of state switch band diagram explained in below section, this induce lower leakage and optimized ambipolar conduction compared to conventional TFETs. The composite Structure BSD-SG TFET has lower width of tunnelling window in source-channel junction suggesting reduction in tunnelling resistance and higher current driving capability. This structure also exhibits lower conduction band bending state in channel-drain interface than valence band state band bending at interface, thus ruling out possibility of reverse conduction from drain to channel, resulting minimized ambipolar conduction than the other three structures. Further energy band variation can be optimized by maintaining suitable doping and length modulation. Figure 3.10 presents the effect of width modulation of upper part of drain D1 on energy band bending of structure SD-SG TFET, when the upper highly doped region, Yd1 is 25% of the total drain region, thus the band bending in drain side is causing more reduction of reverse conductivity.

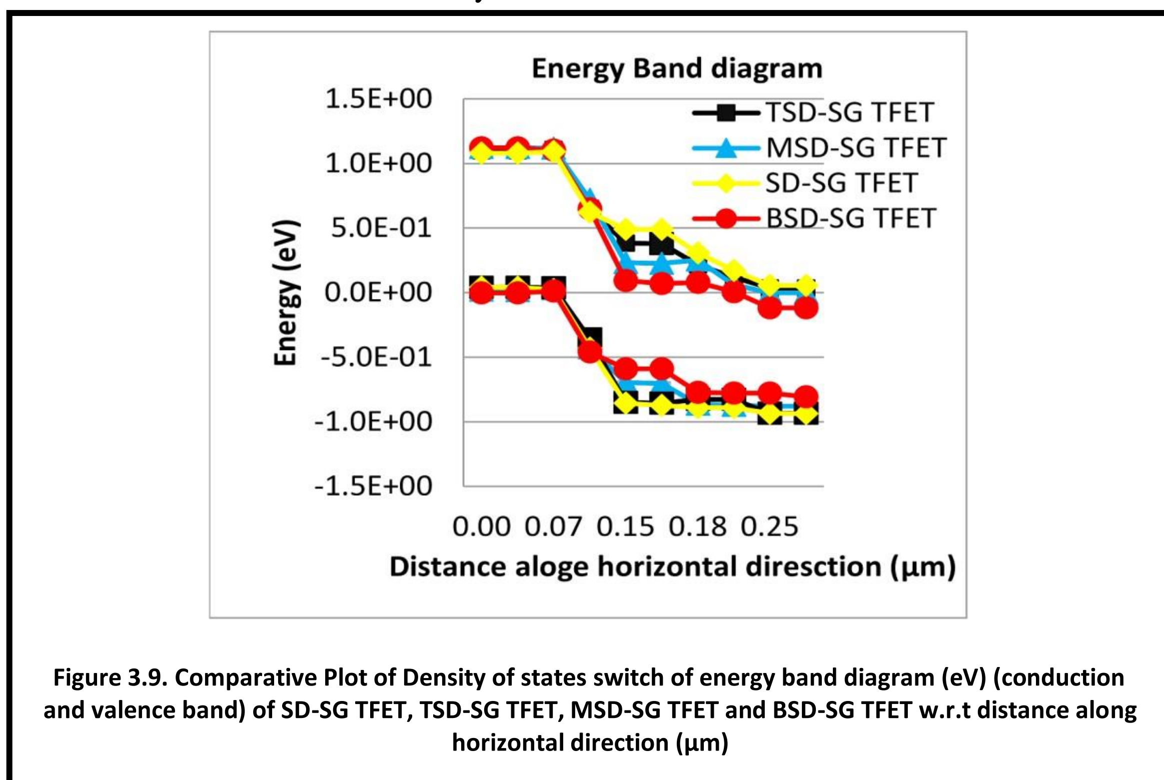

Figure 3.9. Comparative Plot of Density of states switch of energy band diagram (eV) (conduction and valence band) of SD-SG TFET, TSD-SG TFET, MSD-SG TFET and BSD-SG TFET w.r.t distance along horizontal direction (µm)

3.6.3 Optimization of Ambipolar Conductivity

TFET exhibits unwanted ambipolar conduction due to the inability to form tunnel junction at source-channel and channel-drain interfaces. To compensate the ambipolar conduction, gate–drain underlap structure is proposed but it lowers the current driving capacity, thus this proposed drain engineered structures have advantage over those underlapped structures. If the above half of the drain region is highly doped than the lower half, the tunnelling width at the channel-drain interface increases which in turn reduce the ambipolar current without hampering the ON state current in the TFET. The reduction of the ambipolar current can be observed from the density of states switch band diagram in figure 3.9 and figure 3.10. The sub-threshold slope for tunnelling depends on the steepness of the band edges, and in the above figures the highest point of valence band is almost parallel to the lowest point of conduction band in all four structures, and in structure BSD-SG TFET, the conduction band bending is lower than valence band at channel-drain interface, and as per the switching principle there is minimum possibility of ambipolar conduction by modulating the tunnel barrier by drain doping engineering- splitted drain structure. Further reduction in reverse current can be justified by electric field graphs given in Fig. 8. The second positive ascent in channel- drain interface suggest forward tunnelling, thus less probability of carrier flowing from drain side to channel side, optimizing ambipolarity. With reference to the work [3.13] it has been studied the impact of f two-pocket drain doping (N+ and N- pocket drain regions) as an effective means to conquer the ambipolar conduction in TFETs. We demonstrated that, by this drain doping engineering, the ambipolar behaviour is effectively suppressed.

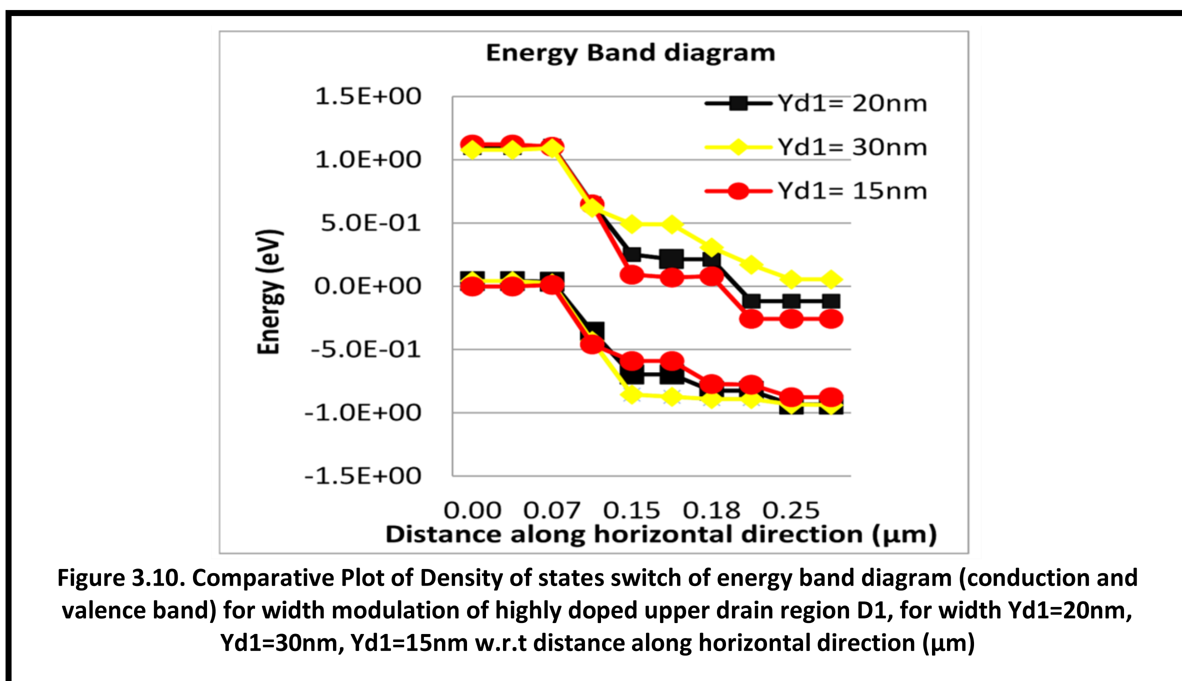

Figure 3.10. Comparative Plot of Density of states switch of energy band diagram (conduction and valence band) for width modulation of highly doped upper drain region D1, for width Yd1=20nm, Yd1=30nm, Yd1=15nm w.r.t distance along horizontal direction (μm)

3.6.4 Transfer Characteristics

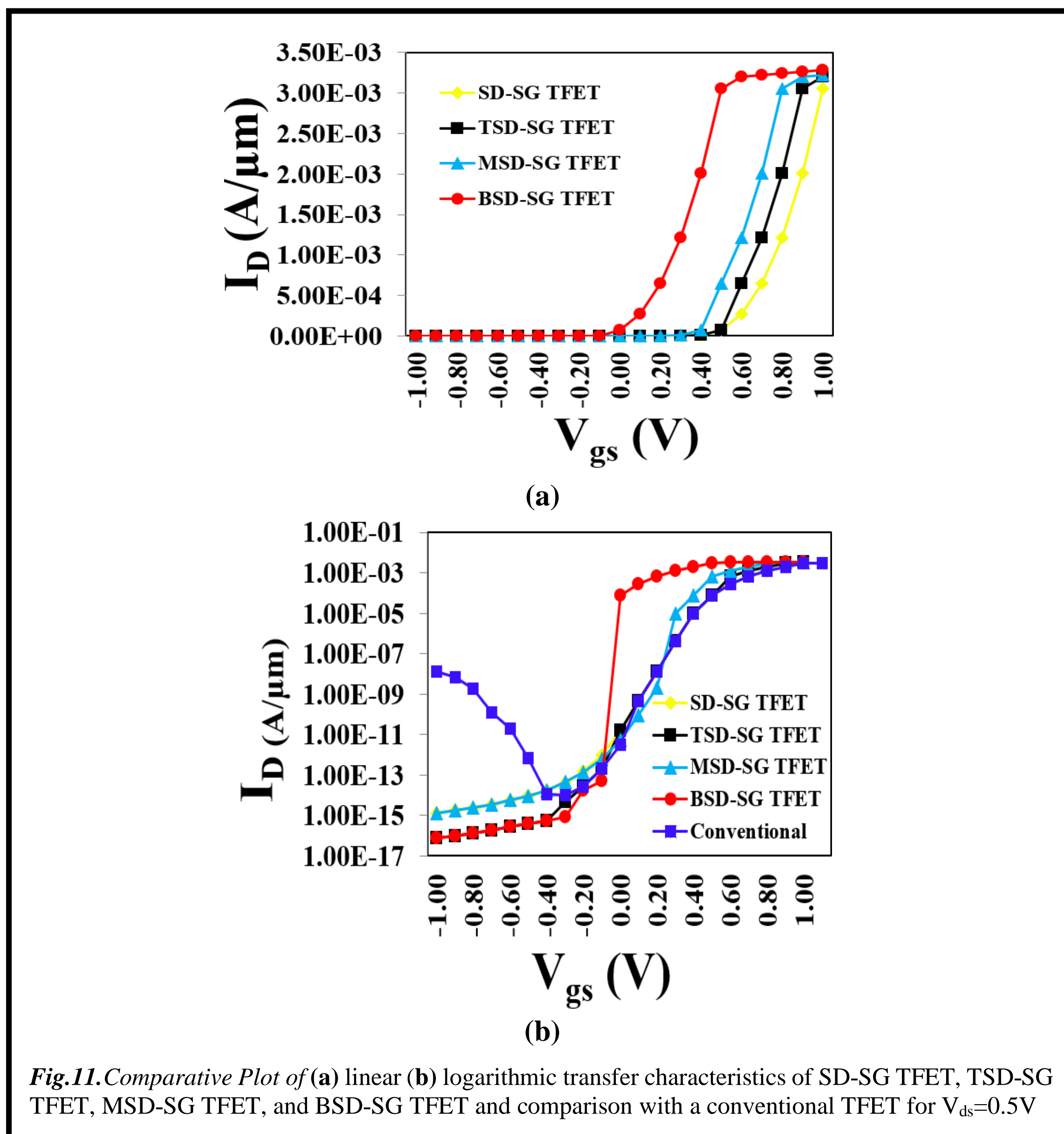

Fig.11.*Comparative Plot of* **(a)** linear **(b)** logarithmic transfer characteristics of SD-SG TFET, TSD-SG TFET, MSD-SG TFET, and BSD-SG TFET and comparison with a conventional TFET for V_{ds}=0.5V

Figure 3.11 (a)compares the transfer characteristics for the four structure SD-SG TFET, TD-SG TFET, MSD-SG TFET and BSD-SG TFET and Figure 3.11 (b)compares the transfer characteristics for the four structure SD-SG TFET, TD-SG TFET, MSD-SG TFET and BSD-SG TFET with an conventional TFET . The drain current is slightly more for BSD-SG TFET as the effective channel length of BSD-SG TFET is 70nm and thus more compared to other structures. Also, BSD-SG TFET can be turned on by applying very low voltage making more suitable for low power devices, followed by MSD-SG TFET and TD-SG TFET, with effective channel length of 60 nm and 50 nm respectively. Ambipolar reduction can be seen from the log transfer characteristic given in Figure 3.11. compared to conventional TFETs [3.30]. From

the Figure 3.11 it can also be observed that the structure BSD-SG TFET has highest ON current starting around in the range of 1×10^{-3} A and OFF current starting around in between 1×10^{-16} A to 1×10^{-17} A Therefore, all the proposed structures have relatively low OFF current as compared to planar TFET as evidenced from the transfer function without hampering the ON current, thus all the structures have relatively high I_{ON}/I_{OFF} ratio than other standard TFET due to higher effective channel length.

3.6.5 Drain Output Characteristics

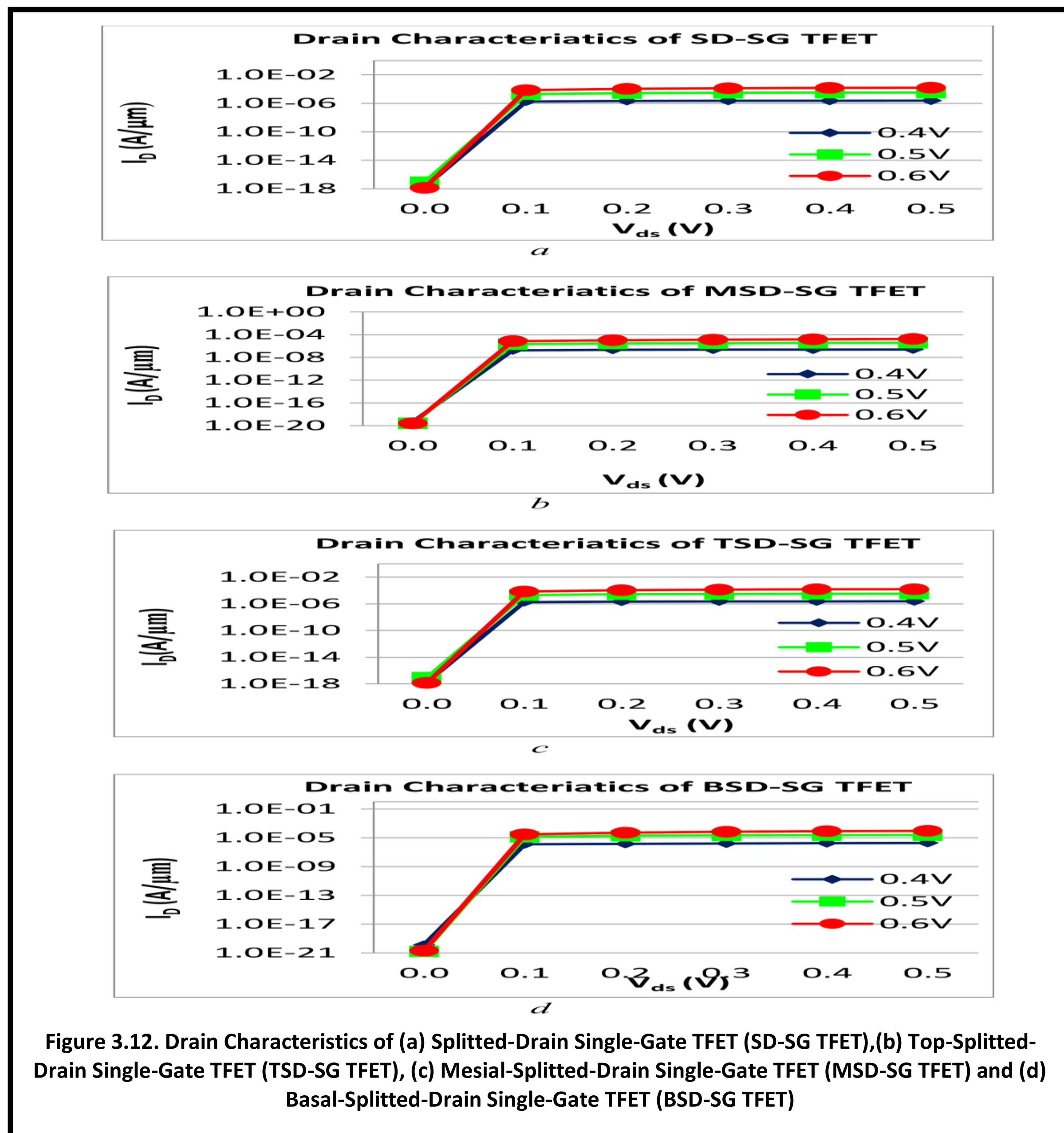

Figure 3.12. Drain Characteristics of (a) Splitted-Drain Single-Gate TFET (SD-SG TFET),(b) Top-Splitted-Drain Single-Gate TFET (TSD-SG TFET), (c) Mesial-Splitted-Drain Single-Gate TFET (MSD-SG TFET) and (d) Basal-Splitted-Drain Single-Gate TFET (BSD-SG TFET)

Figure 3.12 compares the drain output characteristics for the four structure SD-SG TFET, TSD-SG TFET, MSD-SG TFET and BSD-SG TFET. Here, drain voltage V_{ds} is swept to 0.5V and obtained characteristics for 0.4V, 0.5V and 0.6V gate bias voltage. In the figure 3.13 drain output characteristics of the proposed models and conventional TFETs is evaluated and compared for all the developed structures for optimal biasing range of V_{ds} up to 0.5V.

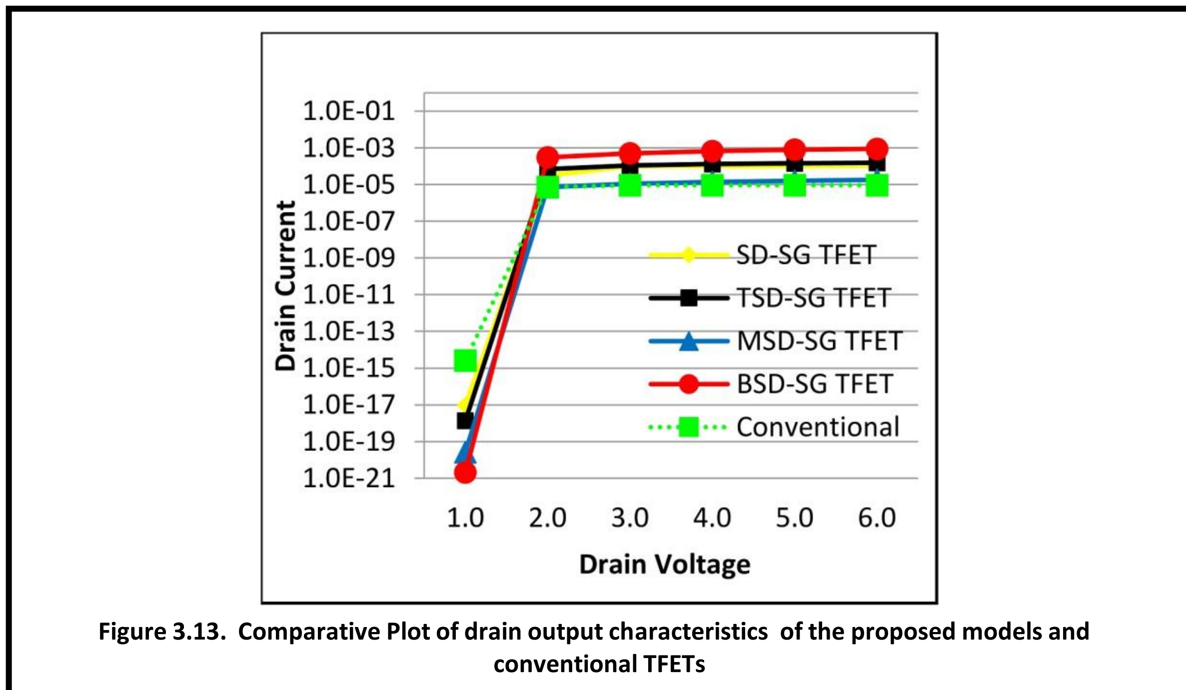

Figure 3.13. Comparative Plot of drain output characteristics of the proposed models and conventional TFETs

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Chapter:4

Chapter 4: Analytical Modelling and optimization of Double Trench Gate Covered TFET suitable for Low-Power Application

4.1 Introduction..105
4.2 Literature Review..107
4.3 Proposed Device Structure and its Parameters................109
4.4 Analytical Modeling..111
4.5 Device Structure and Simulation..117
4.6 Results and Discussion..119
4.6.1 Voltage Optimization..119
4.6.2 Variation of Extended Source Length Ls..................121
4.6.2.1 Energy Band Diagrams..121
4.6.2.2 Electric Field..123
4.6.2.3 Potential Profile..124
4.6.3 Transfer Characteristics..125
4.6.4 Quantum Confinement Effect..126
4.7 DTG-CSC-TFET Inverter..128
References..131

4.1 Introduction

The current generation in MOSFETs is determined by the thermionic emission of high energy carriers, in which only carriers with energy exceeding the source-channel electrostatic potential barrier contribute to the I_{ON}. These high energy carriers follow the Fermi–Dirac distribution and hence have an energy slope of kT (where k is the Boltzman's constant, T is the absolute temperature), causing a thermal limited SS of 60 mV/ decade at the 300 K. Continued transistor scaling and transistor density increasing have significantly increased the power density on-chip. Supply voltage V_{DD} scaling leads to a quadratic reduction of the dynamic power consumption, which is highly desired for energy-efficient computing in power-constrained applications [4.1]. To achieve the same I_{ON}, V_{th} has to be scaled proportionately while reducing the V_{DD} of a transistor, causing an exponential increase in the leakage current and static leakage power [4.2]. This exponential increase of I_{OFF} arises from the thermal limited 60 mV/decade SS in MOSFETs. The trade-off between the V_{th} reduction and low static leakage

power slows the V_{DD} scaling and thereby restrains the further power reduction for high-performance, low-power device applications.

Unlike MOSFETs, TFETs are designed with asymmetrical source/drain doping (p-i-n) as reverse-biased gated p-i-n diodes. The current generation in TFETs is based on quantum mechanics with BTBT. However, the low I_{ON} is an inherent disadvantage in traditional TFETs. In order to improve the I_{ON} of TFETs, structural modification needs to be incorporated into a conventional TFET so that both Point tunnelling and line tunnelling will occur. Point tunneling is the most common type of carrier generation method. The maximum carrier generation rate is almost confined to a point and occurred mainly at the source-channel junction region, in which the carriers at the high energy tail of the Fermi–Dirac distribution are filtered by a tunneling window [4.3] and it gives the prime contribution is localized in a small area. However, for line tunnelling, a gate overlap is created over the source region. The electric field thus formed has to be in a direction that aids tunnelling. The electrons from the inner parts of the source tunnel to the inversion region formed near the surface of the source (for n-TFET). The carrier generation takes place in a line, near the source-gate oxide interface, hence the name is line tunnelling. Since the carrier generation, area/ dimension is larger than point tunnelling, the I_{ON} increases. As subthreshold current is not limited by the Boltzmann distribution of the carrier, an ultra-steep SS of less than 60 mV/dec at the room temperature can theoretically be obtained [4.4–4.6], resulting in high on- I_{ON}/I_{OFF} ratios at low voltages. Therefore, TFET can reduce the supply voltage and the static power consumption of the device. TFET can also operate with a larger transconductance to-current ratio than traditional FET in the sub-threshold region [4.7]. In addition, the higher output resistance offered by TFET-based designs allows for achieving significantly higher intrinsic voltage gain and higher maximum-oscillation frequency at low current levels. Moreover, TFET- exhibits superior performance advantages in track-and-hold [4.8], ambient radio-frequency power scavenging [4.9], and digital to analog converter [4.10]. All these findings indicate that the TFET has a good application prospect in low-power devices [4.11]. However, due to the characteristics of the structure in the TFET, there are still some challenges in circuit design using TFETs. TFET can also operate with a larger transconductance to-current ratio than traditional FET in the sub-threshold region [4.7]. In addition, the higher output resistance offered by TFET-based designs allows for achieving significantly higher intrinsic voltage gain and higher maximum-oscillation frequency at low current levels. Moreover, TFET- exhibits superior performance advantages

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4.2 Literature Review:

Conventional TFETs that are fabricated on Si-substrates exhibit relatively lower I_{ON} as compared to their MOSFET counterparts. This is due to limited BTBT in such TFETs. In order to overcome the low I_{ON} several structural and/or material variations have been studied extensively and exhaustively as such

Khatami et al. [4.12], reported a nov n- and p-type T-FETs which exhibit very small subthreshold swings, as well as low threshold voltages which is based on heterostructure Si/intrinsic-SiGe channel layer.

Ionescu et al. [4.13] presented the TFET as an alternative to MOSFET as an efficient electronic switch by paying attention to power dissipation as a fundamental problem for nanoelectronics circuits.

Dutta et al [4.14] reported a renovated silicon-based TFET structure with 21 nm of channel length. The broken-gate TFET (BG-TFET) shows a very low ambipolar current, and good SS and ON-currents comparable to the contemporary structures of similar dimensions.

Saha, et al [4.15] develop 2D-analytical models of a DM-VSTB strained FET with a focus on SCE in the nanoscale range. Across gate/channel and dielectric wall/channel interface the potential is derived with the parabolic approximation method.

Seabaugh et al. [4.16] introduce the development of TFETs which provide a higher drive current than the MOSFET as V_{GS} when it approaches 0.1 Volt.

Saurabh et al. [4.17] demonstrate the application of a DMG-TFET to optimize the I_{OFF}, I_{ON}, V_{th} and improve the average SS, the nature of the output characteristics, and immunity against the DIBL.

Sarkhel et al [4.18] formulated a 2D-analytical model of TMG-DG-FET with step graded channel. Lower channel doping concentration and lower work-function metal near the drain side suppress the unwanted impact induced by HCEs, thereby making it a suitable ultra-low dimensional device.

Saha et al [4.19] developed nonconventional MOSFET structures which reduce various SECs that arise with the continuous minimization of device dimensions. Also explored the gate engineering and dielectric engineering on a Schottky barrier symmetric double-gate FET.

Ghosh et al. [4.20] proposed and investigated a Si-channel heavily n-type-doped JLFET, using two isolated gates with two different metal work functions, resulting higher I_{ON}/I_{OFF} ratio, less SS of ~38 mV/decade with high-k dielectric material (TiO_2) promises for a switching performance.

Lattanzio et al. [4.21] present germanium EH-TFET, explore the carrier tunneling through a bias-induced EH bilayer making it a suitable low-dimensional device.

Kumar et al. [4.22] had presented a DM-DG- TFETs with SiO_2/HfO_2 stacked gate-oxide structure. An analytical model is also derived for surface potential, electric field, I_{DS}, SS and V_{th} .

Upasana et al. [4.23] formulated a drain current model for DG P-N-I-N TFET using Lambert-W function which includes the impact of mobile charges, t_{ox} and t_{si} on quasi fermi level, V_{th}, V_{Gonset} and TBW over the entire operating range to accumulation inversion state.

Dash et al. [4.24] incorporate the analytical modeling and the benefits of asymmetric hetero-dielectric engineering DM-DG-TFET, which exhibits higher I_{ON} , better I_{ON}/I_{OFF} and suppressed SCE.

Padilla et al. [4.25] analysis of the Heterogate Electron–Hole Bilayer TFET with partially doped channels and documented the effects on tunneling distance modulation(TDM) and occupancy probabilities.

Kumar et al. [4.26] proposed a 2-D analytical model for DG TFETs for such surface potential, I_{DS}, and V_{th} with a SiO_2 /high-k stacked gate-oxide structure.

Bagga et al. [4.27], investigated an analytical model for TBM in TM-DG-TFET where the reverse tunneling of the carrier can be restricted by using three different metals. This mechanism allows a form of a barrier over the channel. The choice of metals with different work-functions helps in increasing the I_{ON} and also reduces the I_{OFF}.

Woo et al. [4.28] shows that the TFETs based on Si-channel have better process compatibility than those with III-V compound-based channels and heterojunctions. Germanium and III-V compounds are neither compatible with established conventional CMOS processes nor are they applicable to SOC designs that are presently based on silicon transistors.

In lieu of this, structural variations are plausible for addressing critical issues such as poor subthreshold slope and low I_{ON}. In order to ensure practical feasibility and viability, the

proposed structure is a Si-based TFET. Owing to the practical limitations on material variations, newer TFET models are being proposed by incorporating a variety of innovative structural modifications. Most recently line-tunneling type Z/ T / U/ L- shaped TFETs [4.29-4.32] have been considered to achieve better subthreshold swing and higher I_{ON} . Essentially, these structures comprise a source/channel/gate overlap region whereby the band-to-band tunneling is aligned parallel with the gate electric field. Such modifications achieve higher I_{ON}- as - (1) BTBT paths are short and 1D (2) the tunneling area is maximized. This is the motivation behind the proposed structure.

Kim et al. [4.33] investigated on the corner effect of L-shaped TFET and their fabrication method.

Kanrar et al. [4.34] present quantum analytical modeling of a sub-20 nm of DM-DG-TFET using a self-consistent solution of Schrödinger-Poisson's equation for sub-band quantization, bandgap shifting, tunnelling through the barrier.

Najam et al. [4.35] explored the impact of the geometrical quantum confinement effect (QCE) in LTFET as with feature sizes of 20nm or less, present-day TFET structures suffer from the quantum confinement effect (QCE).

4.3 Proposed Device Structure and its Parameters:

In this work, a novel Double Trench Gate Covered Source-Channel TFET [DTG-CSC-TFET] has been proposed. An analytical current model has been presented to obtain the expression for the ON-current in the DTG-CSC-TFET. The parameters have been optimized and the analytical model has been validated through Silvaco, Atlas simulations. The Double Trench-Gate with Covered Source-Channel allows for remarkable increase in tunneling area, which is reflected in sharply enhanced band-to-band tunneling rates. Hence, this device has greatly increased I_{ON} as compared to conventional planar TFETs. The proposed structure is depicted in figure 4.1. The source is extended well into the channel in order to maximize the region of channel that lies between the source and the gate. The trench gate height is denoted by L_T, the source extension length is denoted by L_S, the thickness of the channel between the source and gate is represented by t_{si} and the oxide thickness is t_{OX}. The oxide material near the source is HfO_2, which is a high-k dielectric and that near the drain is SiO_2, which is a low-k dielectric. Such a configuration enhances BTBT at the source-channel junction and reduces BTBT at the channel-drain junction, thereby suppressing the possibility of ambipolar

conduction. The low doped drain (LDD) region at the drain end also aids ambipolar current suppression.

The advantage of our proposed structure is that it enhances the I_{ON} not only due to the double gate structure but also due to the two quantum mechanical BTBT mechanisms that inherently occurs in the structure. The tunneling mechanism at the lateral part of the extended source region is point tunneling. Hence, tunneling takes place at the source-channel interface in the direction along the channel, under the influence of the gate. A second type of tunneling occurs in the part of the channel which lies between the source and the gate. BTBT occurs under the influence of the high vertical electric field in the narrow channel region. The carriers so generated, are swept towards the drain end under the lateral electric field generated by the drain bias. This type of tunneling is known as line tunneling. From figure 4.1 it may be assumed that $2(L_T+L_S)$ is the total length along which line tunneling occurs. This length hence plays a crucial role in determining the amount of BTBT that takes place in the structure. Also, figure 4.1 shows two cutlines which will be needed later for the analysis of the device parameters.

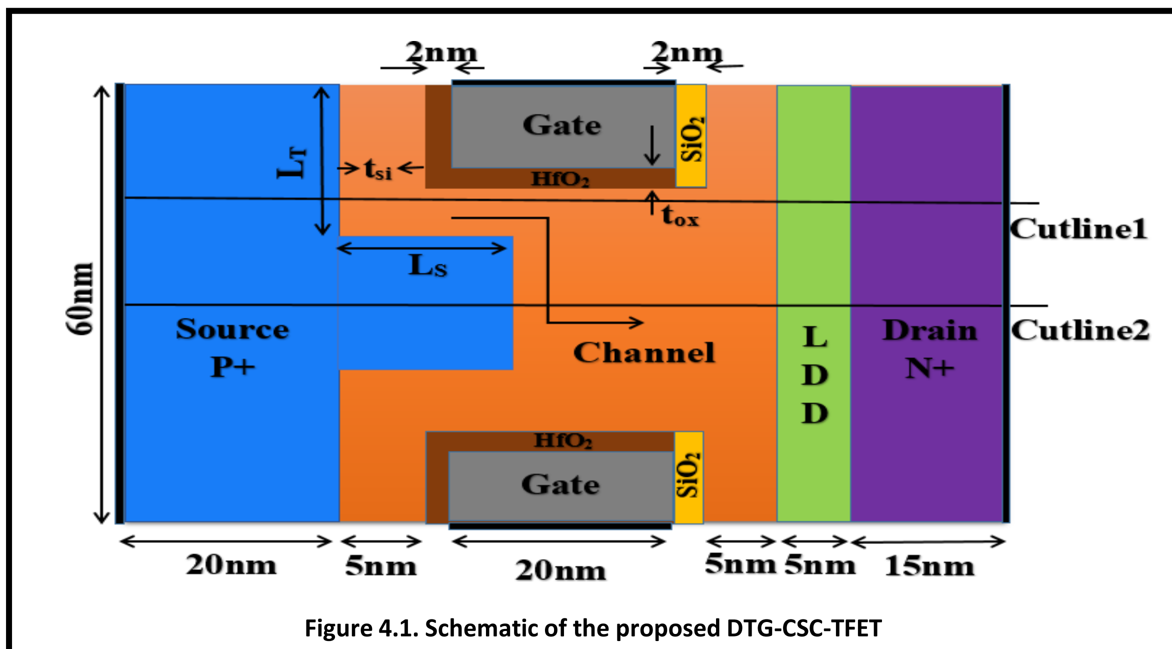


Figure 4.1. Schematic of the proposed DTG-CSC-TFET

Further going to implement any digital/analog application, the basic requirement is to design an inverter. But to comply the CMOS characteristics on a TFET, both N-TFET and P-Tfet should be designed properly by suppressing the ambipolar current for complementary performance [22-24]. In contrast, quantum simulation based approached is incorporated on the proposed DTG-CSC-TFET n-type and p-type TFET to improve device ON current and suppress the ambipolarity. Moreover, DTG-CSC-TFET inverter is simulated using SPICE calibration to evaluate its performance in circuit applications.

4.4 Analytical Modeling

In order to determine the total current, the contributions of the line tunneling and the point tunneling phenomena are calculated separately and the resultant currents are added. In practice, one tunneling mechanism may dominate the other depending on the oxide thickness, source-doping concentration, and biasing conditions [18].The carrier generation rate is calculated using Kane's Model as:

$$G = A\frac{\varepsilon^{D}}{\sqrt{E_G}}\exp\left(-BE_G{}^{3/2}/\varepsilon\right)$$
$$or$$
$$G = A\frac{E_G{}^{D-1/2}}{q^{D}w_{tun}{}^{D}}\exp\left(-Bq\sqrt{E_G}w_{tun}\right) \tag{1}$$

where Ɛ is the average electric field and is given as:

$$\varepsilon = \frac{E_G}{qw_{tun}} \tag{2}$$

In the above equations, G is the generation rate which is expressed as the number of carriers generated per unit volume per unit time, q is the charge, w_{tun} is the tunneling width, E_G is the energy bandgap and A, B & D are the Kane's model parameters whose values are material dependent. The default value of D is 2. Kane's model is applicable for the dimensions considered in the proposed DTG-CSC-TFET in accordance with [19]. The total current in the TFET may be determined by integrating the generation rate over the volume as:

$$|I| = q\int G\,dV \tag{3}$$

Figure 4.2 depicts the pathway of point tunneling. Here, the co-ordinates are so chosen that x=0 represents the source channel interface and y=0 is indicative of the gate & gate dielectric interface. In order to simplify the calculations the following assumptions have been made: (1) Potential drop due to depletion in the source is zero and the potential at x=0 is equivalent to the source potential. (2) Effect of charge in the channel on the channel potential is neglected. (3) Any charge that may be present in the gate dielectric is neglected. (4) Gate dielectrics with same electrical thickness will result in similar potential profile in the channel region.

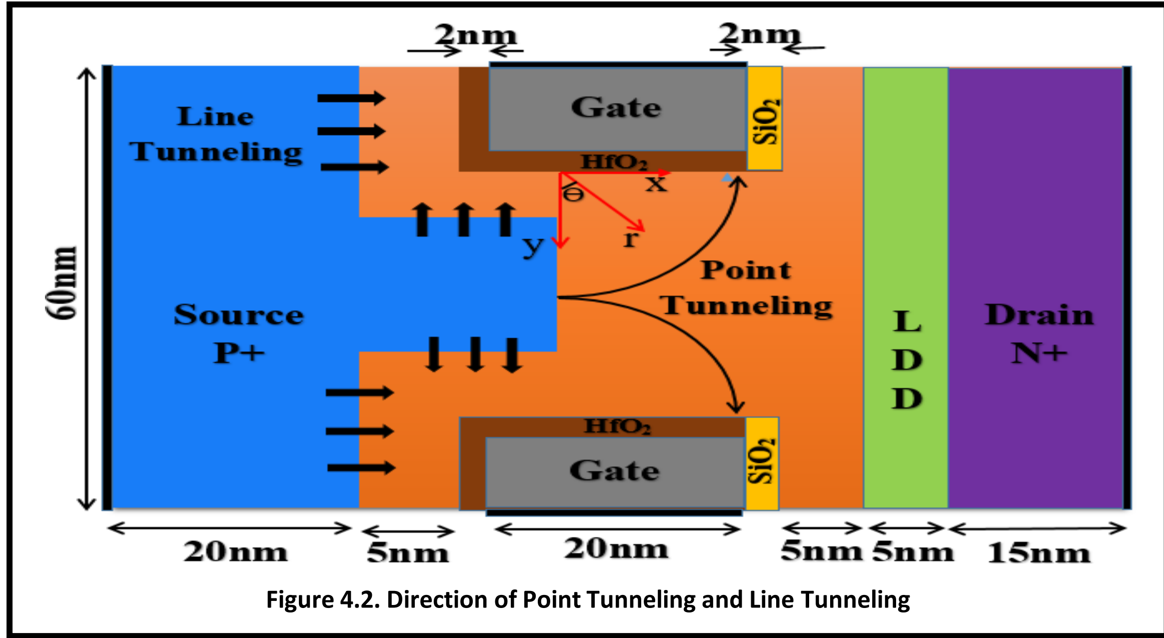


Figure 4.2. Direction of Point Tunneling and Line Tunneling

Towards assumption (4), the semiconductor equivalent thickness of the gate oxide is calculated as:

$$t_{ox}^{'} = t_{ox}\frac{\varepsilon_{Si}}{\varepsilon_{ox}} \tag{4}$$

where, ε_{Si} and ε_{ox} are the silicon and gate dielectric constant and t_{ox} is the physical dielectric thickness. The potential in the gate dielectric as well as the channel follow Poisson's Equation as:

$$\nabla^2\psi = -\frac{\rho}{\varepsilon} \tag{5}$$

where Ψ represents semiconductor valence band edge potential and ρ is the charge density. As per the assumptions, $\rho = 0$ in the gate dielectric and channel. Hence, Eq.(5) reduces to Laplace equation. Furthermore, the electrostatic potential obeys the following boundary conditions: $\Psi(0,y) = \Psi_S$ and $\Psi(x,0) = \Psi_G$. Assume that $\Psi_S = 0$ and $\Psi_G = V_{GS}-V_{FB}$, where V_{GS} is the applied gate bias and VFB is the flatband voltage.

Let the semiconductor extend towards infinity for (x>0 & y>0). Using the polar co-ordinates for the curved electric field lines, we represent potential as:

$$\psi(x, y) = \psi_G \frac{2}{\pi}\theta \quad ; \text{for } 0 \le \theta \le \pi/2 \tag{6}$$

Here, x = rsinθ and y = rcosθ. For 2D potential, the tunneling path length is expressed as the length of an arc along an electric field line:

$$w_{tun} = r\theta_0 \tag{7}$$

where,

$$\theta_0 = \frac{\pi E_G}{2q\psi_G} \tag{8}$$

θ_0 is the angle between two equipotential lines whose potential difference is E_G/q. To get the total point tunneling current we must integrate the generated charge over the entire tunneling area:

$$I = qW\int_{r_0}^{\infty}\int_{\theta_0}^{\arccos(t'_{ox}/r)} G(r).r\,d\theta\,dr$$
$$I = qW\int_{r_0}^{\infty}\int_{\theta_0}^{\arccos(t'_{ox}/r)} A\frac{E_G^{D-1/2}}{q^D w_{tun}^D}\exp(-Bq\sqrt{E_G}\,w_{tun})\,r\,d\theta\,dr$$
$$= WA\int_{r_0}^{\infty}\int_{\theta_0}^{\arccos(t'_{ox}/r)} \frac{E_G^{D-1/2}}{q^{D-1} r^{D-1}\theta_0^D}\exp(-Bq\sqrt{E_G}\,r\theta_0)\,dr\,d\theta \tag{9}$$
$$\therefore I = WA\int_{r_0}^{\infty}\int_{\theta_0}^{\arccos(t'_{ox}/r)} \left(\arccos\left(t'_{ox}/r\right) - \theta_0\right)\frac{E_G^{D-1/2}}{q^{D-1} r^{D-1}\theta_0^D}\exp(-Bq\sqrt{E_G}\,r\theta_0)\,dr$$

where,

$\theta_0 = arccos(t'_{ox}/r_0)$

To solve Eq. (9) we perform first order Taylor expansion about $r = r_0$:

$$f(r_0) = \left(\arccos(t'_{ox}/r_0) - \theta_0\right)\frac{E_G^{D-1/2} e^{-Bq\sqrt{E_G}\,r_0\theta_0}}{q^{D-1} r_0^{D-1}\theta^D} \tag{10}$$

Putting the value of $f(r_0)$ and $f'(r_0)$ in the formula of Taylor expansion, and neglecting $\cos(\theta_0)$ w.r.t. unity we obtain:

$$f(r) = f(r_0) + f'(r_0)(r - r_0)$$

$$I \approx \frac{WAE_G^{D-1/2}}{q^{D-1} r_0^{D-1} \theta_0^{D}} \int_{r_0}^{\infty} \frac{t'_{ox}(r - r_0) e^{-Bq\sqrt{E_G} r \theta_0}}{r_0^2 \sqrt{1 - \left(\frac{t'_{ox}}{r_0}\right)^2}} dr$$

$$\approx \frac{WAE_G^{D-3/2} t'_{ox}}{q^{D-1} B^2} \cdot \frac{1}{\theta_0^{D+2} r_0^{D+1}} e^{-Bq\sqrt{E_G} r_0 \theta_0} \tag{11}$$

Approximating r_0 as a function of gate potential:

$$r_0 \approx t'_{ox} \frac{2q\psi_G}{\pi (q\psi_G - E_G)} \tag{12}$$

Hence, finally putting the value of θ_0 and the default values for Kane's model parameter D=2, we obtain an expression of current as:

$$I = WP \frac{q\psi_G}{E_G} \left(\frac{q\psi_G}{E_G} - 1 \right)^3 e^{Q / \left(\frac{q\psi_G}{E_G} - 1 \right)}$$

$$where,$$

$$P = \frac{2A\sqrt{E_G}}{\pi q^3 B^2 t'_{ox}}$$

$$Q = -Bq\sqrt{E_G} t'_{ox} \tag{13}$$

The total point tunneling current is twice the current in Eq. (13). as it is contributed both by the top gate and bottom gate of the DTG-CSC-TFET.

$$\therefore \left| I_{point} \right| = 2WP \frac{q\psi_G}{E_G} \left(\frac{q\psi_G}{E_G} - 1 \right)^3 e^{Q / \left(\frac{q\psi_G}{E_G} - 1 \right)} \tag{14}$$

It is assumed that line tunneling occurs along the entire the region of the channel that lies between source and gate. For the region $2(L_T+L_S)$, where the electrostatic potential is predominantly controlled by the gate, the effect of drain bias may be neglected to simplify the calculations. To this effect, we consider a one-dimensional potential profile in the semiconductor while considering line tunneling:

$$\psi(y) = \frac{qN_A}{2\varepsilon_S}(y - y_{max})^2$$
$$E(y) = -\frac{d\psi(y)}{dy} = -\frac{qN_A}{\varepsilon_S}(y - y_{max}) \tag{15}$$

where y_{max} is the length of the depletion region, which depends on the gate voltage, as shown in figure 4.3.

The tunneling width may be defined as the distance between the valence band and conduction band corresponding to equal energy level. The average electric field in y direction is:

$$E_{y,avg} = \frac{E_G}{qw_{tun}} \tag{16}$$

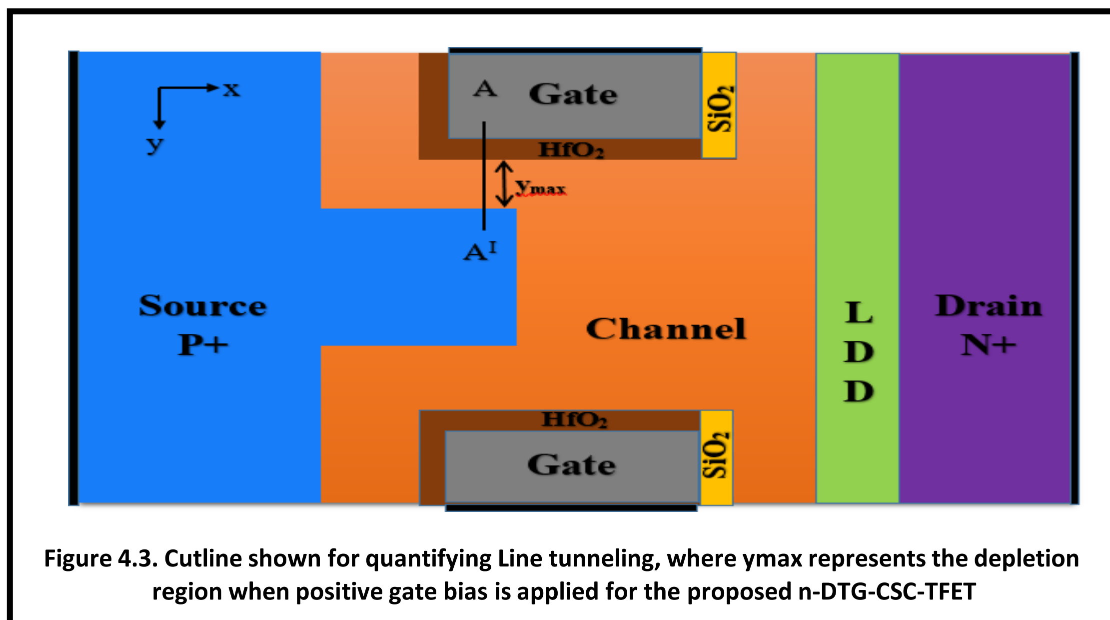


Figure 4.3. Cutline shown for quantifying Line tunneling, where ymax represents the depletion region when positive gate bias is applied for the proposed n-DTG-CSC-TFET

In order to calculate w_{tun} the y coordinates of the same potential in the valence band and conduction band are taken into consideration (as shown in Figure 4.4):

$$\psi_v(y_1) = \frac{qN_A}{2\varepsilon_S}(y_1 - y_{max})^2 + \frac{E_G}{q}$$
$$\psi_C(y_2) = \frac{qN_A}{2\varepsilon_S}(y_2 - y_{max})^2 \tag{17}$$

It can be deduced that:

$$w_{tun} = y_1 - y_2$$

$$\psi_v(y_1) = \psi_c(y_2)$$

Expressing y_2 as a function of w_{tun}:

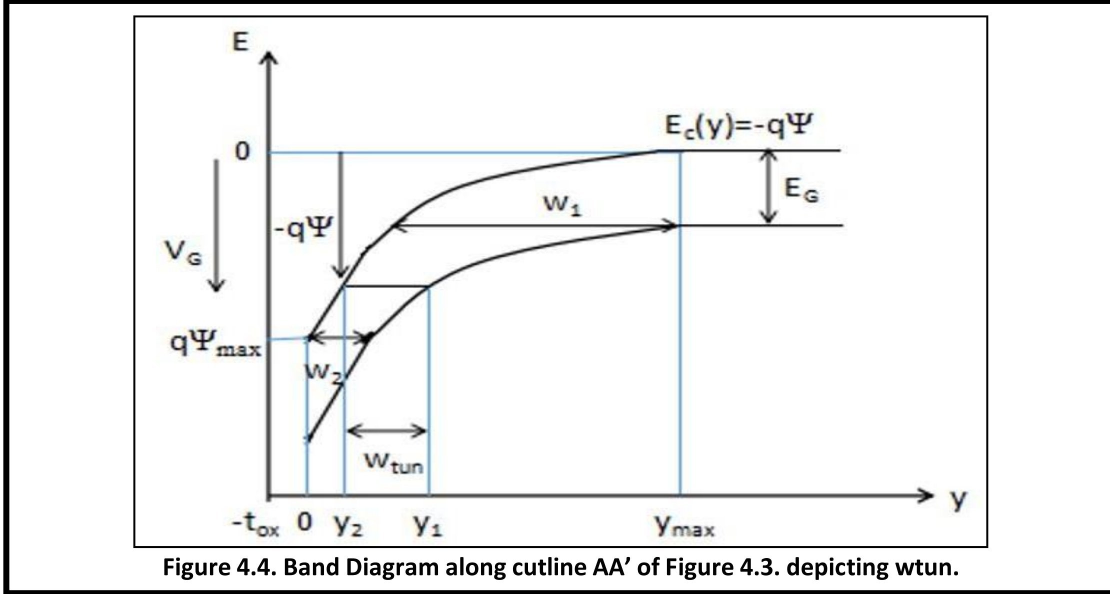


Figure 4.4. Band Diagram along cutline AA' of Figure 4.3. depicting wtun.

$$\therefore y_1 = w_{tun} + y_2$$

$$\frac{qN_A}{2\varepsilon_S}(y_1 - y_{max})^2 + \frac{E_G}{q} = \frac{qN_A}{2\varepsilon_S}(y_2 - y_{max})^2$$

$$\Rightarrow y_2 = y_{max} - \frac{1}{2}\,\frac{w_{tun}^2 + {2E_G\varepsilon_S}/{q^2 N_A}}{w_{tun}} \tag{18}$$

Differentiating Eq. (18) to obtain an expression for dy:

$$dy = -\frac{1}{2}\left[1 - \frac{2E_G\varepsilon_S}{q^2 N_A w_{tun}^2}\right] dw_{tun} \tag{19}$$

Combining Eq.(1), (3) and (19), we obtain:

$$|I| = qWL\int G\,dy$$

$$|I| = \frac{qWLA}{2}\int_{w_1}^{w_2}\frac{E_G^{D-1/2}}{q^D w_{tun}^D}\, e^{-Bq\sqrt{E_G w_{tun}}\left(1-\frac{q^2 N_A w_{tun}^2}{2E_G\varepsilon}\right)}\, dw_{tun} \tag{20}$$

In DTG-CSC-TFET total tunneling length $2(L_T+L_S)$.

$$\therefore |I_{line}| = qW\left(L_T+L_S\right)\int_{w_1}^{w_2}\frac{E_G^{D-1/2}}{q^D w_{tun}^D}\, e^{-Bq\sqrt{E_G w_{tun}}\left(1-\frac{q^2 N_A w_{tun}^2}{2E_G\varepsilon_S}\right)}\, dw_{tun} \tag{21}$$

Therefore, the total current expression is obtained from Eq. (14) and (21) as:

$$|I_{total}| = |I_{point}| + |I_{line}| \tag{22}$$

The current expression obtained in Eq. 22 is for the ON-current. The band-to-band tunneling at the channel-drain interface is not considered in the calculations as the applied gate bias is positive and as such tunneling distance between the channel valence band and the drain conduction band is very large. Hence, no tunneling occurs at the channel-drain interface under the given gate bias. The calculation of ambipolar current for negative gate bias has not been considered in this treatment.

4.5 Device Structure and Simulation Setup

The device dimensions and doping concentrations are highlighted in this section. The source is heavily doped P+ (1020 cm-3), the channel is lightly doped n-type (1012 cm-3), the LDD region is doped N (1017 cm-3) and the drain region has N+ doping (1019 cm-3). The oxide thickness tOX=2nm. The total lateral extent of the device is 74nm while the vertical extent is 60nm. The length of the source excluding the extended-source region is 20nm. The extended-source region length is denoted by LS, as previously mentioned. The tSi as denoted in figure 4.1 is 5nm. This value is optimum for studying quantum confinement effect. The vertical extent of the extended-source region is 20nm. The LDD and drain regions have lateral dimensions of 5nm and 15nm, respectively. It is evident that the structure is symmetrical about cutline 2. The width between the extended source and the gate is 8nm. The work function of the gate metal has been fixed at 4.85eV for the purpose of simulation. Device optimization has

been achieved by varying the value of L_S (10nm, 15nm, 20nm). The doping profiles of the three structural variants have been shown in figure 4.5.

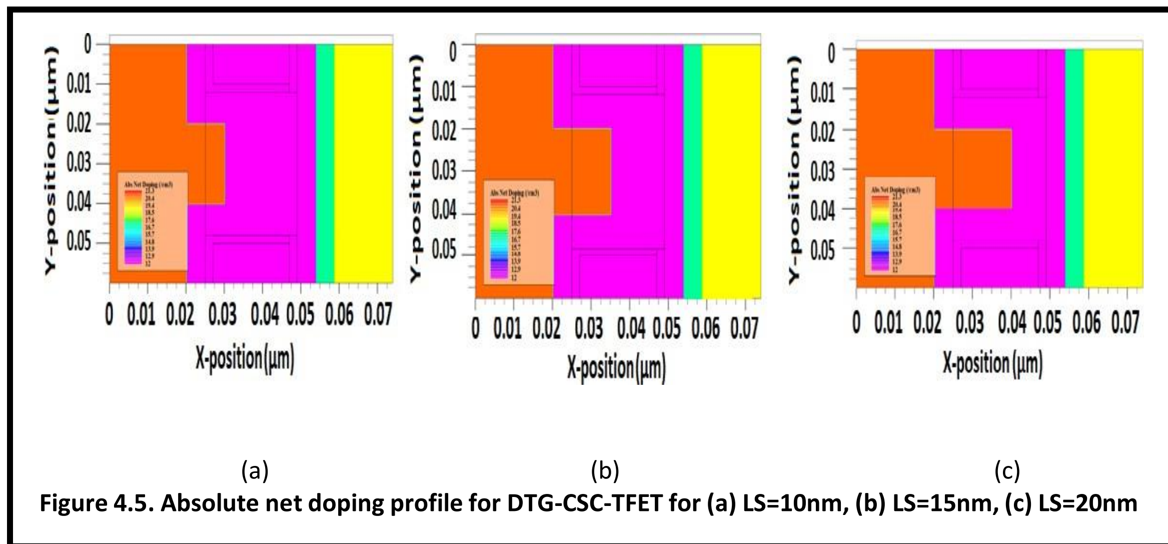


Figure 4.5. Absolute net doping profile for DTG-CSC-TFET for (a) LS=10nm, (b) LS=15nm, (c) LS=20nm

SILVACO ATLAS version 5.20.2.R was utilized to perform all the simulations. Appropriate mathematical models such as Lombardi Mobility Model, non-local BTBT model (BBT.NONLOCAL), Fermi Dirac Statistics, bandgap narrowing model, Auger and Shockley-Read Hall (SRH) recombination models and Drift diffusion carrier transport models were included to account for the underlying device physics of the proposed DTG-CSC-TFET. For the purpose of quantum simulations, the self-consistent Schrodinger-Poisson model has been used. This model accounts for the quantum mechanical effects under very low device dimensions.

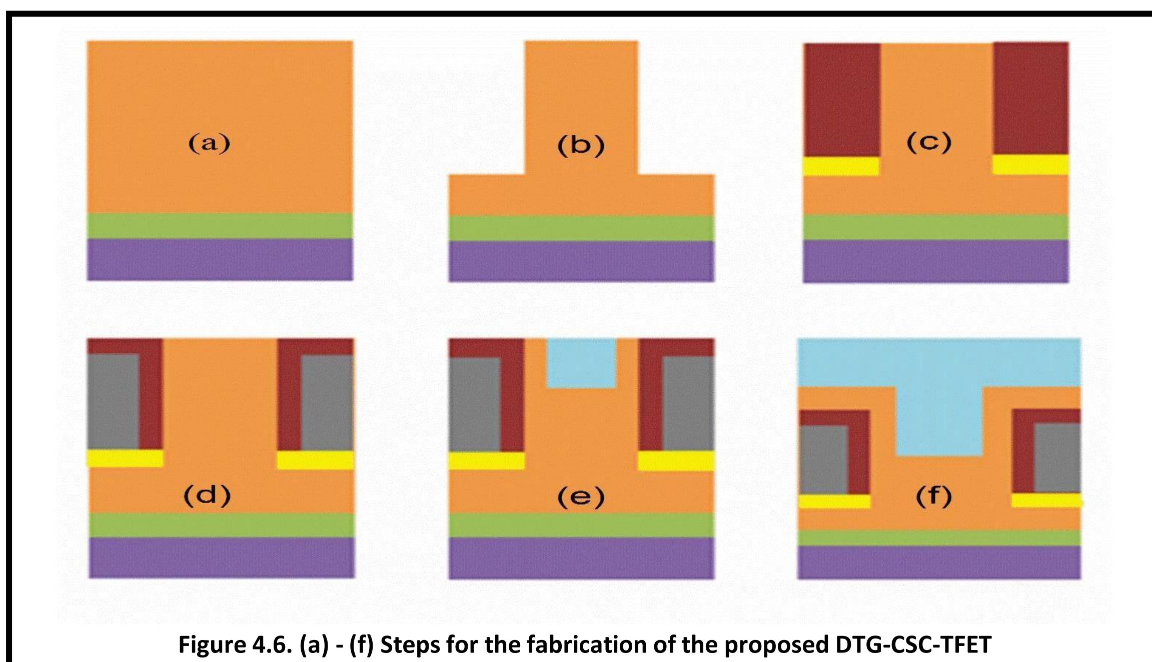


Figure 4.6. (a) - (f) Steps for the fabrication of the proposed DTG-CSC-TFET

Figure 4.6 summarizes the fabrication steps for the DTG-CSC-TFET. The N+ drain, LDD and n-substrate are grown epitaxially. Selective lateral etching is used to create pockets for developing the gate region of the double gate structure as shown in figure 4.6(b). This is followed by the lateral oxidation process. Firstly, SiO_2 layer is deposited by thermal oxidation. This is followed by the deposition of HfO_2 by the atomic layer deposition (ALD) process, as shown in figure 4.6(c). Dry plasma removal of HfO_2 is performed to create pockets for depositing the gate metal. This is followed by metallization to obtain the gate. A diffusion step is crucial to create the extended source region where the depth of diffusion can be controlled, as shown in figure 4.6(e). Subsequent expitaxial growth steps are instrumental to the development of the covered source-channel region and the P+ source region, as shown in figure 4.6(f).

4.6 Results and Discussion

4.6.1 Voltage Optimization

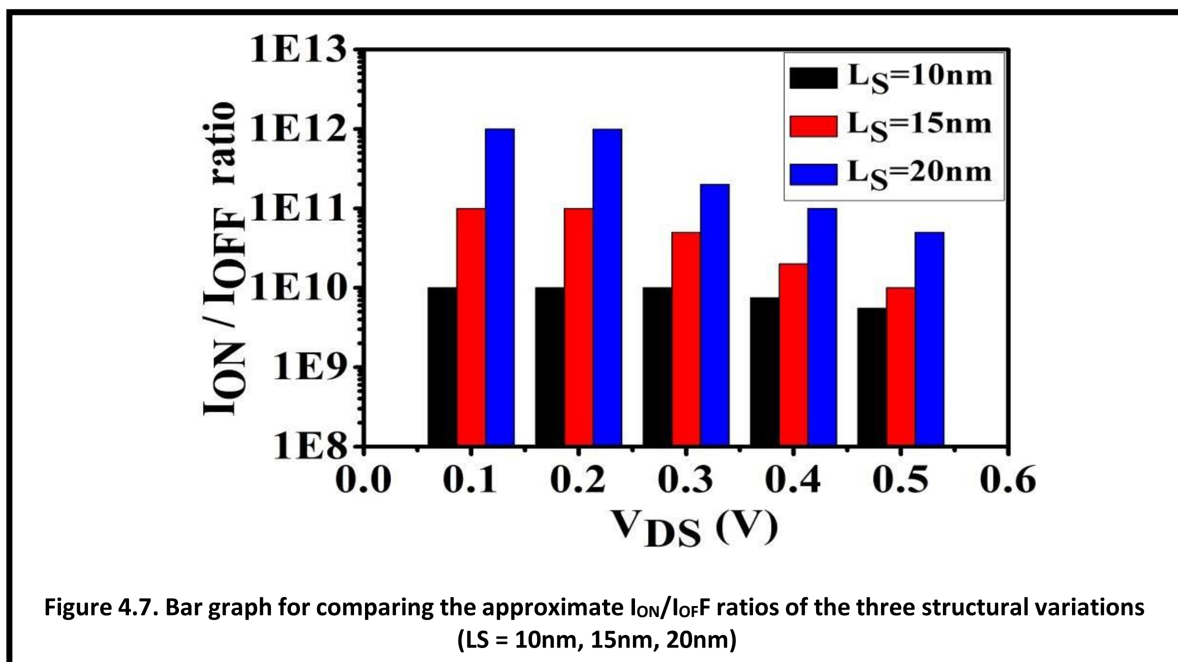


Figure 4.7. Bar graph for comparing the approximate $I_{ON}/I_{OF}F$ ratios of the three structural variations (LS = 10nm, 15nm, 20nm)

Voltage optimization was performed by comparing the subthreshold swing (SS), I_{ON}/I_{OFF} ratio and threshold voltage (V_{th}) for the proposed DTG-CSC-TFET for varying L_S (10nm, 15nm, 20nm) under five different values of drain voltage (V_{DS}). These calculations were performed on the Silvaco, Atlas software by use of appropriate codes as available in [4.20]. Ideally, subthreshold swing (SS) must be low, I_{ON}/I_{OFF} ratio must be high and the threshold voltage (V_{th}) must be low. Figure 4.7 shows a bar graph for comparing the I_{ON}/I_{OFF} ratio of the three

structural variations. It is seen that the device has similar I_{ON}/I_{OFF} ratio for V_{DS}=0.1V and V_{DS}=0.2V which is approximately 10^{12} for L_S = 20nm. Such high I_{ON}/I_{OFF} is obtained in the DTG-CSC-TFET due to the double gate configuration and the remarkably high tunneling area that results in increased ON-current. It is also worth noting that I_{ON}/I_{OFF} ratio is, in general, higher for L_S=20nm than for L_S=10nm and L_S=15nm. This is discussed in details in the forthcoming sections.

Figure 4.8(a) shows a bar graph for comparing the subthreshold swing (SS) for varying L_S (10nm, 15nm, 20nm) under five different values of the drain voltage (V_{DS}). We know that lower subthreshold swing value is preferred under the prescripts of device miniaturization. The lowest values of SS is obtained at V_{DS}=0.1V for L_S = 20nm, with the lowest recorded value of 22 mV/decade for L_S=20nm.

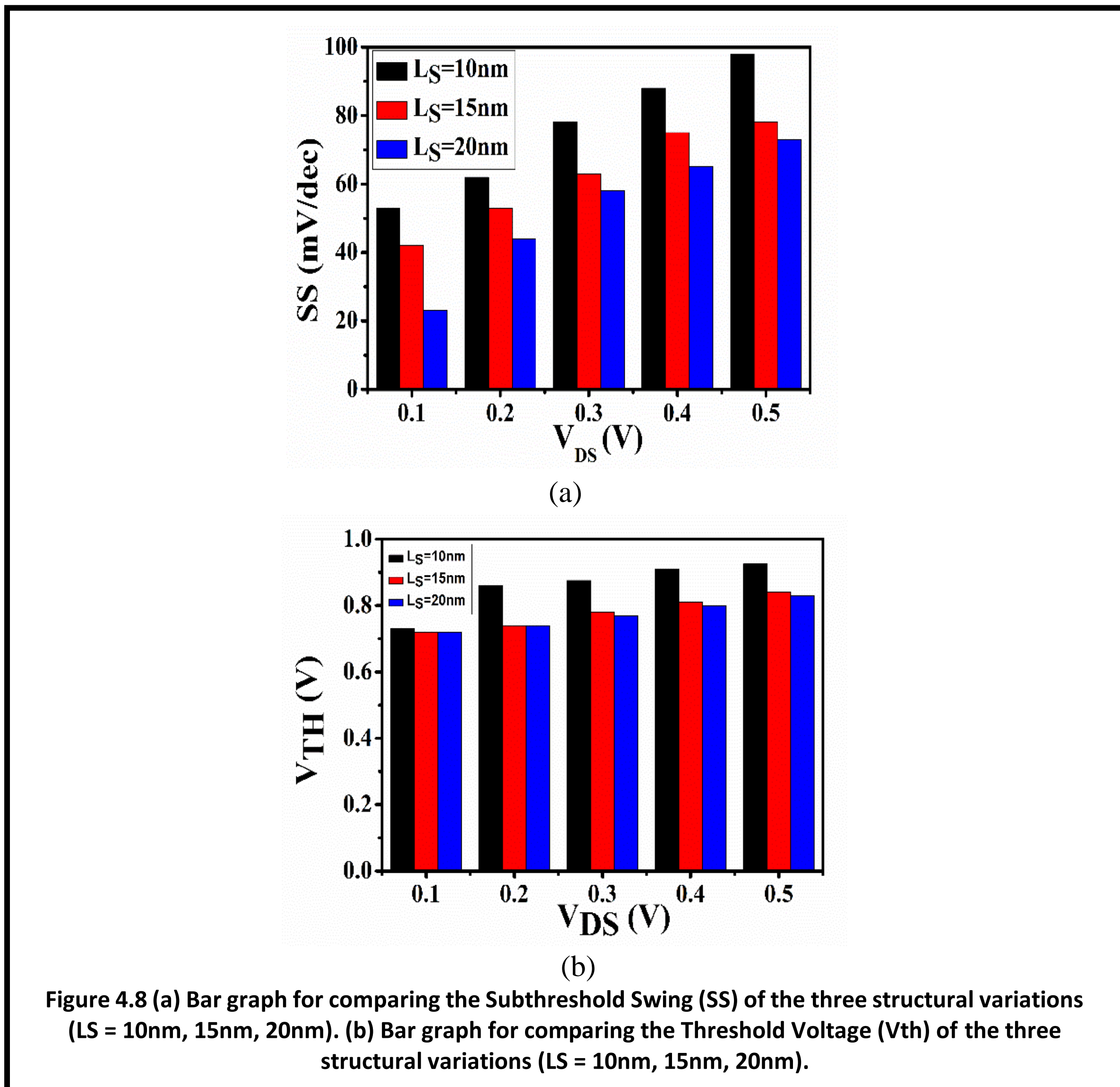


Figure 4.8 (a) Bar graph for comparing the Subthreshold Swing (SS) of the three structural variations (LS = 10nm, 15nm, 20nm). (b) Bar graph for comparing the Threshold Voltage (Vth) of the three structural variations (LS = 10nm, 15nm, 20nm).

Figure 4.8(b) shows a bar graph for the comparison of threshold voltage (V_{th}). It can be observed that the lowest recorded threshold voltage value is obtained for V_{DS}=0.1V for Ls=20nm. It can be concluded from the figure 4.7, and figure 4.8(a) and 4.8(b) that the drain voltage V_{DS}=0.1V is the most optimized value for the proposed structure. Such low values of drain voltage agree well with the results presented in [4.21]. Hence, this device is best suited for low power applications. All further simulations presented in this chapter have been performed for V_{DS}=0.1V.

4.6.2 Variation of Extended Source Length L_s

4.6.2.1 Energy Band Diagrams

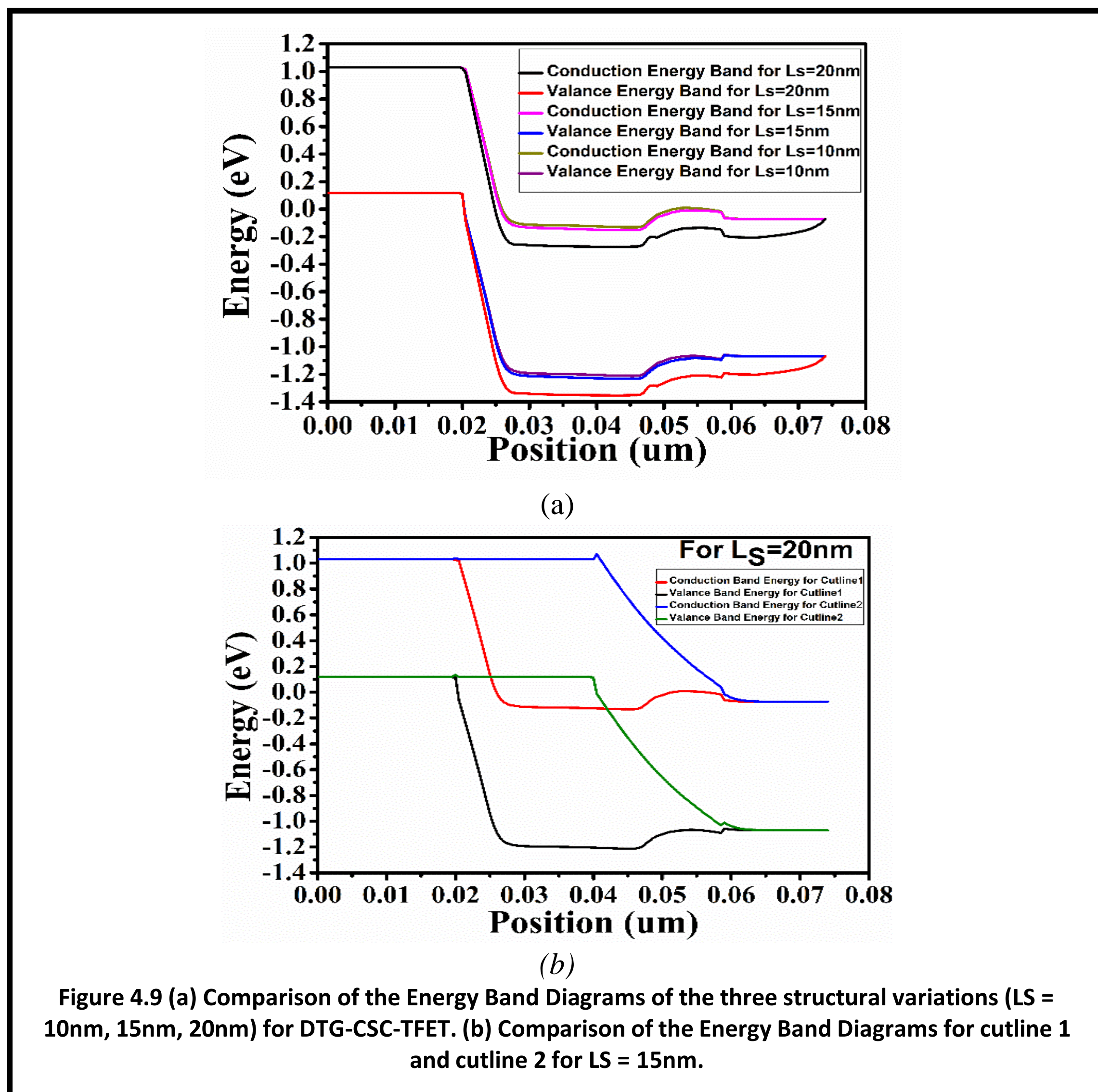


Figure 4.9 (a) Comparison of the Energy Band Diagrams of the three structural variations (LS = 10nm, 15nm, 20nm) for DTG-CSC-TFET. (b) Comparison of the Energy Band Diagrams for cutline 1 and cutline 2 for LS = 15nm.

The energy band diagrams have been plotted for the DTG-CSC-TFET for L_S=10nm, L_S=15nm and L_S=20nm under ON-state at cutline 1. It is known that tunneling probability is

inverse exponentially related to the tunneling length. From figure 4.9(a) it is evident that the least tunneling length occurs for L_S=20nm. Hence, the tunneling probability is highest in this case. The slightly bent energy band characteristics at the drain end is due to LDD and as such is responsible for reduced ambipolar conduction for the proposed structure. Figure 4.9(b) shows the comparison of the energy band diagrams for cutline 1 and cutline 2. It is seen that the tunneling probability is higher in case of cutline 1 than for cutline 2. The cutline 2 passes through the middle of the extended source region and hence, the source-channel interface is well ahead along the x-axis to that in case of cutline 1. This difference in tunneling probabilities is evident from figure 4.10 which shows the contour diagram of the BTBT rates for cutline 1 and cutline 2.

It has been previously assumed that line tunneling occurs for a total length of $2(L_T+L_S)$. Hence, this value is indicative of the band-to-band tunneling area. In order to validate this assumption, three different values of L_S have been taken as L_S=10nm, L_S=15nm and L_S=20nm. The effect of this structural variation on the energy band diagram, electric field, potential and transfer characteristics have been compared in this section. Also, the aforementioned parameters have been compared for two different cutlines that were shown in figure 4.10. The transfer characteristics obtained from the analytical model has been compared with the simulation results.

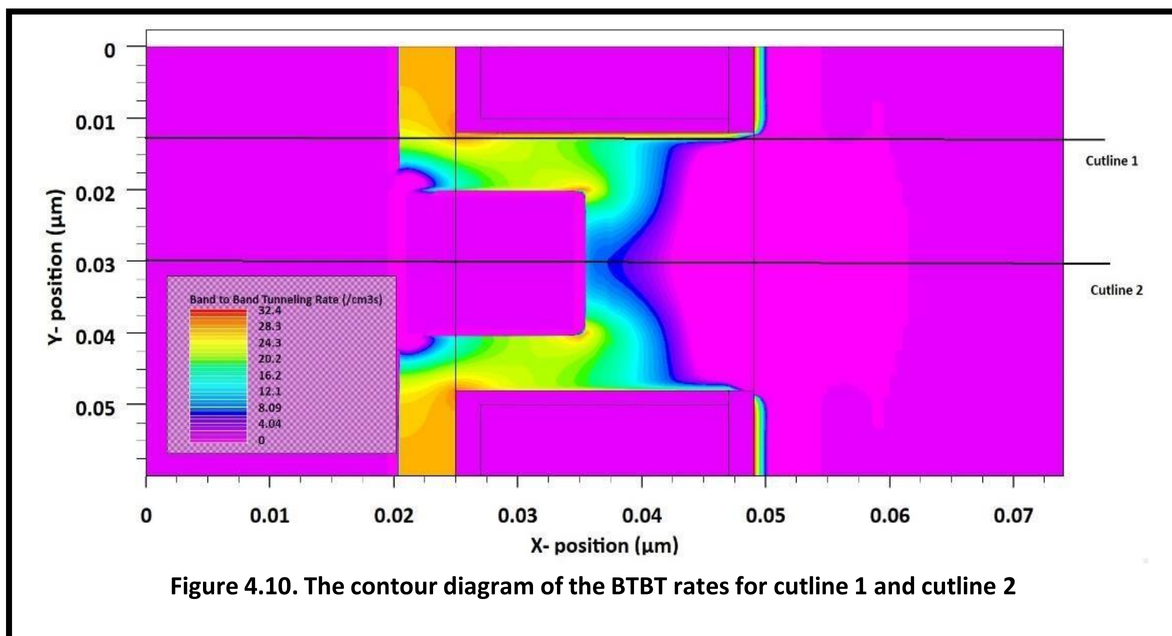


Figure 4.10. The contour diagram of the BTBT rates for cutline 1 and cutline 2

4.6.2.2 Electric Field

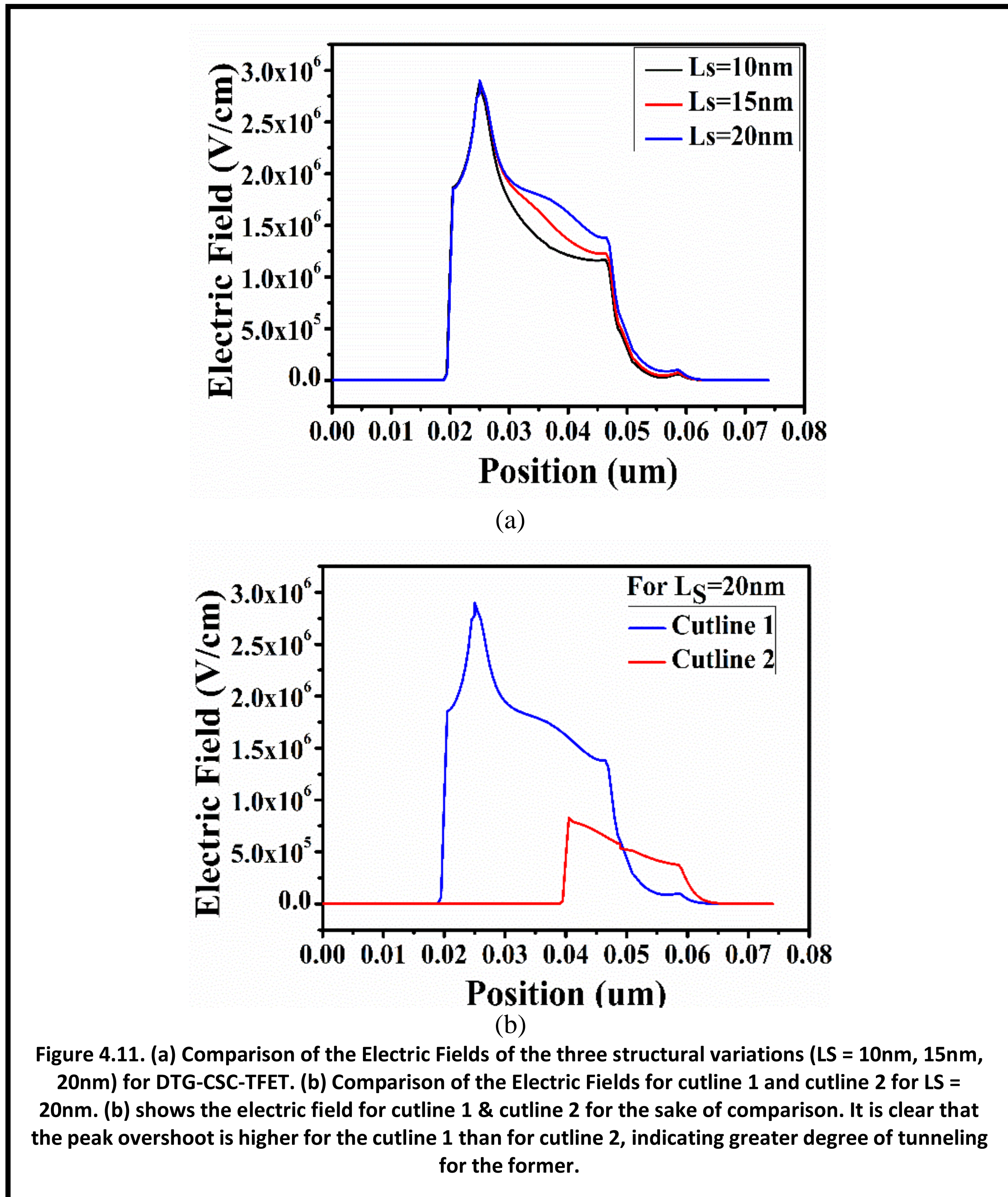


Figure 4.11. (a) Comparison of the Electric Fields of the three structural variations (LS = 10nm, 15nm, 20nm) for DTG-CSC-TFET. (b) Comparison of the Electric Fields for cutline 1 and cutline 2 for LS = 20nm. (b) shows the electric field for cutline 1 & cutline 2 for the sake of comparison. It is clear that the peak overshoot is higher for the cutline 1 than for cutline 2, indicating greater degree of tunneling for the former.

The peak overshoot in the electric field at the source-channel interface is an indicative of the extent of tunneling. The electric field is compared for all the three structural variations at cutline1 in figure 4.11. The highest peak is observed for L_S=20nm at the source channel junction for cutline1. The electric field characteristic remains high for a considerable channel length owing to the covered-source configuration of the DTG-CSC-TFET. The presence of a peak at the channel drain interface indicates suppressed reverse ambipolar tunneling. This peak

also suggests the impact of DIBL effect. It is seen that the electric field peak is slightly higher for L_S=10nm at the channel drain interface as compared to the other two variations suggesting lower DIBL effect for this structure. The electric field at the source channel junction is much higher than that at the channel-drain junction suggesting reduced hot carrier effect in the proposed device.

4.6.2.3 Potential profile

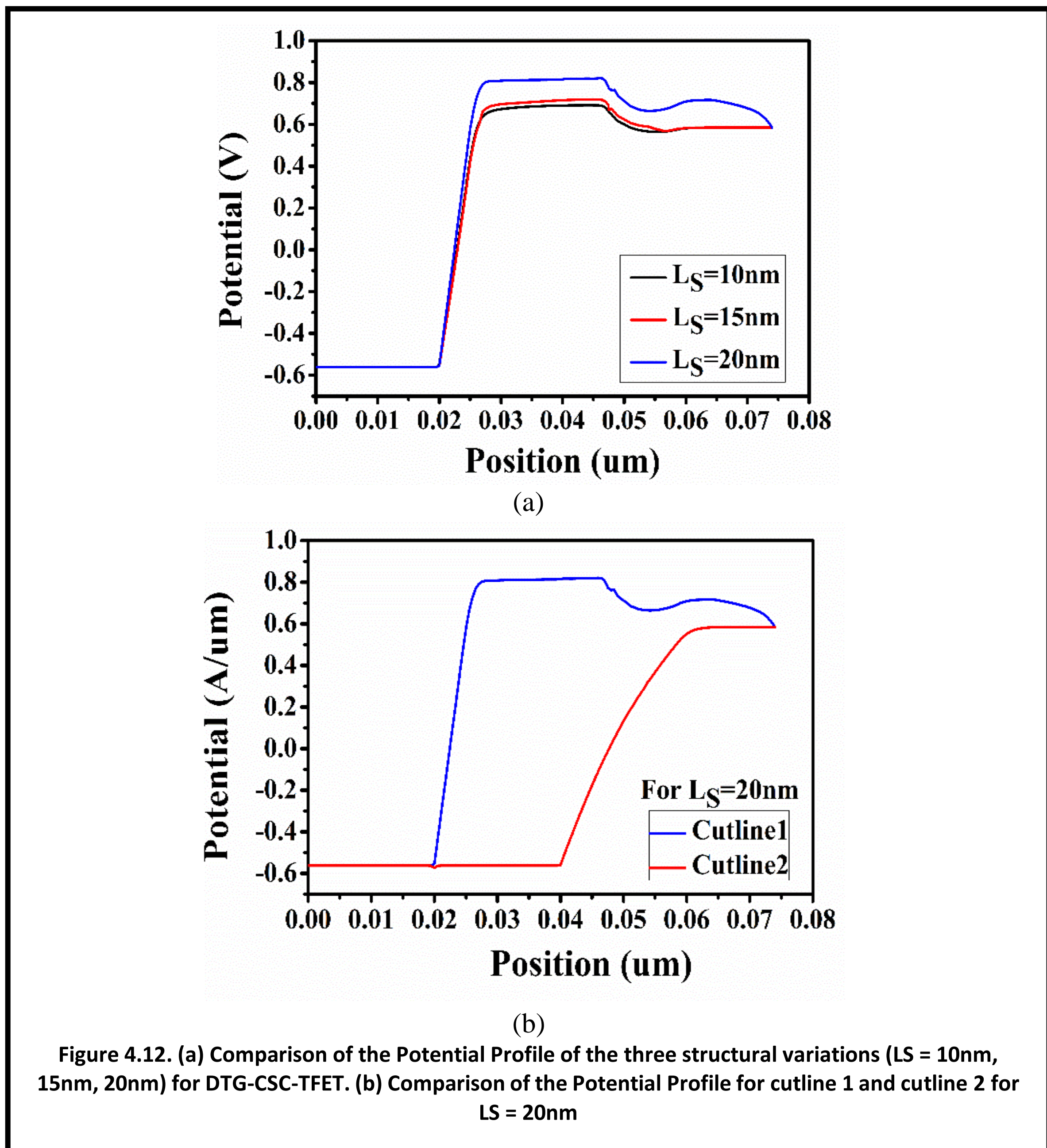


Figure 4.12. (a) Comparison of the Potential Profile of the three structural variations (LS = 10nm, 15nm, 20nm) for DTG-CSC-TFET. (b) Comparison of the Potential Profile for cutline 1 and cutline 2 for LS = 20nm

The peak in potential profile at the source channel junction gives a measure of the overall tunneling. It can be observed form figure 4.12(a) that the overall tunneling is highest for L_S=20nm. Moreover, greater value of potential at the channel drain junction suggests that the

electrons which tunnel at the source channel interface effectively reach the drain end. This is the case for L_S=20nm. figure 4.12(b) compares the potential profiles for cutline 1 and cutline 2 for L_S=20nm. It is seen that the potential value is higher for cutline 1 than for cutline 2 suggesting lower extent of overall tunneling at the cutline 2. This agrees well with the observations from figure 4.11(b).

4.6.3 Transfer Characteristics

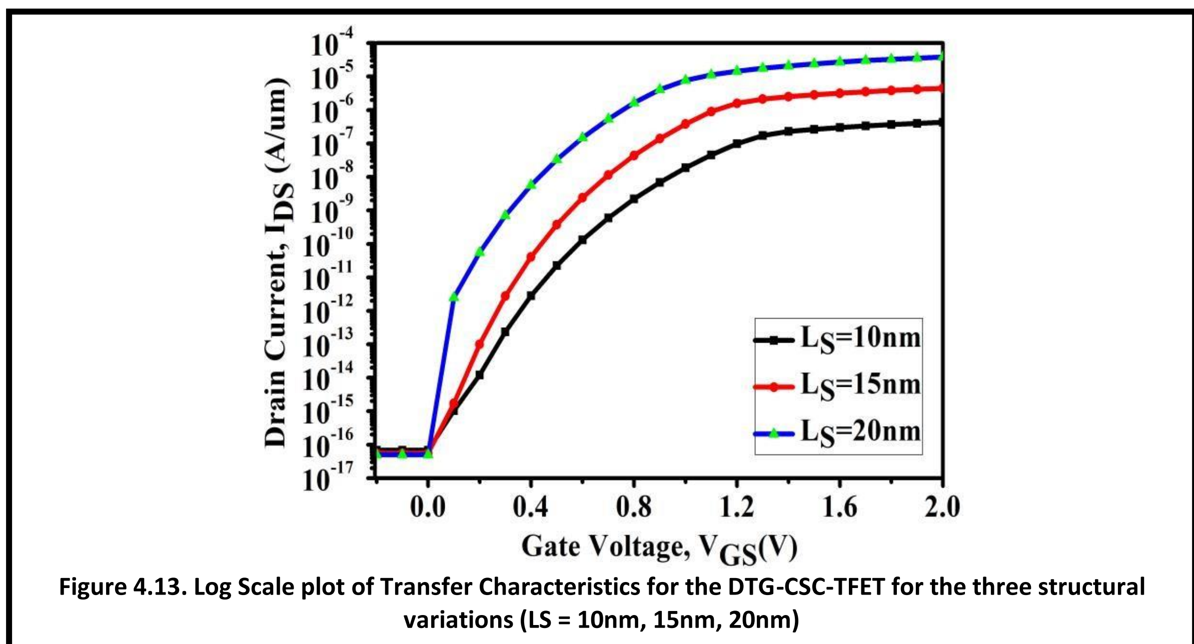


Figure 4.13. Log Scale plot of Transfer Characteristics for the DTG-CSC-TFET for the three structural variations (LS = 10nm, 15nm, 20nm)

Figure 4.13 shows the linear plot of I_{DS}-V_{GS} transfer characteristics for the different values of L_S (10nm, 15nm, 20nm). It is seen that as L_S increases, more BTBT occurs due enhanced tunneling area. This results in higher I_{ON} because the extended portion is where line tunneling occurs. Figure 4.13 shows the log transfer characteristics. It is evident that the subthreshold swing (SS) is 22mV/decade for L_S=20nm, 41mV/decade for L_S=15nm and 52mV/decade for L_S=10nm.

Furthermore, as was evident from figure 4.8(b) the threshold voltage (V_{th}) decreases with an increase in L_S as the BTBT electrons are generated at lower values of gate voltage. From all the analysis presented, it can hence be concluded that L_S=20nm is the most optimized structural variant.

Figure 4.14. shows a comparison between the transfer characteristics depicting the curve for ON-current as obtained from simulation and analytical modelling for the most optimized structural variant L_S = 20nm. The two curves agree well with one another, thus validating the proposed model.

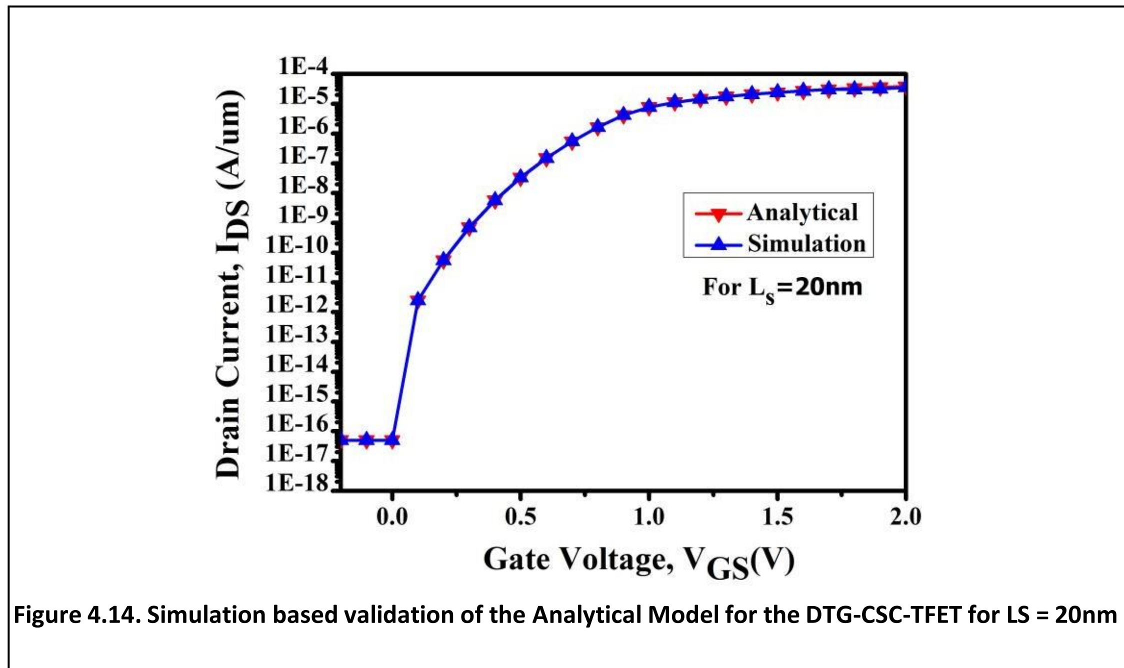


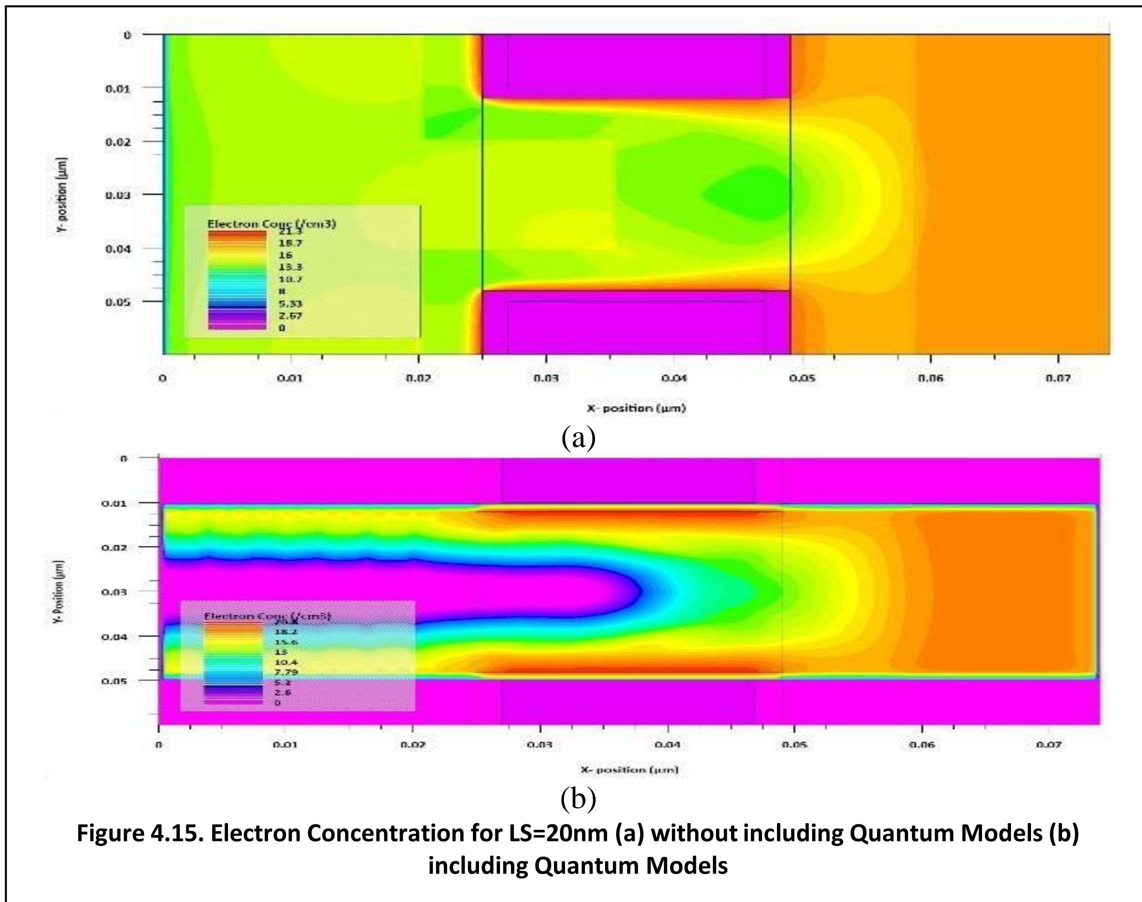
Figure 4.14. Simulation based validation of the Analytical Model for the DTG-CSC-TFET for LS = 20nm

4.6.4 Quantum Confinement Effect

Owing to extensive scaling, in the present nanodevice scenario, a phenomenon, known as quantum confinement effect (QCE) has become more pronounced. In this phenomenon, the energy band structure is altered under the influence of ultra-low length scale. For group IV, II-V and II-VI, the length scale between 1 to 5 nm corresponds to the pronounced quantum confinement regime. Such low dimensions impose geometrical constraints on the electrons. In particular, as the particle size approaches the Bohr exciton radii, the QCE becomes more pronounced. Thus, in QCE the continuous energy bands of the bulk material collapse into discrete energy levels. The QCE in the proposed DTG-CSC-TFET was visualized by employing the self-consistent Schrödinger-Poisson (SP) model on Silvaco, Atlas. This was necessary as the t_{Si} of the proposed structure is 5nm. Due to energy band discretization, the conduction band-valence band overlap region gets significantly reduced at the source channel junction resulting in greater tunneling length. This reduces the extent of BTBT significantly.

Figure 4.15 shows a comparison between the electron concentration for L_S=20nm with and without considering QCE. Carrier confinement is clearly seen in figure 4.15(b) where negligible carriers are present along the channel region with thickness t_{Si}. It is also seen that a confined region just below the gate oxide has very high electron concentration. As a direct result of this, the transfer characteristics with and without consideration of quantum confinement effect is different, with poor SS and reduced ON-current in case of the QCE consideration. The comparison in transfer characteristics is shown in figure 4.16 for L_S=20nm.

Where ambipolar current is significantly high when quantum confinement is included be attributed by the combined effect (1) the discrete set of energy band in the conduction and valance band due to quantum confinement and (2) the high electron concentration in the confined region just below the gate oxide [4.36] [4.37]. Further, the oversimplified model deployed here is also a reason for such variation as depicted in figure 4.16.



(a)

(b)

Figure 4.15. Electron Concentration for LS=20nm (a) without including Quantum Models (b) including Quantum Models

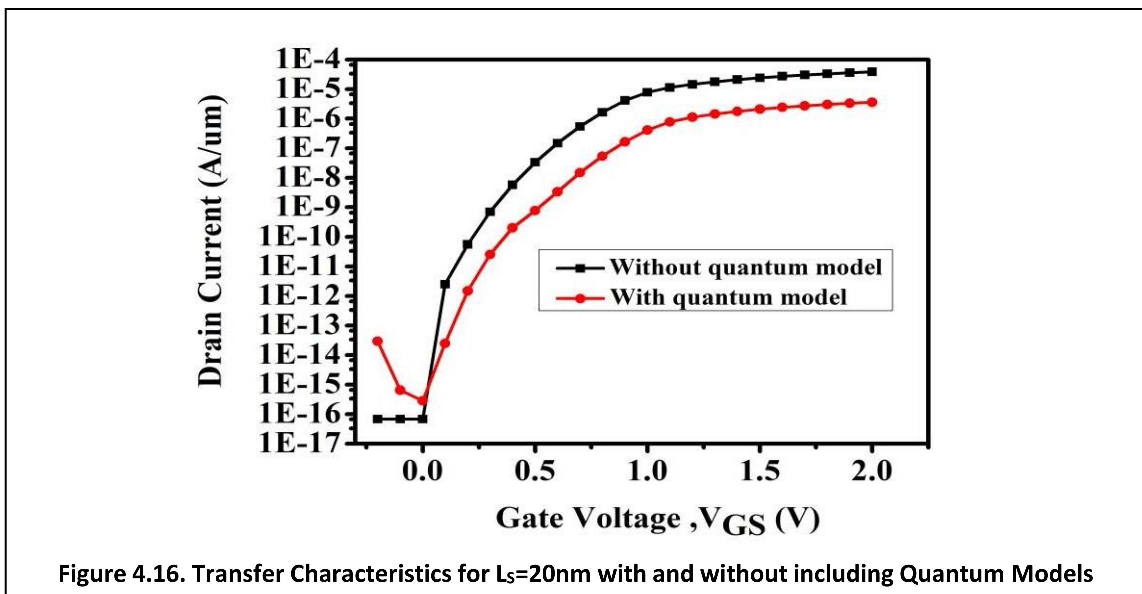


Figure 4.16. Transfer Characteristics for L_S=20nm with and without including Quantum Models

4.7 DTG-CSC-TFET Inverter

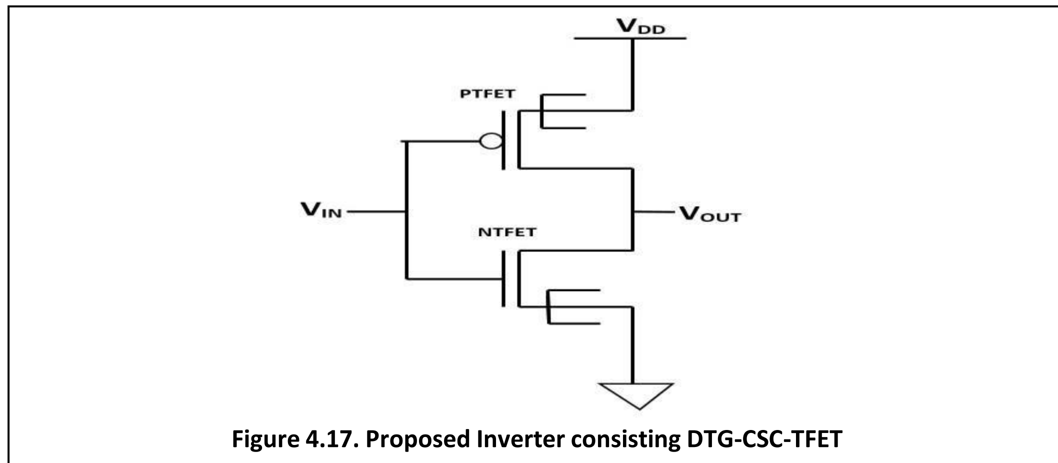


Figure 4.17. Proposed Inverter consisting DTG-CSC-TFET

(a)

(b)

Figure 4.18. (a) VTC of the DTG-CSC-TFET inverter with supply voltage (VDD) from 0.2 V to 0.5 V. (b) voltage gain of the DTG-CSC-TFET inverter under various VDD, showing high gain even at VDD = 0.2 V.

The schematic of the inverter is shown in figure 4.17. Figure 4.18(a) shows the proposed inverter has better gain at V_{DD}=0.2V [4.23-4.24] because of larger ION and suppressed ambipolarity and follow ideality. When the electric field increases the gate lies in the linear region and when the gate moves in the saturation or in the deep saturation region and that leads to degradation of mobility of the carriers and degrades the performance of the device and deviates from ideality. When the V_{DD} is more, the depletion capacitance at the drain side is expected to be more, and that gives rise to increase rise time and fall time. That leads to non-ideality with the variation of V_{DD}. The simulated VTC shows that the transition voltage of the inverter is located around $V_{DD}/2$ and a clearly separation between the high and the low levels, indicating both devices are working properly. High voltage gains (V_{OUT}/V_{IN}) is also achieved as shown in figure 4.18(b) at lower V_{DD}=0.2V. A voltage gain as high as 24 is obtained, demonstrating high potential for future low power applications. In order to estimate the noise margin, figure 4.18(a) shows the VTCs of the proposed TFET inverter at V_{DD}=0.2V.

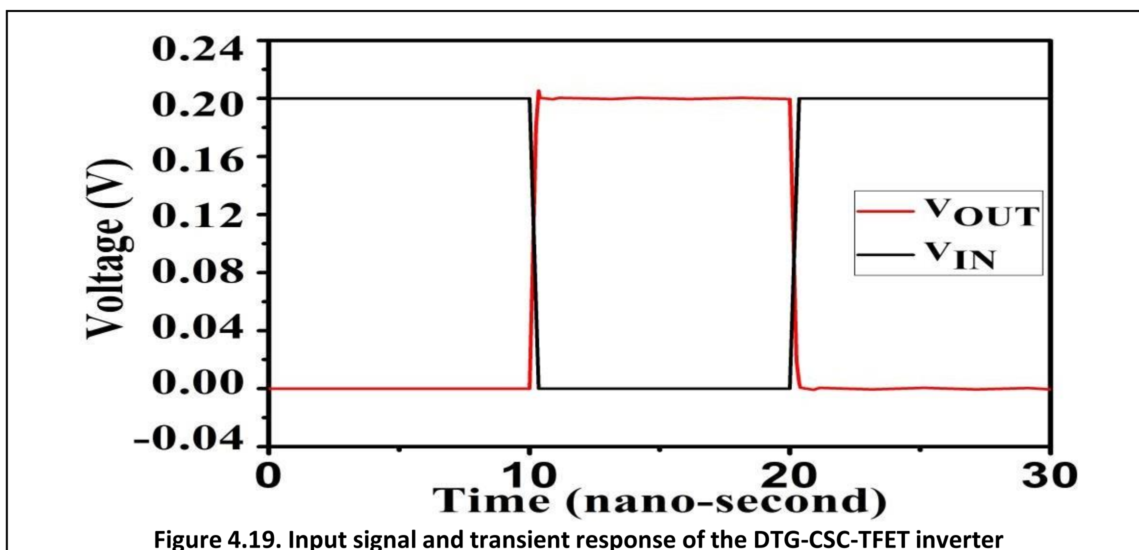


Figure 4.19. Input signal and transient response of the DTG-CSC-TFET inverter

Parameters	DC value in Voltage	Compared TFET [22]
V_{IL}	94.31mV	0.42 V
V_{OL}	4.99 mV	0
V_{OH}	194 mV	0.59 V
V_{IH}	105.75 mV	1 V
$NM_L=V_{IL}-V_{OL}$	89.32 mV	42
$NM_H= V_{OH}-V_{IH}$	88.25 mV	41
Delay time	19.6 ps	26.76 ps
Rise time	20.81 ps	46.21 ps
Fall time	20.68ps	46.20 ps
Power Dissipation	41.45nW	92 nW

Table 4.1: Different DC parameters of the proposed inverter at Vdd=0.2 volt

Table I represents the different DC parameters related to VTC. Figure 4.19 shows the transient behavior of DTG-CSC-TFET inverters simulated for a peak-to-peak voltage of 0.2 V for 30 ns without considering any load capacitance. Figure 4.19 shows that overshoot in output voltage occurs when the input voltage makes a transition from high to low. The output overshoot voltage is slightly higher in the DTG-CSC-TFET due to enhanced Miller capacitance. Table I. justifies that the proposed DTG-CSC-TFET inverter has a promising future for low-power digital applications.

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Chapter:5

CHAPTER – 5: To Study the Impact of Source Pocket Doping in PNPN-DG TFET

5.1 Introduction 136
5.2 Literature Review 138
5.3 Incorporation of Centrally Aligned Source Pocket Region in TFET: 2D- Modeling and Simulation-Based Performance Assessment 140
5.3.1 Device Structure of a CA-PNPN-DG TFET 140
5.3.2 Analytical Model 141
5.3.3 Results and Discussions 146
5.3.3.1 Potential Distribution 146
5.3.3.2 Electric Field Distribution 148
5.3.3.3 Conduction Band and Valence Band Energy. 149
5.3.3.4 Transfer Characteristics 150
5.4. Incorporation of two symmetric pockets at Source Region in TFET: 2D- Modeling and Simulation-Based Performance Assessment 150
5.4.1 Device Structure of a TB-PNPN-DG TFET 150
5.4.2 Analytical Model 151
5.4.3 Results and Discussions 155
5.4.3.1 Potential Distribution 155
5.4.3.2 Electric Field Distribution 157
5.4.3.3 Conduction Band and Valence Band Energy 158
5.4.3.4 Transfer Characteristics 159
5.5 Comparison 159
5.6 Frequency Analysis 160
5.7 Circuit Design 162
References 164

5.1 Introduction

In the feature dimension of conventional MOSFET scaling below sub-60 nm technology, the MOSFET faces limitations in fabrication process due to short channel effects (SCEs), lowering the barrier due to drain bias and subthreshold swing, which enhances the power consumption and degraded the performance of MOS-device. For the last few years, the

researchers worked rigorously on theoretical and experimental to shift to alternative device designs and architectures which can improve the performance, and overcome the major issue related to MOSFET scaling limitations without changing the manufacturing setup. Several techniques such as silicon-on-insulator (SOIs), nanowire devices, and FinFETs devices are used to improve device performance. However, this device engineering encourages parasitic resistance and enhances the process complexity. Further, the drift-diffusion current of the device is the main difficulty that essentially confines scaling supply voltage and power dissipation. Tunnel Field Effect Transistor (TFET), a non-conventional device with almost similar geometry, has emerged in the research lime limelight possible successor for bulk MOSFET. Tunnel FET working on the principle of band-to-band tunneling mechanism through a barrier instead of modulating thermionic emission over a barrier as in traditional MOSFETs, has come up as a promising candidate with the advantages of going below the limit of 60mV/decade sub-threshold slope, yielding higher I_{ON}/I_{OFF} at lower V_{DD}, lower leakage current, and thus capable of reducing the power consumption, and achieving energy-efficient fast switching transistors having a basic constrain is its low I_{ON}. The basic TFET architecture is that of a reverse-biased gated p-i-n diode. Various design optimizations and modifications have been done since its inception to enhance the performance of TFET to make it a competing technology for future technology nodes. However, the low I_{ON} of TFET, originating because of the large tunneling resistance at the tunneling junction, limits its application in high-speed integrated circuits. One of the techniques reported in this regard is creating heavily doped pocket implantation between the source and the channel region. Pocket doped is also known to be as p-n-p-n TFET is a promising TFET architecture because of its advantage of steep band bending and thus reduction of barrier width. It enhances the electric field at the tunneling junction and thus results in a steep subthreshold slope, better ON-state current, reduced tunneling voltage drop, and improved reliability compared to the conventional p-i-n TFET. To fully gain the aforementioned electrical characteristics from the source-pocket PNPN TFET, ideally, the size of the pocket should be very narrow and the doping level should be high. The steepness of doping transition from one type to the other is also a key parameter. This transition slope depends on the fabrication process and determines the net-doped transition distance. This net-doped transition distance controls the tunneling width and therefore, should be less than the N+ pocket length to maintain the promised performance. Fulfilling the above requirements of realizing a narrow N+ pocket in a PNPN TFET is a technological challenge.

5.2 Literature Review

THE improvement of the performance of the devices is achieved by scaling of the device size, modification of device structure with new material incorporation, and structure varieties. MOSFET structures have their limitation over the betterment of performance due to the short channel effects and therefore researchers opted for TFET devices which contributes to the new ways of developing advanced device structures. The TFET devices are capable of achieving a lower SS of less than 60mV/decade than MOSFET due to the BTBT mechanism that leads to a higher I_{on}/I_{off} ratio. There have been several experimental and simulation studies justify in the direction to the development of a compact analytical model and working principles for TFET. Some of the current research in this direction is as follows

Kathy et al [5.1] propose and validate a DG-TFET, which improves performence to single-gate devices having high-gate dielectric. DG-TFET, achieves I_{ON} /I_{OFF} ratio of more than 10^{11}. The 2D current flow nature demonstrated that the current is not confined to the channel at the gate-dielectric surface. When varying temperature, TFETs with a high-k gate dielectric have a smaller V_{th} shift than those using SiO_2, while the SS for fixed values of V_{gs} remains nearly unchanged.

The research groups led by Sarkar et al [3.17, 3.18] have worked on Double gate FET models consisting of two gates, one at the top and the other at the bottom. This configuration improves the electrostatic control of the gate on the channel allowing the field lines from the gate to terminate at the back gate rather than terminating in the channel. The impact is well reflected as magnified ON-state current compared to single gate counterpart, since there are two channels available to support flow of current in the device.

Chun-Hsing et al [5.2] present a sub-10-nm TFET with bandgap engineering using a graded Si/Ge heterojunction. In the on-state tunneling barrier around the source was narrowed resulting in high I_{ON} and in the off-state tunneling barrier was raised controlling the SEC and ambipolar $I_{Leakage}$.

Lattanzio et al [5.3] simulated a Ge-EHBTFET which exploits carrier tunneling through a bias-induced electron-hole bilayer. Ge EHBTFET has low operating voltage, due to its super-steep SS, higher I_{ON}/I_{OFF} ratio, and drive current I_{ON}.

Mallik et al [5.4] reported the analog performance of a double-gate n-type TFET with a relatively small body thickness of 10 nm, and showed high I_{ds}.

Rui et al [5.5] demonstrated an AlGaSb/InAs TFET employs a staggered heterojunction with the tunneling direction oriented in line with the gate field. with an on-current of 78 μA/μm at 0.5 V.

Bagga et al [5.6] proposed an analytical model of GAA-TM-TFET that justifies three different metals over the channel region to form a barrier in the channel. The choice of three metals with different work functions helps to increase the I_{ON} and also reduces the I_{OFF}.

Further, Dey et al [3.21] paid attention to an SOI-based device to investigate the electrical characteristics. The entire thin silicon layer is depleted and the drain-body and source-body depletion regions are kept small. It is reported the buried oxide layer blocks all the source-to-drain leakage paths through the bulk region providing better gate control over the channel. This also leads to a smaller source/drain to substrate capacitance.

SON, an innovative SOI version enables the fabrication of extremely thin silicon (5 to 20 nm) and buried dielectric (10 to 30 nm) offering quasi-total suppression of SCEs with excellent electrical performances [3.22]. In a SON device, the buried oxide of simple SOI structure is replaced with air and it has been proven theoretically and experimentally that with the air-gap, the SCEs of the conventional SOI structures can be reduced [3.23-3.24]. SON MOSFET is an improved SOI structure which is widely discussed as a lucrative scalable solution to satisfy the ITRS Roadmap requirements [3.25].

Jaya et al [5.7] incorporated a gate-drain overlap engineering scheme over the cylindrical gate all around TFET (GAA-TFET) to suppress ambipolar current. However, to enhance the ON current, incorporated hetero-gate dielectrics are used in the gate oxide region.

Chen et al [5.8] explained the energy efficiency of TFET. From the perspective of circuit energy efficiency for TFET devices, a source doping gradient variation provides helpful design guidelines.

Mohammadi et al [5.9] by considering the junctions depletion regions and the channel mobile charge carriers proposed an analytical model for DG-TFETs for important quantities in TFETs, such as lateral electric field, minimum tunneling length, and I_{DS}.

Ritesh et al [5.10] simulate and fabricated p-i-n and source-pocket TFETs with different pocket conditions to observe the effect of pocket doping as well as the annealing schemes on the source-pocket TFET.

Mohata et al [5.11] experimentally demonstrate a staggered-source and N+ pocket-doped Channel III-V TFET, 100% enhancement in I_{ON} over, In0.53Ga0.47 as n-channel homojunction TFET by replacing In0.53Ga0.47.

S. H Kim [5.12] proposed and investigated Germanium-source TFET as a logic switch that can achieve steeper switching characteristics than MOSFET. Here it has been experimentally demonstrated that Ge-source TFET performed better than CMOS, showing greater than 10x improvement in the overall energy efficiency for a higher frequency range due to operating at lower V_{th} and V_{DD}.

Gholizadeh et al [5.13] proposed an analytical model for DG-TFETs which is validated by comparing it with the simulated results for different sets of parameters. The analytical model predicts the effects of gate oxide thickness, body thickness, gate oxide dielectric, and channel length, on-device characteristics which allows us to gain insight into the device operation.

Kosala et al [5.14] proposed a compact model to calculate the inner and outer fringe capacitances of a gate to source/drain underlapped double-gate (DG)-MOSFET in the sub-threshold condition. This model includes the varying electric field in the underlap region derived using the conformal mapping technique, along with the non-abrupt S/D body junctions resulting in effective underlapping.

5.3 Incorporation of Centrally Aligned Source Pocket Region in TFET: 2D- Modeling and Simulation-Based Performance Assessment

5.3.1 Device Structure of a CA-PNPN-DG TFET

The 2-D cross-sectional perspective on the p-channel TFET structures with absolute net doping profile is given in figure 5.1 utilizing Silvaco Atlas. The structure contains a centrally aligned Source Pocket region that is absent in a traditional TFET. This is a heavily doped region. The specific doping concentration of the TFET models is the P^+ type source region (1×10^{20} cm^{-3}), P channel region (1×10^{12} cm^{-3}), N^+ type Drain region (1×10^{18} cm^{-3}), and the N^+ Pocket region (1×10^{19} cm^{-3}), which are kept constant for all the simulations. Such doping fixations create a tunneling junction between source and channel where the phenomenon of interband tunneling can happen.

The simulated device has a total length of 46nm and a vertical dimension of 49nm. The gate length is varied to 24nm, 14nm, and 7nm. But the effective channel length is examined to be 22nm. The lateral and the vertical dimensions for both the Source and Drain regions are 10nm and 43nm, respectively. The Pocket Region has lateral and vertical dimensions of 2nm and 25nm respectively. The dielectric used for the gate electrode is Hafnium Oxide which has a thickness of t_{ox} = 2nm and the dielectric constant is approx 40.

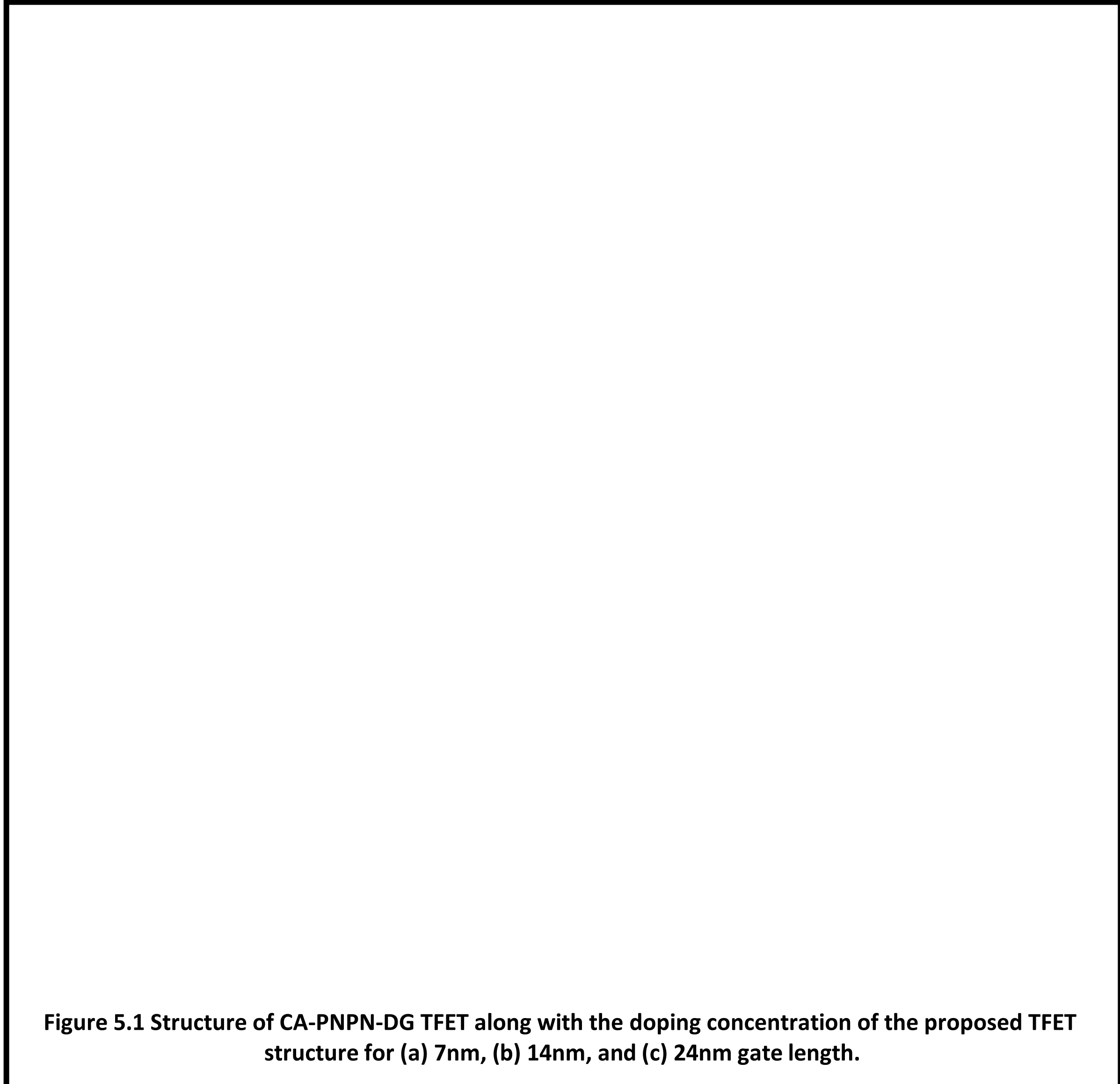


Figure 5.1 Structure of CA-PNPN-DG TFET along with the doping concentration of the proposed TFET structure for (a) 7nm, (b) 14nm, and (c) 24nm gate length.

5.3.2 Analytical Model

The analytical modeling of the surface potential has been verified with the simulated results.

Surface Potential

2-D Poisson's equation is used to administer the surface potential of the proposed structure which is given by

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=-\frac{qN_{cn}}{\varepsilon_{si}} \quad (1)$$

Where $0 \le x \le L$ and $0 \le y \le t_{si}$

Here is the doping concentration at the channel region and the channel length L is divided into three regions. Thus, the total length L = L1+L2+L3. The surface potential profile has been approximated using the parabolic polynomial function such as

$$\phi(x, y) = \phi_s(x) + C_1(x) y + C_2(x) y^2 \quad (2)$$

Where C1 and C2 are arbitrary functions of x and $\phi_s(x)$ is surface potential. As the channel is divided into three regions of the aforementioned length therefore the surface potential under different regions as considered here can be represented in the following way

$$\phi_j(x, y) = \phi_{sj}(x) + C_{j1}(x) y + C_{j2}(x) y^2 \quad (3)$$

for $L_{j-1} \le x \le L_j$, $0 \le y \le t_{si}$ and j=1,2 ,3.

The surface potential can be achieved by solving Poisson's equations with the application of the boundary conditions as follows.

The electric field is continuous at y=0 that is for the front–gate oxide interface which leads to the three expressions corresponding to three regions below:

$$\left.\frac{d\phi_1(x, y)}{dx}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s1}(x) - V_{GS1}}{t_f} \quad (4)$$

$$\left.\frac{d\phi_2(x, y)}{dx}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s2}(x) - V_{GS1}}{t_f} \quad (5)$$

$$\left.\frac{d\phi_3(x, y)}{dx}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s3}(x) - V_{GS1}}{t_f} \quad (6)$$

Here $V_{GS1} = V_{GS} - V_{FB,L1}$ and $V_{FB,L1} = \phi_{MS1} = \phi_M - \phi_{si}$ where $V_{FB,L1}$ is the flat band potential, ϕ_M and ϕ_{si} are the metal and silicon work functions respectively. Also, $\phi_{si} = \chi + \frac{E_g}{2q} + \phi_B$ where

χ is electron affinity, E_g is bandgap of silicon, ϕ_B is built-in potential and is given by $\phi_B = V_T \ln \frac{N_{cn}}{n_i}$.

The electric field is continuous at $y=t_{si}$ that is for the back–gate oxide interface which leads to the three expressions corresponding to three regions below:

$$\left.\frac{d\phi_1(x,y)}{dx}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V'_{GS,b1} - \phi_{B1}(x)}{t_b} \quad (7)$$

$$\left.\frac{d\phi_2(x,y)}{dx}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V'_{GS,b1} - \phi_{B2}(x)}{t_b} \quad (8)$$

$$\left.\frac{d\phi_3(x,y)}{dx}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V'_{GS,b1} - \phi_{B3}(x)}{t_b} \quad (9)$$

where $V'_{GS1,b} = V_{GS} - V_{FB,L1}$

Using these three boundary conditions mentioned above solution for the arbitrary functions of the parabolic approximation are found to be

$$C_{11}(x) = \frac{\varepsilon_{ox}}{\varepsilon^{si}} \frac{\phi_{s1}(x) - V_{GS1}}{t_f} \quad (10)$$

$$C_{21}(x) = \frac{\varepsilon_{ox}}{\varepsilon^{si}} \frac{\phi_{s2}(x) - V_{GS1}}{t_f} \quad (11)$$

$$C_{31}(x) = \frac{\varepsilon_{ox}}{\varepsilon^{si}} \frac{\phi_{s3}(x) - V_{GS1}}{t_f} \quad (12)$$

$$C_{12}(x) = \frac{1}{2C_{si}t_{si}^2}\left[C_b(V'_{GS,b1} - \phi_{B1}(x)) - C_f(\phi_{s1}(x) - V_{GS1})\right] \quad (13)$$

$$C_{22}(x) = \frac{1}{2C_{si}t_{si}^2}\left[C_b(V'_{GS,b1} - \phi_{B2}(x)) - C_f(\phi_{s2}(x) - V_{GS1})\right] \quad (14)$$

$$C_{32}(x) = \frac{1}{2C_{si}t_{si}^2}\left[C_b(V'_{GS,b1} - \phi_{B3}(x)) - C_f(\phi_{s3}(x) - V_{GS1})\right] \quad (15)$$

The values of these constants are put into (2) and solving for (1), the surface potential is achieved in the following format corresponding to the three regions considered in the structure,

$$\frac{\partial^2 \phi_{s1}(x)}{\partial x^2} - \alpha \phi_{s1}(x) = \beta_1 \tag{16}$$

$$\frac{\partial^2 \phi_{s2}(x)}{\partial x^2} - \alpha \phi_{s2}(x) = \beta_2 \tag{17}$$

$$\frac{\partial^2 \phi_{s3}(x)}{\partial x^2} - \alpha_3 \phi_{s3}(x) = \beta_3 \tag{18}$$

where α, α_3, β_1, β_2 and β_3 are given by:

$$\alpha = \frac{2C_f}{C_{si} t_{si}^2 \left(1 + \frac{C_{ox}}{C_{si}} - \frac{C_f}{C_{si}}\right)} \tag{19}$$

$$\beta_1 = \left[-\frac{qN_{cn}}{\varepsilon_{si}} - \frac{2V_{GS1}C_f}{C_{si} t_{si}^2}\right]\left[\frac{1}{1 + \frac{C_{ox}}{C_{si}} - \frac{C_f}{C_{si}}}\right] \tag{20}$$

$$\beta_2 = \left[-\frac{qN_{cn}}{\varepsilon_{si}} - \frac{2V_{GS1}C_f}{C_{si} t_{si}^2}\right]\left[\frac{1}{1 + \frac{C_{ox}}{C_{si}} - \frac{C_f}{C_{si}}}\right] = \beta_1 \tag{21}$$

$$\alpha_3 = \frac{2C'_f}{C_{si} t_{si}^2 \left(1 + \frac{C_{ox}}{C_{si}} - \frac{C'_f}{C_{si}}\right)} \tag{22}$$

and $$\beta_3 = \left[-\frac{qN_{cn}}{\varepsilon_{si}} - \frac{2V_{GS1}C'_f}{C_{si} t_{si}^2}\right]\left[\frac{1}{1 + \frac{C_{ox}}{C_{si}} - \frac{C'_f}{C_{si}}}\right] \tag{23}$$

Where $c_f^{'} = c_{if} + c_{of}$ and the values of inner fringing capacitance (C_{if}) and outer fringing capacitance (C_{of}) are taken from [14].

Solving those three differential equations i.e. (15), (16) and (17) using C.F. and P.I. and combining the two, solution for surface potential of the three regions are found such as

$$\phi_{s1}(x) = Ae^{\sqrt{\alpha}x} + Be^{-\sqrt{\alpha}x} - \frac{\beta_1}{\alpha} \tag{24}$$

$$\phi_{s2}(x) = Ce^{\sqrt{\alpha}(x-L1)} + De^{-\sqrt{\alpha}(x-L1)} - \frac{\beta_2}{\alpha} \tag{25}$$

$$\phi_{s3}(x) = Ee^{\sqrt{\alpha}(x-L1-L2)} + Fe^{-\sqrt{\alpha}(x-L1-L2)} - \frac{\beta_3}{\alpha_3} \tag{26}$$

where the values of the constants A, B , C, D , E and F are found to be :

$$A = \frac{\beta_1\left(e^{\sqrt{\alpha}L_1}-1\right)}{\alpha\left(e^{2\sqrt{\alpha}L_1}-1\right)} + \frac{\left[V_{bi}\left(e^{\sqrt{\alpha}L_1}-1\right) + (V_{ds}(\frac{L_2}{L})+V_{bi})e^{\sqrt{\alpha}L_1}\right]}{\left(e^{2\sqrt{\alpha}L_1}-1\right)} \tag{27}$$

$$B = \frac{\beta_1 e^{\sqrt{\alpha}L_1}\left(e^{\sqrt{\alpha}L_1}-1\right)}{\alpha\left(e^{2\sqrt{\alpha}L_1}-1\right)} + \frac{e^{\sqrt{\alpha}L_1}\left[V_{bi}\left(e^{\sqrt{\alpha}L_1}-1\right)+(V_{ds}(\frac{L_2}{L})+V_{bi})\right]}{\left(e^{2\sqrt{\alpha}L_1}-1\right)} \tag{28}$$

$$C = \frac{\beta_2\left(e^{\sqrt{\alpha}L_2}-1\right)}{\alpha\left(e^{2\sqrt{\alpha}L_2}-1\right)} + \frac{\left[(V_{ds}(\frac{L_2}{L})+V_{bi})\left(e^{\sqrt{\alpha}L_2}-1\right)+(V_{ds}(\frac{L_3}{L})+V_{bi})e^{\sqrt{\alpha}L_2}\right]}{\left(e^{2\sqrt{\alpha}L_2}-1\right)} \tag{29}$$

$$D = \frac{\beta_2 e^{\sqrt{\alpha}L_2}\left(e^{\sqrt{\alpha}L_2}-1\right)}{\alpha\left(e^{2\sqrt{\alpha}L_2}-1\right)} + \frac{e^{\sqrt{\alpha}L_2}\left[(V_{ds}(\frac{L_2}{L})+V_{bi})\left(e^{\sqrt{\alpha}L_2}-1\right)+(V_{ds}(\frac{L_3}{L})+V_{bi})\right]}{\left(e^{2\sqrt{\alpha}L_2}-1\right)} \tag{30}$$

$$E = \frac{\beta_3\left(e^{\sqrt{\alpha_3}L_3}-1\right)}{\alpha_3\left(e^{2\sqrt{\alpha_3}L_3}-1\right)} + \frac{\left[(V_{ds}(\frac{L_3}{L})+V_{bi})\left(e^{\sqrt{\alpha_3}L_3}-1\right)+(V_{ds}+V_{bi})e^{\sqrt{\alpha_3}L_3}\right]}{\left(e^{2\sqrt{\alpha_3}L_3}-1\right)} \tag{31}$$

$$F = \frac{\beta_3 e^{\sqrt{\alpha_3}L_3}\left(e^{\sqrt{\alpha_3}L_3}-1\right)}{\alpha_3\left(e^{2\sqrt{\alpha_3}L_3}-1\right)} + \frac{e^{\sqrt{\alpha_3}L_3}\left[(V_{ds}(\frac{L_2}{L})+V_{bi})\left(e^{\sqrt{\alpha_3}L_3}-1\right)+(V_{ds}(\frac{L_3}{L})+V_{bi})\right]}{\left(e^{2\sqrt{\alpha_3}L_3}-1\right)} \tag{32}$$

Where , L_1, L_2 and L_3 are considered as

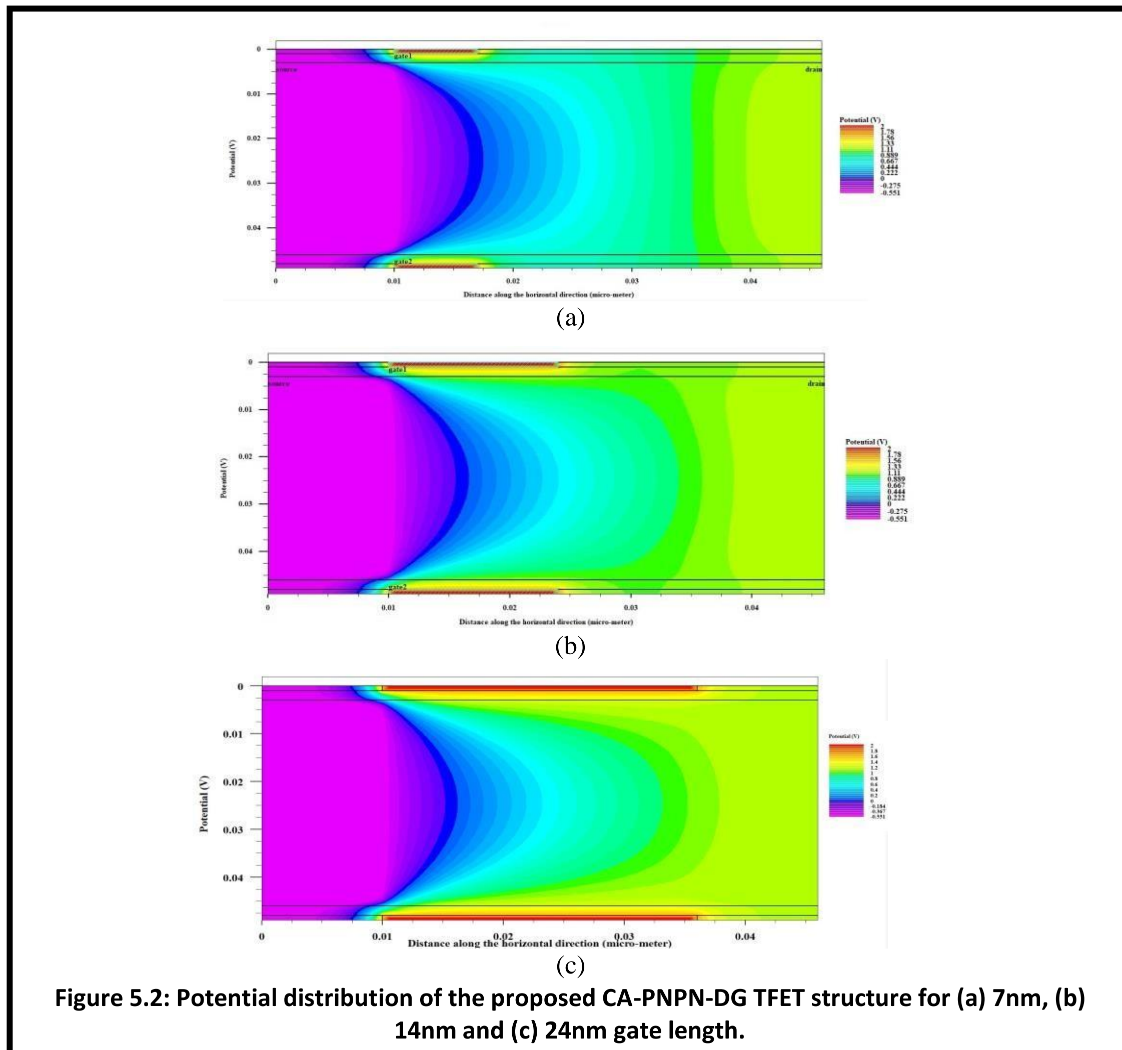
$$L_1 = l_p$$
$$L_2 = l_g - l_p$$
$$L_3 = L - l_g - l_p$$

and l_p, l_g are defined as the length of the source pocket region and gate respectively.

5.3.3 Results and Discussions

Endeavours are made for simulation predicated validation studies of the proposed contrivance structures. The simulation results along with visual graphical plots of potential profiles, electric field, electron current, hole current, total current etc. for different gate lengths of the structure are portrayed in this section.

5.3.3.1 Potential Distribution

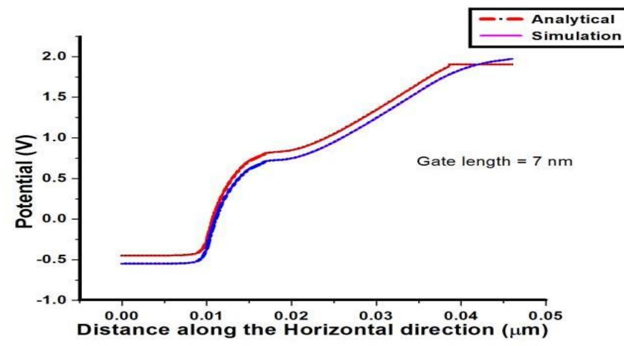


(a)

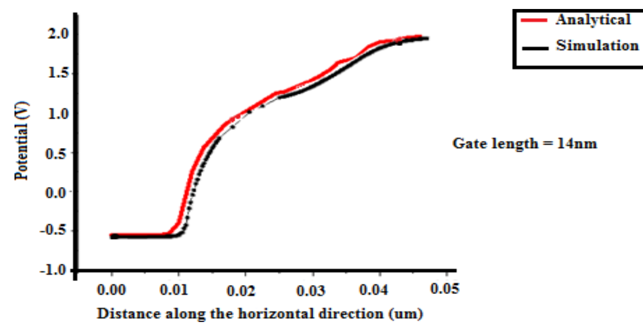
(b)

(c)

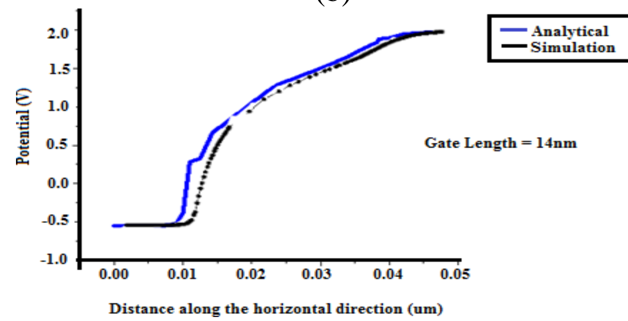
Figure 5.2: Potential distribution of the proposed CA-PNPN-DG TFET structure for (a) 7nm, (b) 14nm and (c) 24nm gate length.



(a)



(b)



(c)

Figure 5.3. Comparison of analytical result of the surface potential distribution and simulation outcome for (a)7nm, (b) 14nm and (c) 24nm gate length.

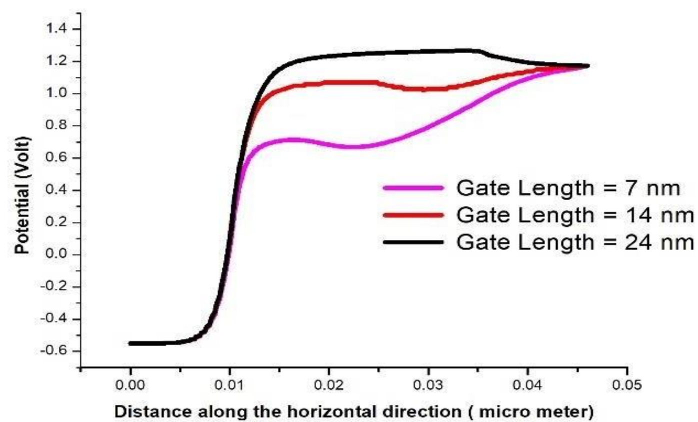
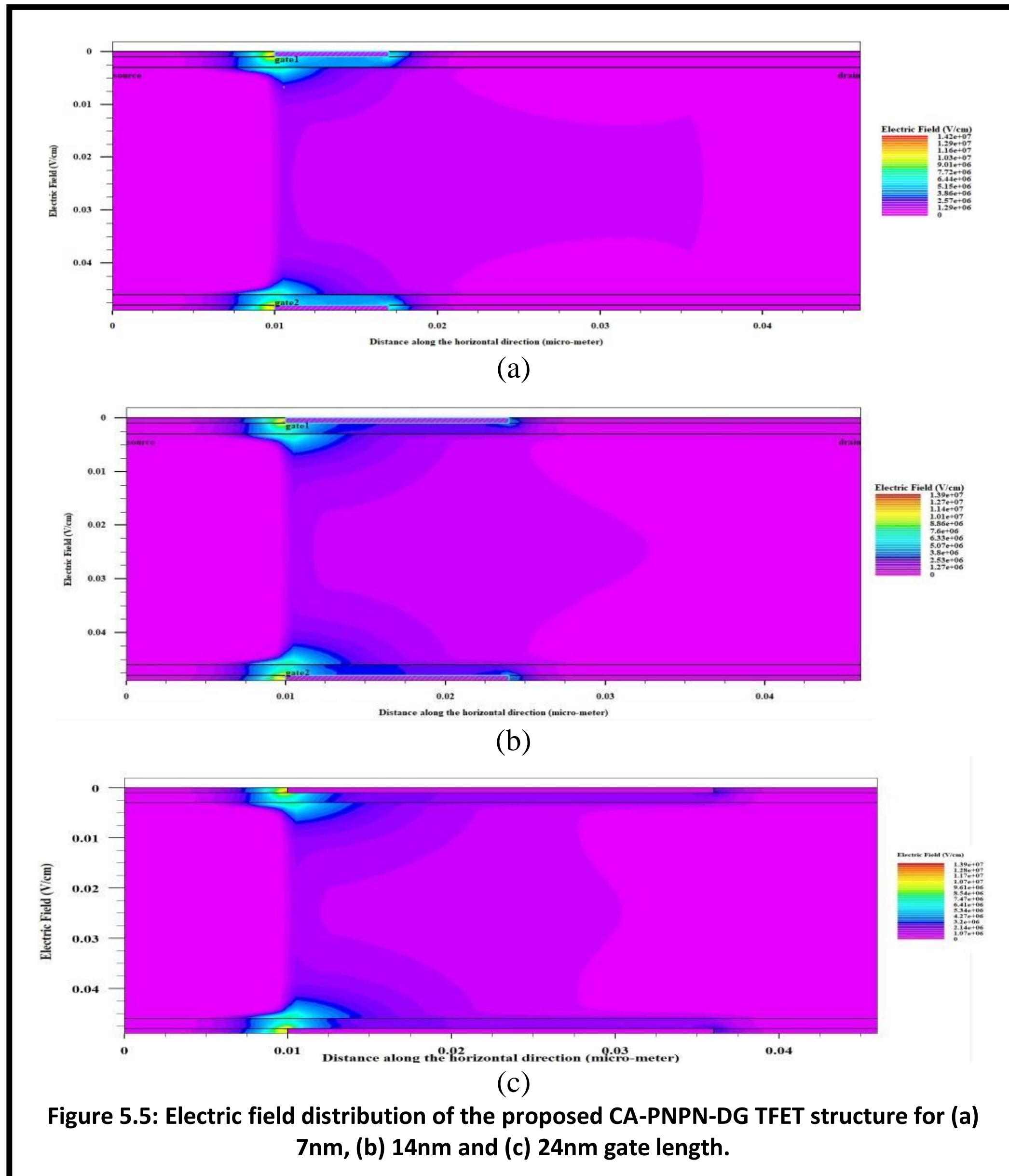


Figure 5.4: Potential Distribution along the length of the proposed CA-PNPN-DG TFET structure for (a) 7nm, (b) 14nm and (c) 24nm gate length.

5.3.3.2 Electric Field Distribution

The electric field profiles for various gate lengths have been delineated in Fig.3. For a gate length of 14nm and 24nm, the electric field is non-uniform in the channel which is obvious from the distribution curvature in Fig.3.(b) and Fig.3.(c). Besides that two symmetrical zero electric field regions are shaped towards the drain side of the channel for these two cases. Considering Fig.3.(a) 7nm gate length structure, it is noticeable that the electric field is uniform at the channel side and the zero field areas are practically missing.



(a)

(b)

(c)

Figure 5.5: Electric field distribution of the proposed CA-PNPN-DG TFET structure for (a) 7nm, (b) 14nm and (c) 24nm gate length.

The electric field along the length of the PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths have been portrayed in Fig.7. The high electric field at the source channel intersection clarifies the tunnelling phenomena while the expansion of electric field at the

channel-drain intersection exhibits that the electrons from drain side cannot pass to the channel. Thus diminishing the ambipolarity of the device.

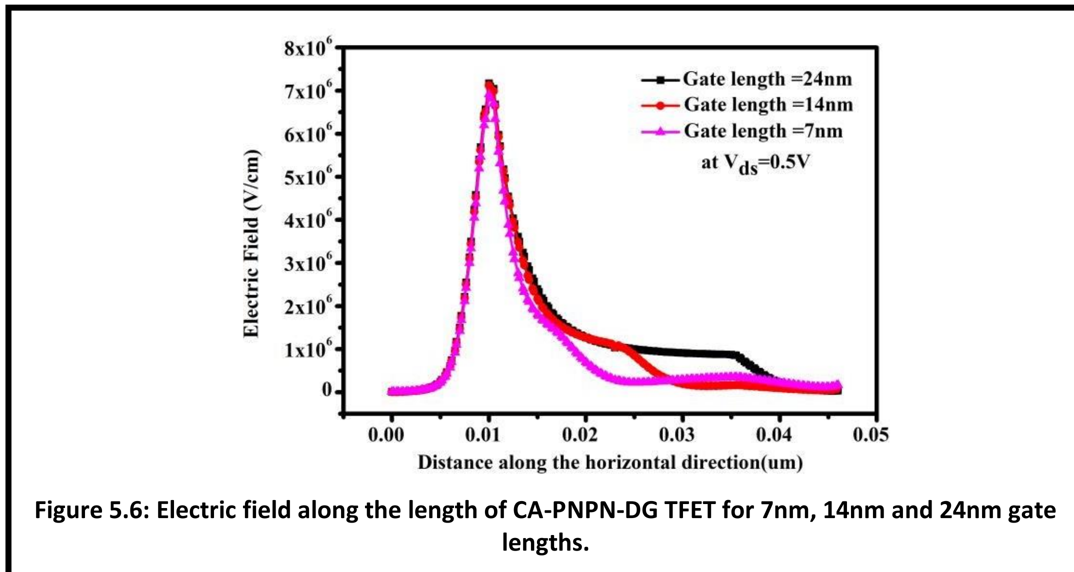


Figure 5.6: Electric field along the length of CA-PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths.

5.3.3.3 Conduction Band and Valence Band Energy

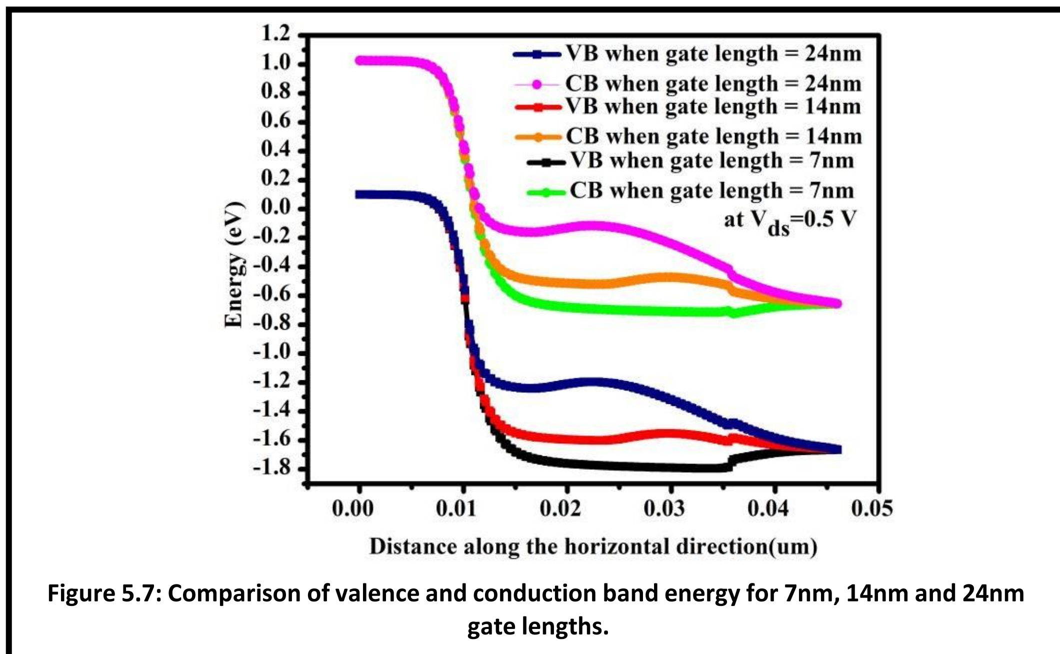


Figure 5.7: Comparison of valence and conduction band energy for 7nm, 14nm and 24nm gate lengths.

The correlation of conduction and valence bands for the structures with three diverse gate lengths is represented in Fig.5 It can be noticed from the diagram that the tunneling is practically comparative for the three cases, however, 7nm gate length structure displays reverse band bending at the channel-drain junction which shows the reason for decreased ambipolar conduction for the resultant structure. Likewise, it is clear that valence and conduction bands

are getting parallel to one another along the drain region which invalidates the further plausibility of ambipolar conduction.

5.3.3.4 Transfer Characteristics

The transfer characteristics of CA-PNPN-DG TFET for three diverse gate lengths of 7nm, 14nm and 24nm have been illustrated in Fig.8. The structure with the minimum gate length of 7nm displays OFF current of the order of 10^{-16} to 10^{-17}. It illustrates that the smaller gate length upgrades the execution of the device and henceforth 7nm structure is the best among the three considered in this work.

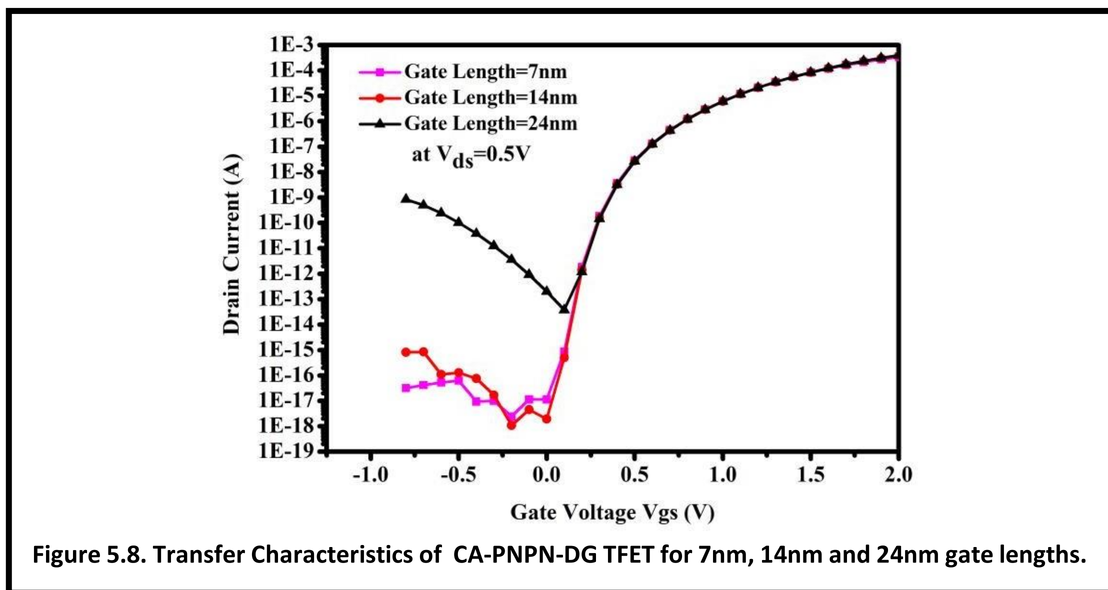


Figure 5.8. Transfer Characteristics of CA-PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths.

5.4. Incorporation of two symmetric pockets at Source Region in TFET: 2D- Modeling and Simulation-Based Performance Assessment

5.4.1 Device Structure of a TB-PNPN-DG TFET

The proposed 2D structure of the double gate TFET consists of two symmetric gates on both top and bottom of the device. The device length is considered to be 46nm along with the vertical dimension of 49nm. The gate length is varied [13] to 24nm, 14nm and 7nm whereas the effective channel length is examined to be 24nm. SiO2 is applied as the oxide material on both side of the device having length as same as the device and thickness of t_{ox}=2nm. The 10nm long drain region is of N+ type with doping concentration of $5x10^{18}$ cm^{-3}. The source region has P+ type doping concentration of $5x10^{20}$ cm^{-3} having the dimension of 10nm length and 43nm of depth.

In addition to this the source region consists of two symmetric pockets of N+ type doped

regions having concentration of 10^{19} cm^{-3} with each having the dimension of 2nm length and 10nm of depth. Both the gate contacts have work function of 5.1eV and the source and drain contacts are considered to be in vertical direction on two opposite sides of the proposed structure.

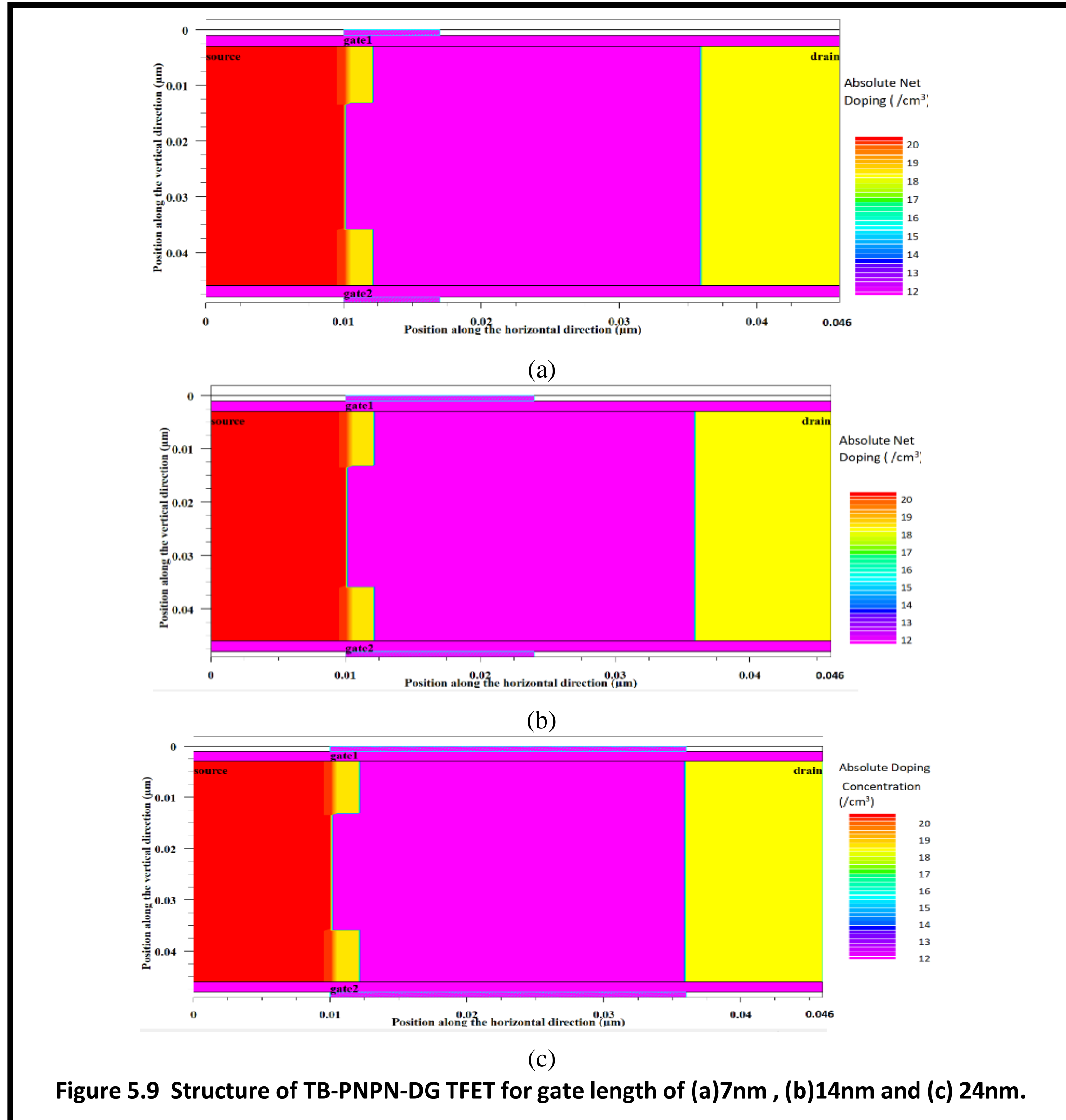


Figure 5.9 Structure of TB-PNPN-DG TFET for gate length of (a)7nm , (b)14nm and (c) 24nm.

5.4.2 Analytical Model

The analytical modelling of the surface potential has been verified with the simulated results.

Surface Potential

2-D Poisson's equation is used to administer the surface potential of the proposed structure which is given by

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=\frac{qN_{cn}}{\varepsilon_{si}} \tag{1}$$

Where $0\le x\le L$ and $0\le y\le t_{si}$

Here N_{cn} is the doping concentration at the channel region and the channel length L is divided into three regions. Thus the total length L = L1+L2+L3. The surface potential profile has been approximated using the parabolic polynomial function such as

$$\phi(x,y)=\phi_s(x)+C_1(x)y+C_2(x)y^2 \tag{2}$$

Where C1 and C2 are arbitrary functions of x and $\phi_s(x)$ is surface potential. As the channel is divided into three regions of aforementioned length therefore the surface potential under different regions as considered here can be represented in the following way

$$\phi_j(x,y)=\phi_{sj}(x)+C_{j1}(x)y+C_{j2}(x)y^2 \tag{3}$$

for $L_{j-1}\le x\le L_j$, $0\le y\le t_{si}$ and j=1,2 ,3.

The surface potential can be achieved by solving the Poisson's equations with the application of the boundary conditions as follows.

The electric field is continuous at y=0 that is for the front–gate oxide interface which leads to the three expressions corresponding to three regions below:

$$\left.\frac{d\phi_1(x,y)}{dx}\right|_{y=0}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s1}(x)-V_{GS1}}{t_f} \tag{4}$$

$$\left.\frac{d\phi_2(x,y)}{dx}\right|_{y=0}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s2}(x)-V_{GS1}}{t_f} \tag{5}$$

$$\left.\frac{d\phi_3(x,y)}{dx}\right|_{y=0}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s3}(x)-V_{GS1}}{t_f} \tag{6}$$

Here $V_{GS1}=V_{GS}-V_{FB,L1}$ and $V_{FB,L1}=\phi_{MS1}=\phi_M-\phi_{si}$ where $V_{FB,L1}$ is the flat band potential , ϕ_M and ϕ_{si} are the metal and silicon work functions respectively. Also, $\phi_{si}=\chi+\frac{E_g}{2q}+\phi_B$ where χ is electron affinity, E_g is bandgap of silicon, ϕ_B is built-in potential and is given by $\phi_B=V_T\ln\frac{N_{cn}}{n_i}$.

The electric field is continuous at y=t_{si} that is for the back–gate oxide interface which leads to the three expressions corresponding to three regions below:

$$\left.\frac{d\phi_1(x,y)}{dx}\right|_{y=t_{si}}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{V'_{GS,b1}-\phi_{B1}(x)}{t_b} \tag{7}$$

$$\left.\frac{d\phi_2(x,y)}{dx}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V'_{GS,b1} - \phi_{B2}(x)}{t_b} \tag{8}$$

$$\left.\frac{d\phi_3(x,y)}{dx}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V'_{GS,b1} - \phi_{B3}(x)}{t_b} \tag{9}$$

where $V'_{GS1,b} = V_{GS} - V_{FB,L1}$

Using these three boundary conditions mentioned above solution for the arbitrary functions of the parabolic approximation are found to be

$$C_{11}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s1}(x) - V_{GS1}}{t_f} \tag{10}$$

$$C_{21}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s2}(x) - V_{GS1}}{t_f} \tag{11}$$

$$C_{31}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s3}(x) - V_{GS1}}{t_f} \tag{12}$$

$$C_{12}(x) = \frac{1}{2C_{si}t_{si}^2}\left[C_b(V'_{GS,b1} - \phi_{B1}(x)) - C_f(\phi_{s1}(x) - V_{GS1})\right] \tag{13}$$

$$C_{22}(x) = \frac{1}{2C_{si}t_{si}^2}\left[C_b(V'_{GS,b1} - \phi_{B2}(x)) - C_f(\phi_{s2}(x) - V_{GS1})\right] \tag{14}$$

$$C_{32}(x) = \frac{1}{2C_{si}t_{si}^2}\left[C_b(V'_{GS,b1} - \phi_{B3}(x)) - C_f(\phi_{s3}(x) - V_{GS1})\right] \tag{15}$$

The values of these constants are put into (2) and solving for (1), the surface potential is achieved in the following format corresponding to the three regions considered in the structure,

$$\frac{\partial^2\phi_{s1}(x)}{\partial x^2} - \alpha\phi_{s1}(x) = \beta_1 \tag{16}$$

$$\frac{\partial^2\phi_{s2}(x)}{\partial x^2} - \alpha\phi_{s2}(x) = \beta_2 \tag{17}$$

$$\frac{\partial^2\phi_{s3}(x)}{\partial x^2} - \alpha_3\phi_{s3}(x) = \beta_3 \tag{18}$$

where α, α_3, β_1, β_2 and β_3 are given by:

$$\alpha = \frac{2C_f}{C_{si}t_{si}^2\left(1 + \frac{C_{ox}}{C_{si}} - \frac{C_f}{C_{si}}\right)} \tag{19}$$

$$\beta_1 = \left[-\frac{qN_{cn}}{\varepsilon_{si}} - \frac{2V_{GS1}C_f}{C_{si}t_{si}^2} \right] \left[\frac{1}{1+\frac{C_{ox}}{C_{si}} - \frac{C_f}{C_{si}}} \right] \quad (20)$$ and

$$\beta_2 = \left[-\frac{qN_{cn}}{\varepsilon_{si}} - \frac{2V_{GS1}C_f}{C_{si}t_{si}^2} \right] \left[\frac{1}{1+\frac{C_{ox}}{C_{si}} - \frac{C_f}{C_{si}}} \right] = \beta_1 \quad (21)$$

$$\alpha_3 = \frac{2C_f'}{C_{si}t_{si}^2\left(1+\frac{C_{ox}}{C_{si}} - \frac{C_f'}{C_{si}}\right)} \quad (22)$$ and

$$\beta_3 = \left[-\frac{qN_{cn}}{\varepsilon_{si}} - \frac{2V_{GS1}C_f'}{C_{si}t_{si}^2} \right] \left[\frac{1}{1+\frac{C_{ox}}{C_{si}} - \frac{C_f'}{C_{si}}} \right] \quad (23)$$

Where $c_f' = c_{if} + c_{of}$ and the values of inner fringing capacitance (C_{if}) and outer fringing capacitance (C_{of}) are taken from [14].

Solving those three differential equations i.e. (15), (16) and (17) using C.F. and P.I. and combining the two, solution for surface potential of the three regions are found such as

$$\phi_{s1}(x) = Ae^{\sqrt{\alpha}x} + Be^{-\sqrt{\alpha}x} - \frac{\beta_1}{\alpha} \quad (24)$$

$$\phi_{s2}(x) = Ce^{\sqrt{\alpha}(x-L1)} + De^{-\sqrt{\alpha}(x-L1)} - \frac{\beta_2}{\alpha} \quad (25)$$

$$\phi_{s3}(x) = Ee^{\sqrt{\alpha}(x-L1-L2)} + Fe^{-\sqrt{\alpha}(x-L1-L2)} - \frac{\beta_3}{\alpha_3} \quad (26)$$

where the values of the constants A, B , C, D , E and F are found to be :

$$A = \frac{\beta_1\left(e^{\sqrt{\alpha}L_1}-1\right)}{\alpha\left(e^{2\sqrt{\alpha}L_1}-1\right)} + \frac{\left[V_{bi}\left(e^{\sqrt{\alpha}L_1}-1\right) + \left(V_{ds}\left(\frac{L_2}{L}\right)+V_{bi}\right)e^{\sqrt{\alpha}L_1}\right]}{\left(e^{2\sqrt{\alpha}L_1}-1\right)} \quad (27)$$

$$B = \frac{\beta_1 e^{\sqrt{\alpha}L_1}\left(e^{\sqrt{\alpha}L_1}-1\right)}{\alpha\left(e^{2\sqrt{\alpha}L_1}-1\right)} + \frac{e^{\sqrt{\alpha}L_1}\left[V_{bi}\left(e^{\sqrt{\alpha}L_1}-1\right) + \left(V_{ds}\left(\frac{L_2}{L}\right)+V_{bi}\right)\right]}{\left(e^{2\sqrt{\alpha}L_1}-1\right)} \quad (28)$$

$$C = \frac{\beta_2\left(e^{\sqrt{\alpha}L_2}-1\right)}{\alpha\left(e^{2\sqrt{\alpha}L_2}-1\right)} + \frac{\left[\left(V_{ds}\left(\frac{L_2}{L}\right)+V_{bi}\right)\left(e^{\sqrt{\alpha}L_2}-1\right) + \left(V_{ds}\left(\frac{L_3}{L}\right)+V_{bi}\right)e^{\sqrt{\alpha}L_2}\right]}{\left(e^{2\sqrt{\alpha}L_2}-1\right)} \quad (29)$$

$$D=\frac{\beta_2 e^{\sqrt{\alpha}L_2}\left(e^{\sqrt{\alpha}L_2}-1\right)}{\alpha\left(e^{2\sqrt{\alpha}L_2}-1\right)}+\frac{e^{\sqrt{\alpha}L_2}\left[(V_{ds}(\frac{L_2}{L})+V_{bi})\left(e^{\sqrt{\alpha}L_2}-1\right)+(V_{ds}(\frac{L_3}{L})+V_{bi})\right]}{\left(e^{2\sqrt{\alpha}L_2}-1\right)} \tag{30}$$

$$E=\frac{\beta_3\left(e^{\sqrt{\alpha_3}L_3}-1\right)}{\alpha_3\left(e^{2\sqrt{\alpha_3}L_3}-1\right)}+\frac{\left[(V_{ds}(\frac{L_3}{L})+V_{bi})\left(e^{\sqrt{\alpha_3}L_3}-1\right)+(V_{ds}+V_{bi})e^{\sqrt{\alpha_3}L_3}\right]}{\left(e^{2\sqrt{\alpha_3}L_3}-1\right)} \tag{31}$$

$$F=\frac{\beta_3 e^{\sqrt{\alpha_3}L_3}\left(e^{\sqrt{\alpha_3}L_3}-1\right)}{\alpha_3\left(e^{2\sqrt{\alpha_3}L_3}-1\right)}+\frac{e^{\sqrt{\alpha_3}L_3}\left[(V_{ds}(\frac{L_2}{L})+V_{bi})\left(e^{\sqrt{\alpha_3}L_3}-1\right)+(V_{ds}(\frac{L_3}{L})+V_{bi})\right]}{\left(e^{2\sqrt{\alpha_3}L_3}-1\right)} \tag{32}$$

Where , L_1, L_2 and L_3 are considered as

$$L_1=l_p$$

$$L_2=l_g-l_p$$

$$L_3=L-l_g-l_p$$

and l_p, l_g are defined as the length of the source pocket region and gate respectively.

5.4.3 Results and Discussions

Attempts are made for Analytical modelling and simulation-based validation studies of the proposed device structures. The simulation results along with visual graphical plots of potential profiles, electric field, electron current, hole current, total current etc. for different gate lengths of the structure are depicted in this section.

5.4.3.1 Potential Distribution

The potential distribution for different gate lengths have been shown in Fig.2. For gate length 7nm depicted in Fig.2.(a) the variation of potential along the vertical dimension at any vertical line is almost nil whereas for gate length of 14nm and 24nm as shown in Fig.2.(b) and Fig.2.(c) the potential varies in vertical dimension which is clear from the curvature of the distributions. So, it signifies that the 7nm structure exhibits negligible ambipolarity and also is more stable.

Comparison between simulated results of surface potential along device length for 7nm, 14nm and 24nm gate length PNPN-DG TFET is shown in Fig.3 which exhibits the surface potential distribution along the length of the device for three different gate lengths of 7nm, 14nm and 24nm.

(a)

(b)

(c)

Figure 5.10. The Potential distribution for different gate lengths (a) 7nm, (b) 14nm , (c) 24nm.

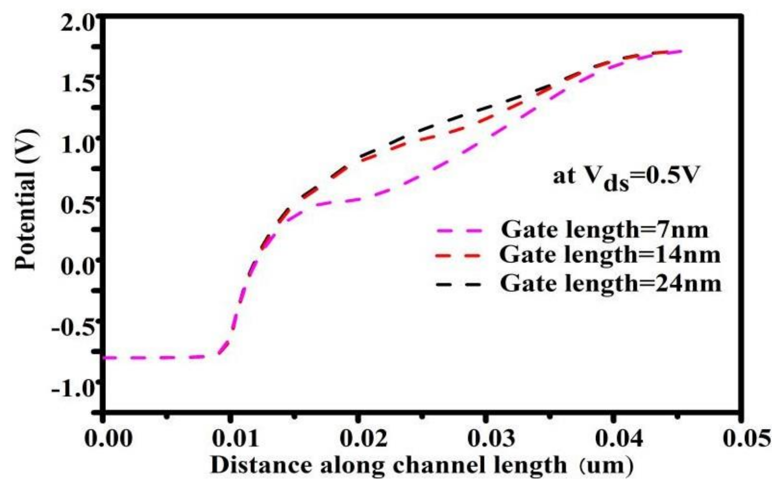
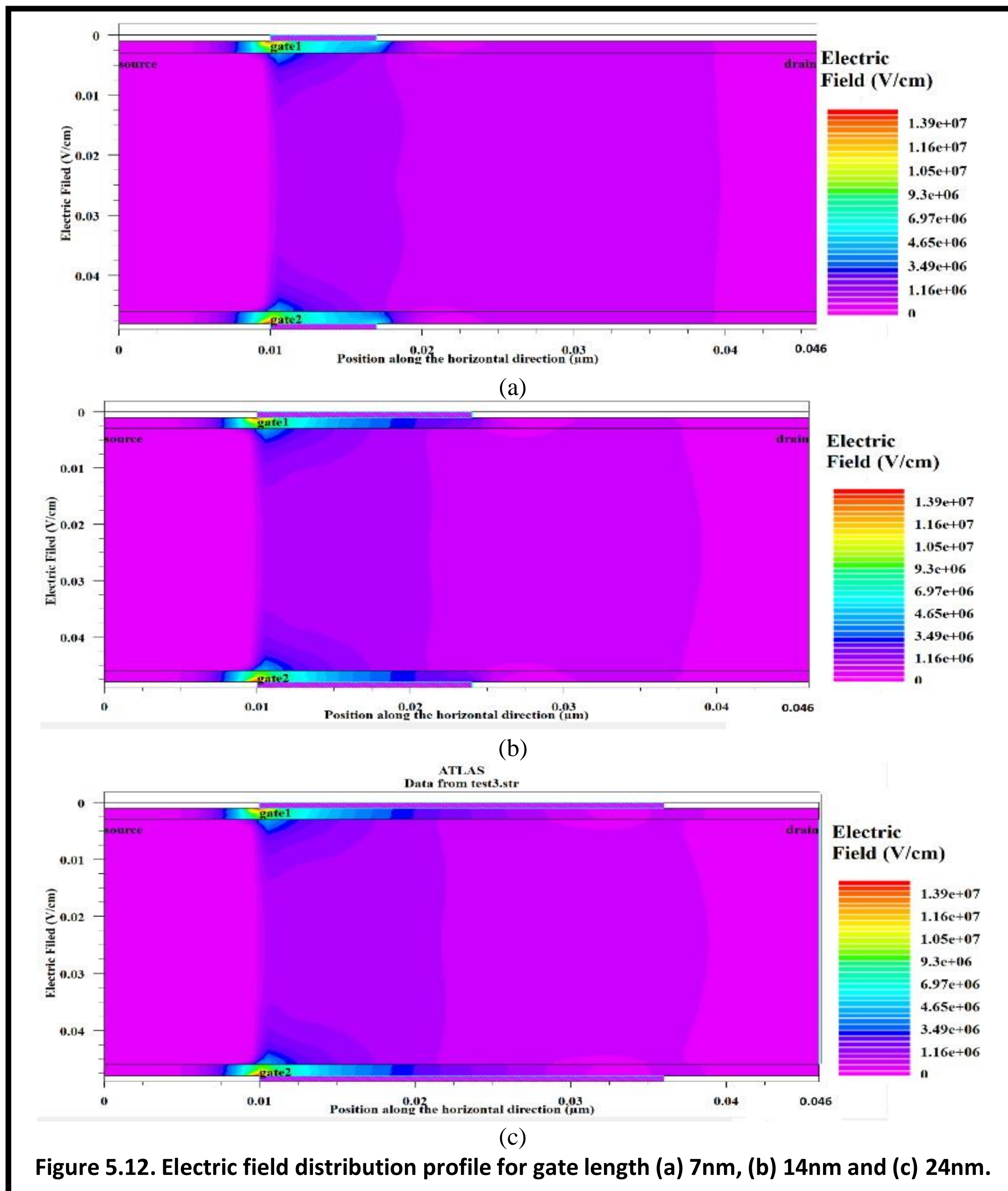


Figure 5.11. Simulation-based results of surface potential distribution for 7nm, 14nm and 24nm gate lengths.

5.4.3.2 Electric Field Distribution



(a)

(b)

(c)

Figure 5.12. Electric field distribution profile for gate length (a) 7nm, (b) 14nm and (c) 24nm.

The electric field distribution profiles for different gate lengths have been illustrated in Fig.4. For 14nm and 24nm gate length shown in Fig.4.(b) and Fig.4.(c) the electric field is non uniform at the drain side which is evident from the distribution curvature. Along with that two symmetrical zero electric field regions are formed towards the drain side of the channel for these two cases. Considering Fig.4.(a) 7nm gate length structure it is visible that the electric field is uniform at the drain side and the zero field regions are almost absent.

The electric field along the length of the PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths have been depicted in Fig.6. The high electric field at the source channel junction

explains the tunnelling phenomenon whereas the increase of electric field at the channel drain junction demonstrates the fact that the electrons from drain side cannot tunnel to the channel i.e. in reverse direction. This in turn helps to reduce the ambipolarity of the device.

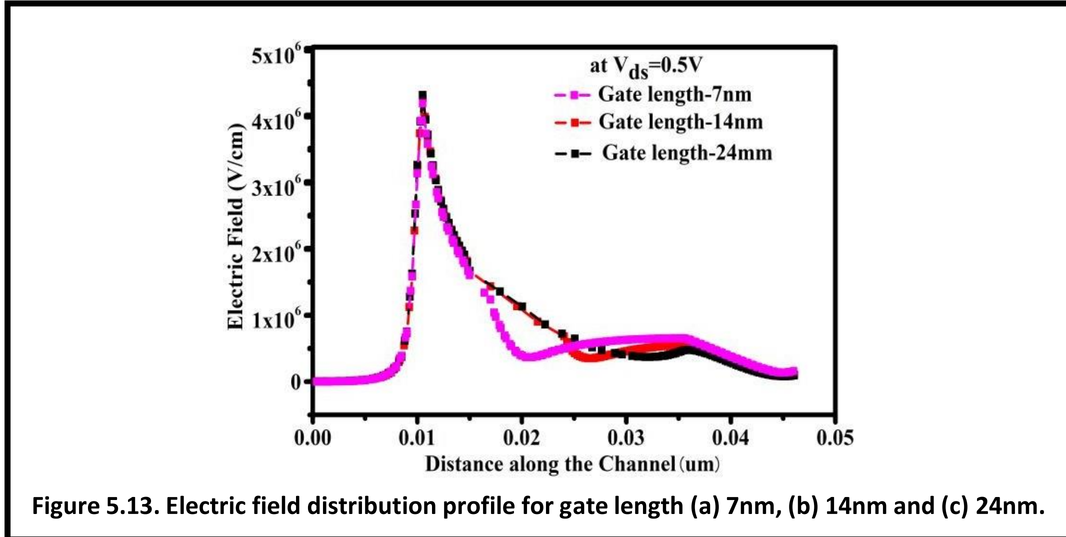


Figure 5.13. Electric field distribution profile for gate length (a) 7nm, (b) 14nm and (c) 24nm.

5.4.3.3 Conduction and Valence Band Energy

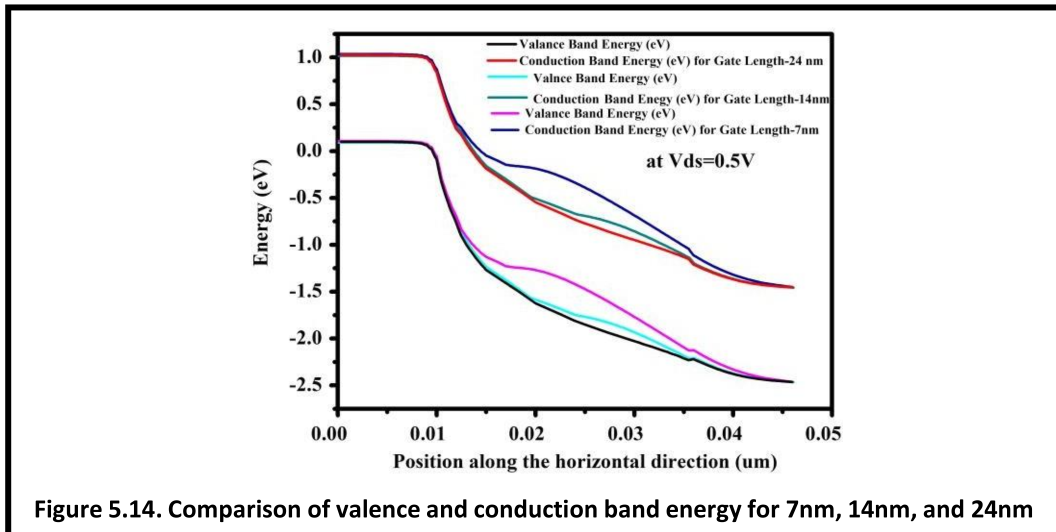


Figure 5.14. Comparison of valence and conduction band energy for 7nm, 14nm, and 24nm

The comparison of conduction and valence band energy for the structures with three different gate lengths is illustrated in Fig.5. It is evident from the graph that the tunnelling is almost similar for the three cases but 7nm gate length structure exhibits reverse band bending at channel drain junction side which manifests the cause of reduced ambipolar conduction for the same. Also it is evident that valence and conduction bands are getting parallel to each other along the drain region which negates the further possibility of ambipolar conduction.

5.4.3.4 Transfer Characteristics

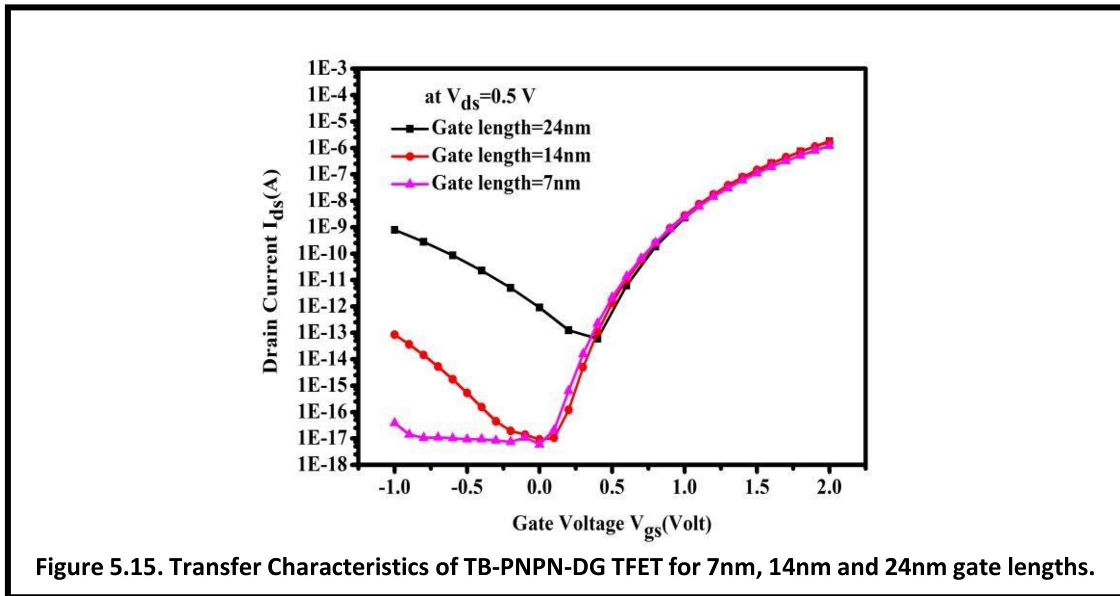


Figure 5.15. Transfer Characteristics of TB-PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths.

The transfer characteristics of PNPN-DG TFET for three different gate lengths of 7nm, 14nm and 24nm have been demonstrated in Fig.5.15. The structure with smallest gate length of 7nm exhibits OFF current of the order of 10^{-16} to 10^{-17}. It elucidates that the smaller gate length enhances the performance of the device and hence 7nm structure is the best among the three considered in this work.

5.5 Comparison:

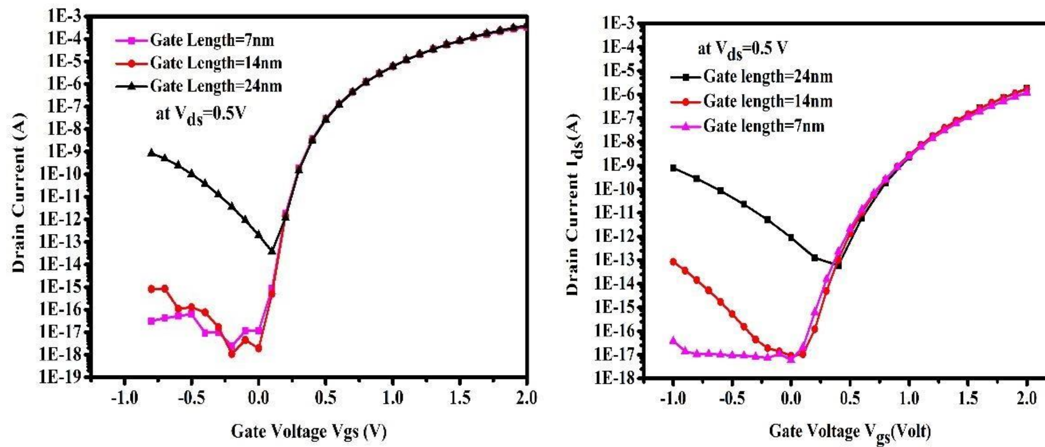


Figure 5.16. Transfer Characteristics of PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths.

Figure 5.16. shows the comparative plot of both CA-PNPN-DG TFET and TB-PNPN-DG TFET . from here it can be justified that the CA-PNPN-DG TFET show better subthreshold swing of 23mv/dec, but having ambipolar current having I_{ON}/I_{OFF} of 10^{13}. Here as the TB-PNPN-DG TFET show that ambipolar current is almost Nil with having a I_{ON}/I_{OFF} of 10^{12} and

SS of 30mv/dec at applied V_{DS}=0.5 volt. Considering the all the parameters to implement a circuit for we opts for CA-PNPN-DG TFET. Therefore, for all future analysis we will consider the CA-PNPN-DG TFET.

5.6 Frequency Analysis

The g_m, C_{gs}, C_{gd}, GBP, τ, f_T, TGF and TFP have all been studied and discussed in this section. Fig. 10(a) and 10(b) illustrate the gate-to-source and gate-to-drain capacitance curves, respectively. C_{gs} rises as V_{gs} rises, but C_{gd} falls as V_{gs} rises. When gate length decreases, the gate lost its control over the current carrier. Here when the channel length 7nm, a losing control means it is now controlling less amount of charge. Controlling the less charge means the capacitor store less amount of charge. So, at low channel length Cgd is less. But as source is not beyond the gate, or it is just before the gate. There is no voltage variation is source and gate. So, there is very less difference is Cgs carve.

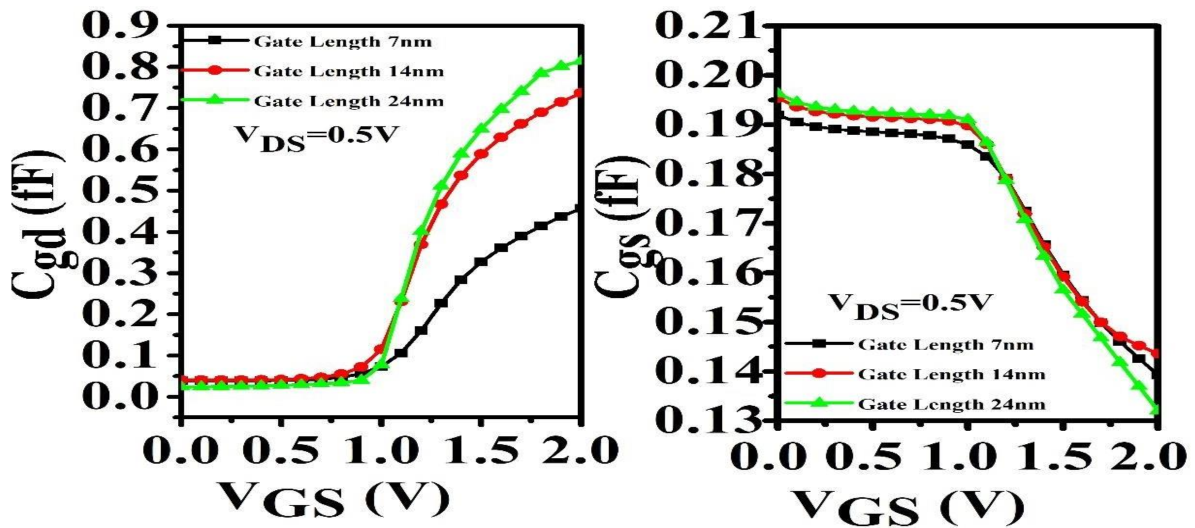
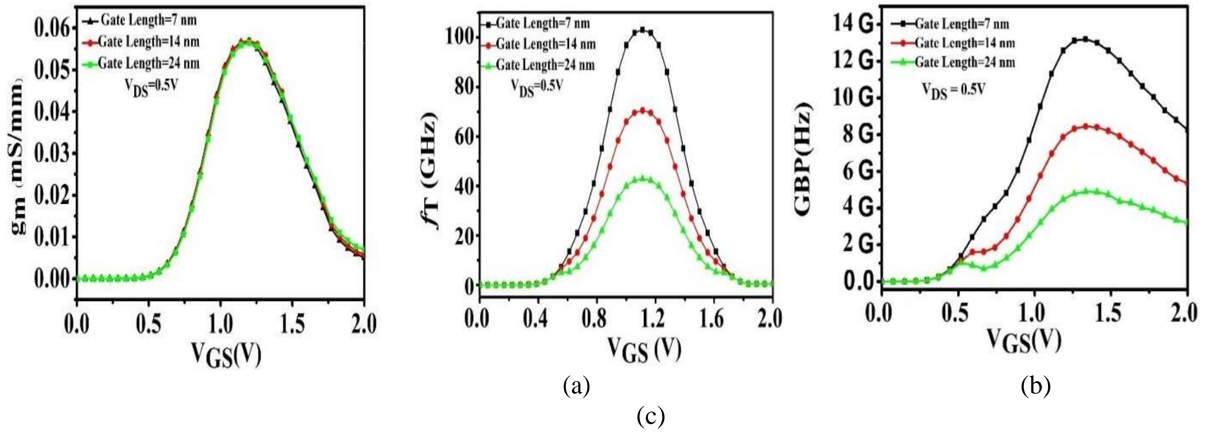


Figure 5.17: Plot of (a) C_{gs} (b)C_{gd} w.r.t V_{GS}

CA-PNPN-DG TFET g_m characteristics are shown in Fig 11(a). With an increase in V_{gs}, the g_m rises. The rate of conversion of gate voltage to drain current is measured by a device's g_m. The frequency at which short-circuited current achieves unity is known as the cut-off frequency (f_T). It is provided by,

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \quad \text{--------(8)}$$

The cut-off frequency increases as V_{gs} increases due to an increase in g_m, as seen in Fig 10(a) and 10(b). CA-PNPN-DG TFET has a cut-off frequency of 100 GHz. [20] The GBP denotes a device's constant gain region. CA-PNPN-DG TFET has a GBP of 12 GHz, as shown in Fig 10(c).



(a) (b)

(c)

Figure 5.18: Plot of (a)g_m (b) f_T (c) GBP wrt V_{GS}

The time it takes for charge carriers to travel from source to drain is called transit time(τ). The transit time of a device is inversely related to its switching performance. The transit time of CA-PNPN-DG TFET is shown in Fig. 11, and it can be seen that switching performance improves as gate-to-source voltage increases. Which is explained as follows in [20, 23],

$$\tau = \frac{1}{2\pi f_T} \text{-----------} (9)$$

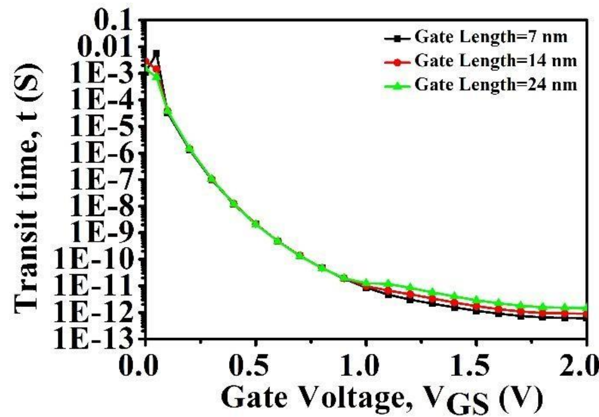


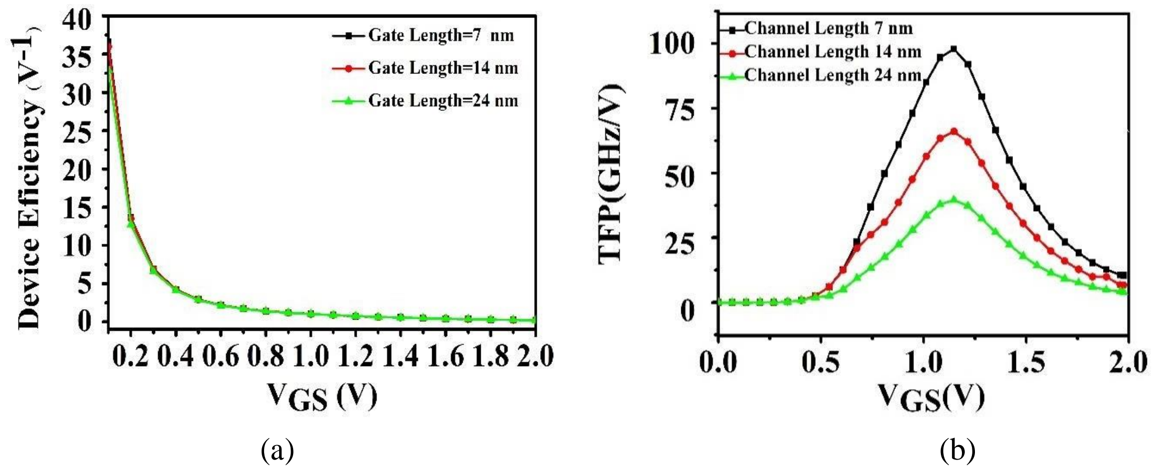
Figure 5.19: Plot of Transit-time(τ) w.r.t V_{GS}

The capacity of a device to convert current to transconductance is known as the transconductance generation factor (TGF). TGF is a trade-off between a device's power and high-speed functioning. It is provided by,

$$TGF = \frac{g_m}{I_{DS}} \text{--------------} (10)$$

The transconductance frequency product (TFP) is the trade-off between a device's bandwidth and power. [9], where TFP is provided by,

$$TGP = \frac{g_m}{I_{DS}} x f_T \text{----------------------} (11)$$



(a) (b)

Figure 5.20: Plot of (a) TGF (b) TFP w.r.t V_{GS}

TGF and TFP plots of CA-PNPN-DG TFET are shown in Figures 12a and 12b. Devices with higher TFP implies good linearity of any FET device and required for high-speed circuit design. The simulated results of shows that gate length 7nm is more suitable then the other two CA-PNPN-DG TFET structure

5.7 Circuit Design

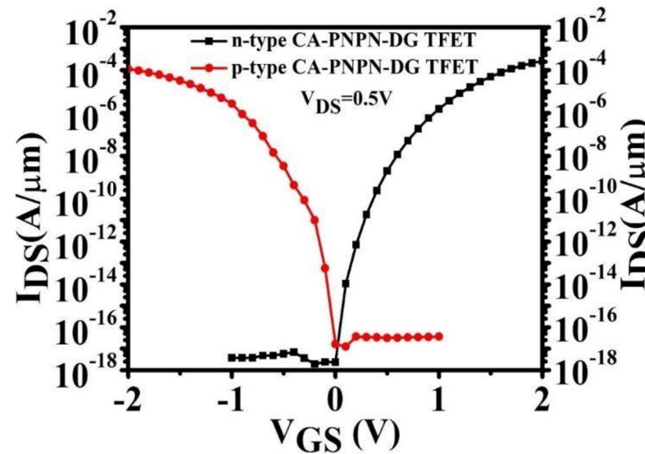


Figure 5.21: I_{DS} VS V_{GS} at V_{DS}=0.5V for n and p-type CA-PNPN-DG TFET

A spice model of the proposed DGF-TFET has been discussed in this part in order to adapt it for logical applications and evaluate circuit level AC performance. The TFET inverter was developed in tanner SPICE. A p-type DGF-TEFT with the same design characteristics as an n-type DGF-TFET was used to simulate the inverter.

The output characteristics of the proposed inverter for both n-type and p-type are shown in Fig. 14. At V_{DD}=1V, the DC performance of the CA-PNPN-DG TFET inverter has been assessed using the VTC curve in Fig. 15. The amount of noise an inverter circuit can take

without affecting the circuit's performance has been estimated using the VTC curve, which is presented in Table 1.

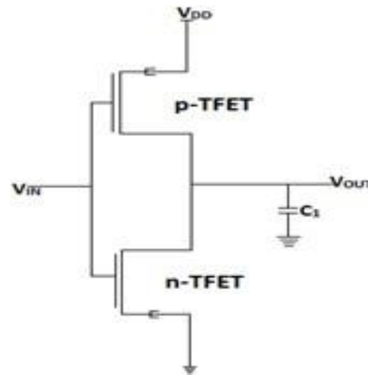


Figure 5.22: Schematic Diagram of CA-PNPN-DG TFET inverter

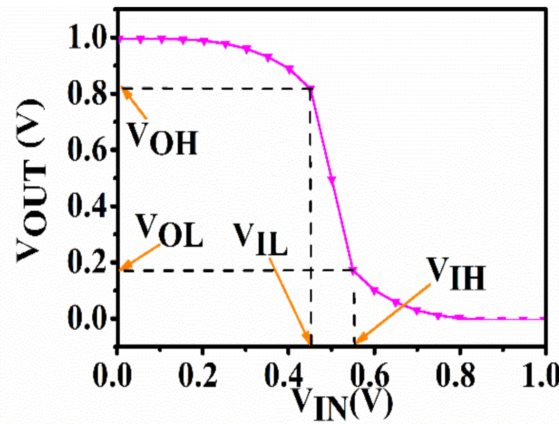


Figure 5.23: VTC of CA-PNPN-DG TFET inverter

Parameters	DC value in Voltage
V_{IL}	0.453V
V_{OL}	0.187 V
V_{IH}	0.558mV
V_{OH}	0.812mV
$NM_L=V_{IL}-V_{OL}$	0.266V
$NM_H= V_{OH}-V_{IH}$	0.254V
Power consumption	47.3nw
Delay	56.28ps

Table 5.1: Different parameters of the inverter based on the proposed CA-PNPN-DG TFET structure

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Chapter:6

Chapter-6: Investigating Ambipolar Current and Quantum Confinement Effect in Two-Source TFET

6.1 Introduction 171
6.2 Literature Survey 172
6.3 Device structure and Parameters 175
6.4 Results and discussions 177
6.4.1 Transfer Characteristics of proposed TFETs for Various Channel length 177
6.4.2 Variation of Oxide Thickness 178
6.4.3 Variation of Gate Work Function 179
6.4.4 Total Current Density & Band to Band Tunneling (BTBT) 180
6.4.5 Output Characteristics of proposed DSS-TFETs... 181
6.5 Circuit-Level Analysis 182
References 189

6.1 Introduction

Miniaturization of device sizes has allowed accomplishing the objective of low-power, high-speed devices with increased package density, which enhances the RF performance throughout the last few decades. However, MOSFETs suffer from short channel effects such as DIBL, threshold voltage roll-off, high leakage, and others due to rigorous scaling of channel length. MOSFET SS is also restricted to 60mV/dec. On the contrary, Tunnel Field Effect Transistor (TFET), a non-conventional device with almost similar geometry, has emerged in the research lime limelight possible successor for bulk MOSFET. The switching principle for TFET is band to band tunneling mechanism through a barrier instead of modulating thermionic emission over a barrier as in traditional MOSFETs, thus it has less electron thermal voltage (kT) dependence. TFET also has a steeper SS. As a result, the TFET is becoming a promising low-power technology thanks to supply voltage scaling. However, because of the BTBT limitation, TFET has a lower I_{ON} than MOSFET. As a result, the switching delay (CV_{DD}/I_{ON}) increases. Several structural changes have been carefully investigated to solve this problem. To obtain superior SS and greater I_{ON}/I_{OFF}, U-shape, L-shape, and TRS-shape TFETs have recently been

used to enhance the tunneling area. Quantum confinement effects (QCE) affect TFETs with features smaller than or equal to 20nm. Yu and Najam investigated the influence of geometrical QCE on the performance of L-TFET in 2019.

Following the semiconductor industry's plan, a new barrier emerges in the form of a small tunnelling area in TFET, which results in a small tunnelling current. Due to the concentrated and confined tunnelling region in TFET, it has been observed that the tunnelling current is constant with respect to the channel length. During the circuit design phase, this event allows for modifying the device driving capabilities to meet the practical demands. The Double Source TFET is proposed to overcome this drawback. In addition, the proposed highly scalable symmetrical DSS n and p-type TFETs use a quantum simulation-based method to enhance device ON current and reduce ambipolarity while retaining almost uniform SS at varied gate lengths.

Before going for any digital or analog circuit-level application, the very first step is to design an inverter. However, both the n-TFET and the p-TFET should be designed appropriately to comply with the CMOS characteristics by suppressing the ambipolar current for complementary performance. Also, NAND and NOR logic gates have been designed and their performances have been compared with the existing TFET-based logic gates to ensure the low power efficiency of the proposed DSS TFETs.

6.2 Literature Survey

Sarkar et al [6.1-6.2]] have worked on Double gate FET models consisting of two gates, one at the top and the other at the bottom. This configuration improves the electrostatic control of the gate on the channel allowing the field lines from the gate to terminate at the back gate rather than terminating in the channel. The impact is well reflected as magnified ON-state current compared to single gate counterpart.

Further, Dey et al [6.3] paid their attention for a SOI based device to investigate the electrical characteristics. The entire thin silicon layer is depleted and the drain-body and source-body depletion regions are kept small. It is reported the buried oxide layer blocks all the source-to-drain leakage paths through the bulk region providing a better gate control over the channel. This also leads to a smaller source/drain to substrate capacitance.

Alper et al [6.4] validate a design methodology for logic circuits that exploit the conduction mechanism and the presence of two independently biased gates ("n-gate" and "p-gate") of the EHB-TFET. It is designed to conduct under certain conditions and allowed to implement certain logic gates having less number of transistors compared to a conventional CMOS logic.

Knoll et al [6.5] fabricated an inverter based on an uniaxially tensile strained Si nanowire TFETs, where steep junctions are formed by dopant segregation at low temperatures to improve the BTBT, resulting in higher I_{ON} of n- and p-TFETs at lower V_{DS}.

Padilla et al [6.6] analyzed an Heterogate-EHB-TFET with partially doped channels to verify the effects on TDM and occupancy probabilities.

Kumar et al [6.7] proposed a compact 2-D analytical model for electrical characteristics of DG TFETs with a SiO_2/High-k stacked gate-oxide structure resulting in higher I_{ON} at lower V_{DS}.

Tripathy et al [6.8] investigate the performance of a vertically grown GaSb/Si V-TFET with a source pocket to enhance the performance of the device and circuit-level assessment of GaSb/Si heterojunction Vertical TFET for low power applications.

Kumar et al [6.9] developed an analytical model of surface potential, electric field, drain current shows better SS and V_{th} on a DM-DG-TFETs with SiO2/HfO2 stacked gate-oxide structure.

Silicon-on-Nothing (SON), an innovative SOI version enables fabrication of extremely thin silicon (5 to 20 nm) and buried dielectric (10 to 30 nm) offering quasi-total suppression of SCEs with excellent electrical performances [6.10]. In a SON device, the buried oxide of simple SOI structure is replaced with air and it has been proven theoretically and experimentally that with the air-gap, the SCEs of the conventional SOI structures can be reduced [6.11-6.12]. SON MOSFET is an improved SOI structure which is widely discussed as a lucrative scalable solution to satisfy the ITRS Roadmap requirements [6.13].

Bhattacharjee et al [6.14] proposed analytical modeling and simulation of drain doping engineered splitted drain structured TFET. The splitted drain structure exhibits a major reduction in ambipolar conduction due to an increase of the tunnelling width at the channel-drain junction.

Bibhas et al [6.15] presented an overall performance comparison for both SOI and SON structures incorporating the concept of binary metal alloy scheme. They verified superiority of SON technology over its SOI counterpart owing to higher level of immunity for the former toward short channel limitations.

Yang et al [6.16] designed a InAs/Si as the n-type TFET and Ge/Si as the p-type TFET based complementary digital inverter structure in which the effective tunneling area & current can't be modulated by the gate length. They can be adjusted depending on the actual requirements of circuit design, thus increases the flexibility of TFET-based circuit design.

Luong et al [6.17] present on strained Si with gate all around nanowire CTFETs based structures on a single chip so with a gate-drain underlap to suppress the ambipolar behavior of the TFETs.

Lin et al[6.18] investigate the performance of recessed-gate TFETs to improve the current of TFETs by increasing the tunnel area with line tunneling with the effects of the recessed-body thickness and the doping level.

Tajally et al [6.19] demonstrated a symmetric U-shaped gate tunnel FET (SUTFET) results in higher ION, low IOFF, lesser SS, and ambipolar current, which can be obtained by using high-k dielectric close to the source and low-k dielectric in the vicinity of the drain. The strong coupling between the gate and transistor channel near the source results in reduced potential barrier width in tunnel junction due to the presence of high-k dielectric, which leads to higher ION and lower subthreshold swing. Moreover, the presence of low-k dielectric near the drain reduces the ambipolar current by increasing potential barrier height.

Woo et al [6.20] proposed a covered source–channel TFETs (CSC-TFET) with trench gate structures showing that the switching characteristics are superior to those of conventional silicon-based TFETs. An inverter circuit is also implemented using the CSC-TFET having a high frequency of approximately 1 GHz at a supply voltage of 1.0 V.

Bagga et al [6.21] demonstrate a two source regions (TSRs) based Novel SOI-based TFET structure. TSR in the SOI platform enhances the effective tunneling area between source–channel junctions and thus boosts the drive current of the device.

Najam et al [6.22] analyzed an LTFET architecture to maximize the BTBT area that employs an overlapped gate/channel/source. As the overlapped channel is very thin and suffers QCE and significantly affects the BTBT. The discretization of the conduction band reduces the BTBT drain-source current of LTFET. QCE also forces the lateral and parasitic component of BTBT to dominate for a significant portion of the gate-bias swing.

Kwon et al [6.23] verify the effects of LBD on alternating current switching characteristics of TFETs inverter with vertical structures. The inverter composed of n-/p-type TFET with the localized p+/n+ body doping results, falling/rising delay is significantly improved due to the locally high channel-to-drain side energy barrier induced by the LBD.

Upasana et al [6.24] uses the Lambert-W function to formulate a drain current model for DG p-n-i-n TFET which includes the impact of mobile charges, gate dielectric thickness, and channel thickness on quasi fermi level, gate threshold voltage (VTG), onset voltage and TBW over the entire operating range i.e. accumulation to inversion state.

Baravelli et al [6.25] investigate the feasibility of creating an inverter based on co-optimized n- and p-type tunnel field-effect transistors.

Mitra et al [6.26] demonstrated a digital inverter using a hetero-dielectric stack gate SOI-TFET with a back gate.

Tripathy et al [6.27] presented a DMG-HD-VTFET and HD-VTFET which possess superior metrics in terms of direct current and RF performance as compared with conventional VTFET and thus suitable for device and circuit-level assessment for low-power applications,"

Boggarapu et al [6.28], explore homo and heterojunction TFET-based NAND and NOR logic circuits using 30 nm technology and compare their performance in terms of power consumption and propagation delay.

Furthermore, several works have already been reported considering bandgap engineering [6.29-6.31], gate work function engineering [6.32-6.34], dielectric engineering [6.35-6.36], channel engineering (i.e. introduction of a strain in the Si-channel to enhance carrier mobility [6.37-6.39]), graded channel engineering [6.40-6.41], and source/drain material engineering [6.42-6.43] with fitting analytical models (for dual gate, tri gate, gate all around structures [6.44-6.45]) to review TFET performance in terms of revamp drive current and decreased ambipolar conduction for realization of TFET industry in nanometer domain.

6.3 Device structure and Parameters

Figs 1(a) and 1(b) show the 2D cross sectional view of the proposed n and p-type DSS TFETs (b). Although the size of both TFETs are identical, the doping options have been chosen based on the kind of TFET. Source1 and Source2 are two distinct highly doped Sources in the proposed structures. Both TFETs have a narrow lightly doped region next to the source, as illustrated in Fig 1. At the source channel junction, this structural variation helps in the introduction of the inter band tunnelling phenomenon. Because the two sources have distinct structural positions, both TFETs can be considered to have two channels (right and left channel). A lightly doped Si layer (p-type for n-TFET or vice versa) has been introduced below the abovementioned two channels to enhance carrier transport from the two sources to drain. As a result, in both

situations, it behaves as a horizontal channel. A SiO_2 box has been incorporated between the drain and source2 region to prevent drain leakage. Different effective channel lengths, such as 5nm, 7nm, 9nm, 13nm, and 20nm, have been used to investigate the performance of both TFETs. Fig 1 depicts the critical parameters for the two devices.

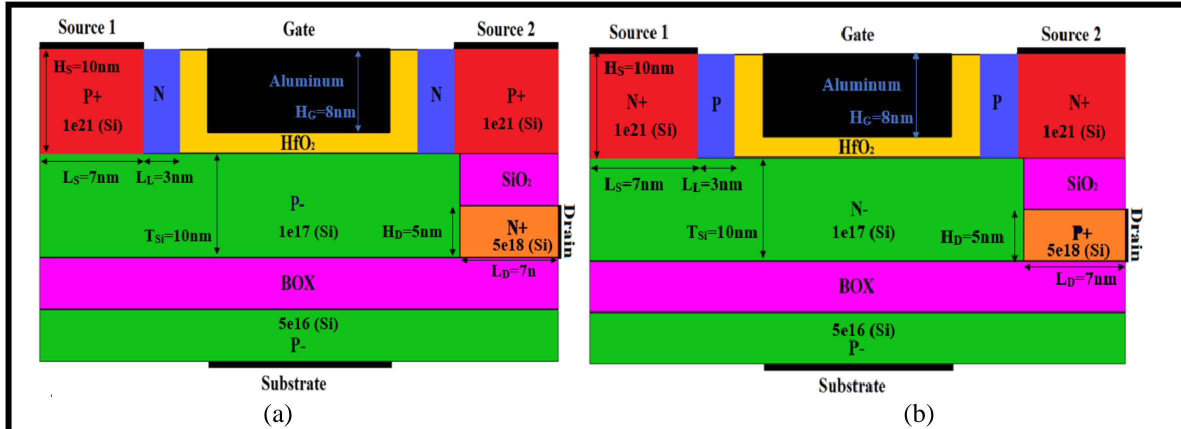


Figure 6.1 . Device structure of (a) n and (b) p-type DSS-TFET

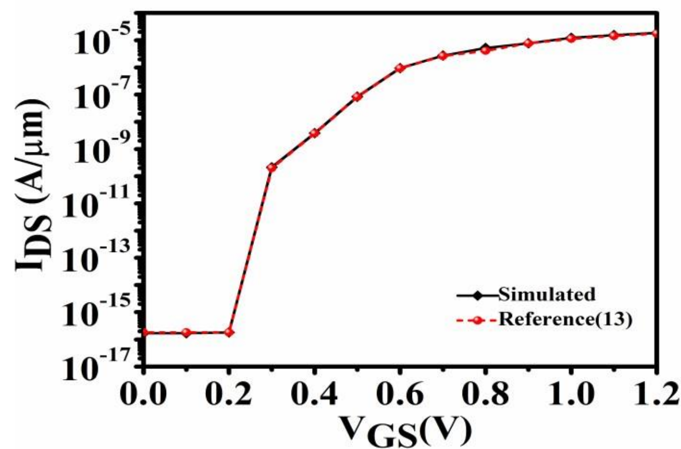


Figure 6.2 Calibration of simulation data with the experimental result of Reference [13].

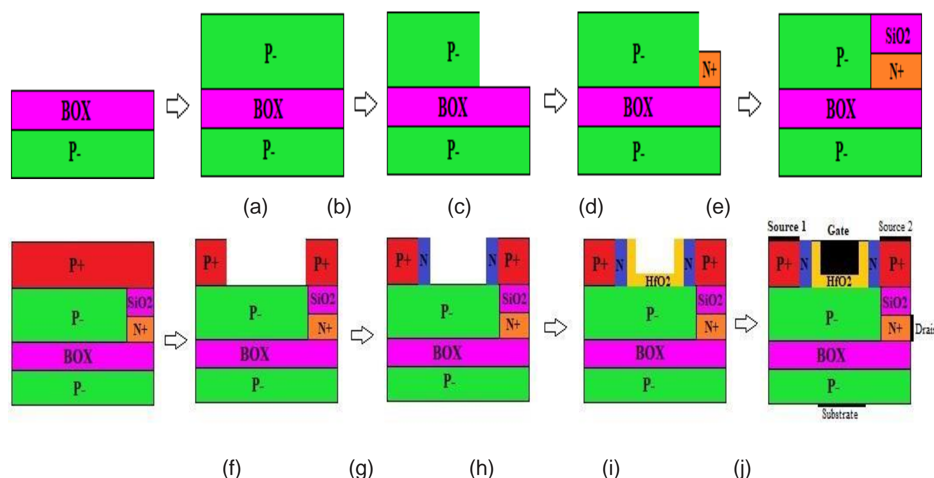


Figure 6.3 Process flow for the fabrication of the proposed DSS- TFET structure

For simulation SILVACO ATLAS has been incorporated. During simulation, many essential models such as CVT, band gap narrowing, non-local BTBT, drift diffusion carrier transport, SRH and Auger recombination and FD statistics were incorporated. The generating rate is calculated using the BTBT model. To account for ambipolar conduction, it will establish a quantum tunnelling region at both junctions. The FD statistics model was used to account for the influence of carrier concentration on device performance. The Auger and SRH recombination models have been used to account for the influence of carrier energy exchange with the surrounding lattice as well as the carrier's life period. The DSS-TFET simulated result has also been calibrated with [13]. Fig.2 shows a reasonable agreement between the two outcomes, indicating that the chosen models are genuine.

Fig. 3 depicts the manufacturing procedures for the proposed DSS-TFET. As shown in Fig. 3, it starts with the creation of a thick buried oxide layer on a p-type silicon wafer using the traditional separation approach [13]. Following that, a lightly doped p-type silicon was produced followed by a highly doped n-type drain slab using epitaxy to construct the channel and drain, as shown in Fig. 3(b)- (d). Fig. 3(e) shows the oxidation process depositing SiO_2 across the drain area. To form the double source, a highly doped P-type is grown using epitaxy process as per Fig. 3 (f). To evolve the sources, a U-shaped window is etched out from the highly doped silicon substrate as shown in Fig. 3 (g), followed by epitaxy process two pockets of n-type besides the both sources grown to enhance the tunnelling shown in Fig. 3(h). Then, as illustrated in Fig. 3(i), high-k gate oxide was deposited over the U-shaped trench area using the Atomic Layer Deposition (ALD) method. Finally, as illustrated in Fig. 3 (j), the gate is deposited and patterned before the contacts are defined at their corresponding locations.

6.4 Results and Discussion

6.4.1 Transfer Characteristics of DSS-TFETs for Various Channel length

Fig. 4 shows the I–V characteristics of both p-type and n-type DSS-TFETs. Both structures outperform [5], [8], and [11] in terms of ION/IOFF. It's worth noting that when the channel length is less than 20nm, the on and off current for both TFETs is nearly constant. As a result, the suggested device can be inferred to be scalable throughout a range of channel lengths from 5nm to 13nm. The structure is robust and scalable even at the quantum level, as shown in Fig. 5. There is negligible change in SS for both TFETs at varied gate lengths, as shown in Fig. 5.

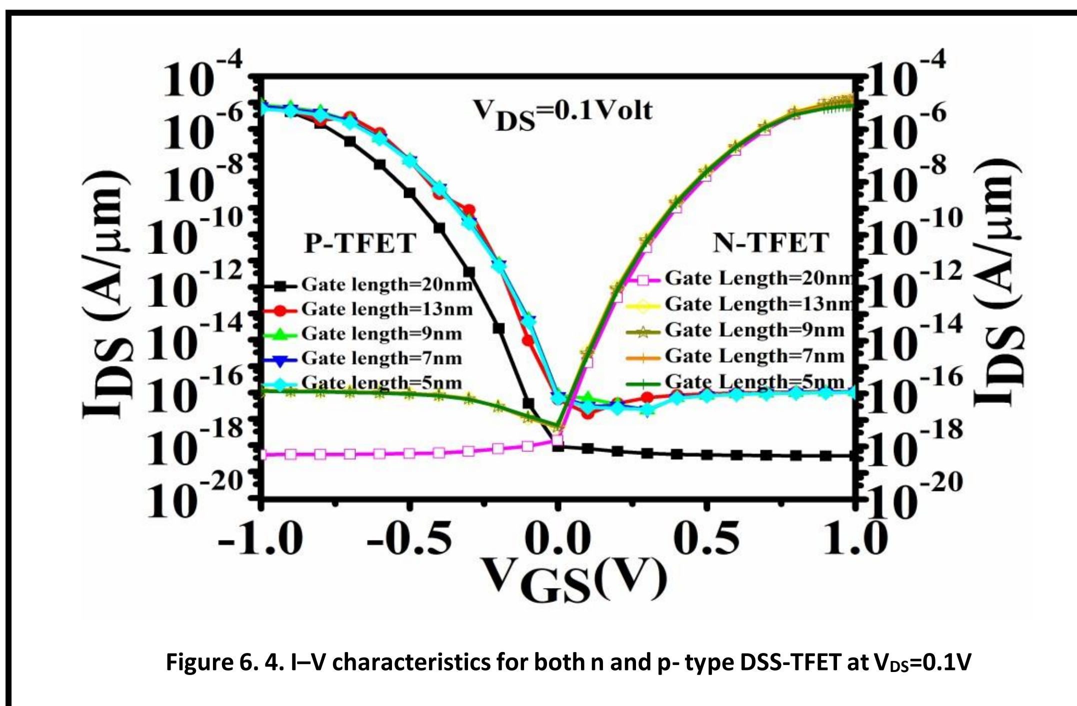


Figure 6. 4. I–V characteristics for both n and p- type DSS-TFET at V_{DS}=0.1V

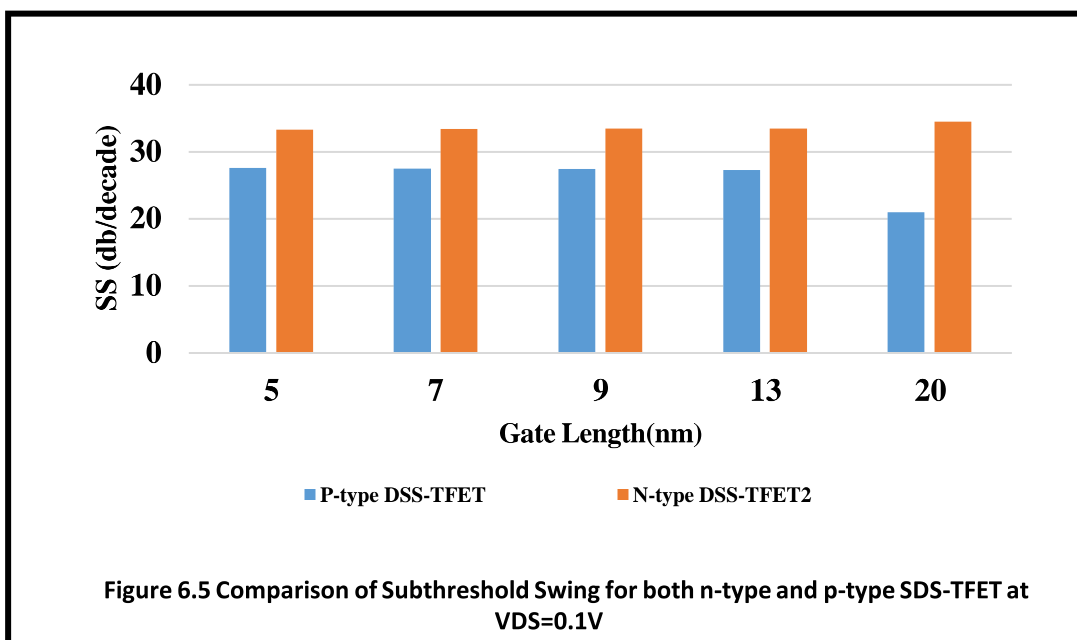


Figure 6.5 Comparison of Subthreshold Swing for both n-type and p-type SDS-TFET at VDS=0.1V

6.4.2 Variation of Oxide Thickness

For several uniform gate oxide thicknesses such as 3nm, 2nm, and 1nm, the transfer characteristics of the proposed DSS-TFETs have been investigated. Fig 6 demonstrates that the performance of both TFETs with a 1nm gate oxide thickness outperforms the other two.

However, as stated in [11], there is a chance that I_{ON}/I_{OFF} will degrade as ambipolarity increases. As a result, the suggested structural device is based on a 2nm gate oxide thickness.

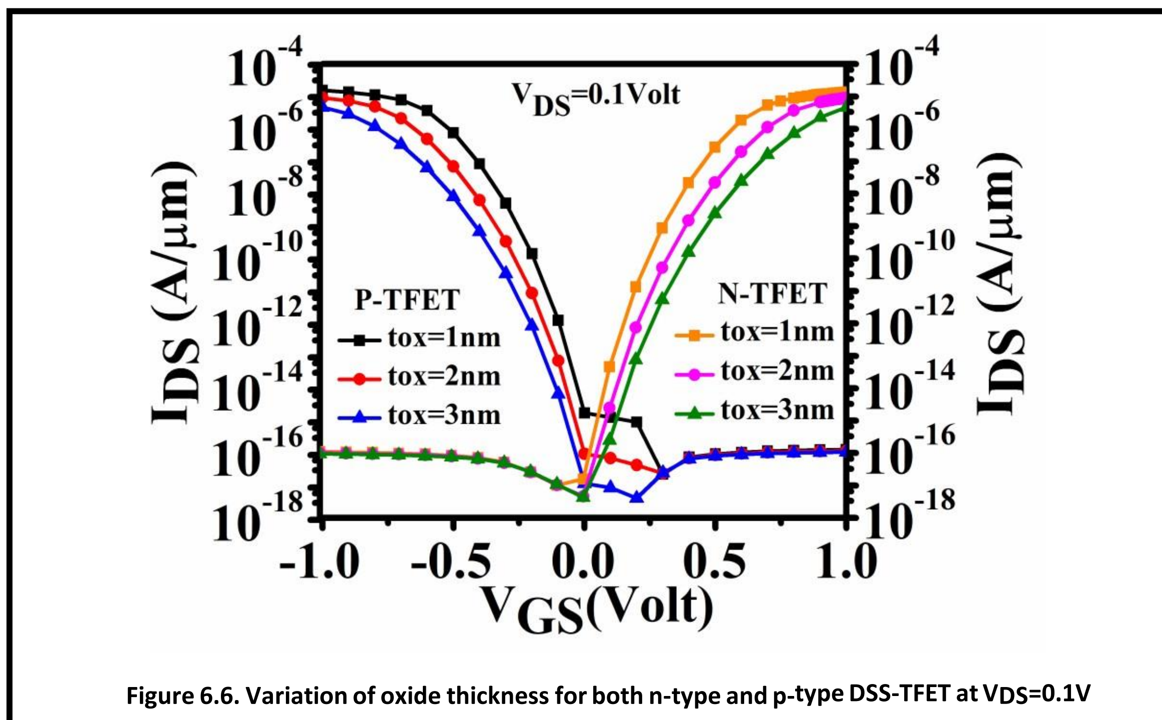


Figure 6.6. Variation of oxide thickness for both n-type and p-type DSS-TFET at V_{DS}=0.1V

6.4.3 Variation of Gate Work Function

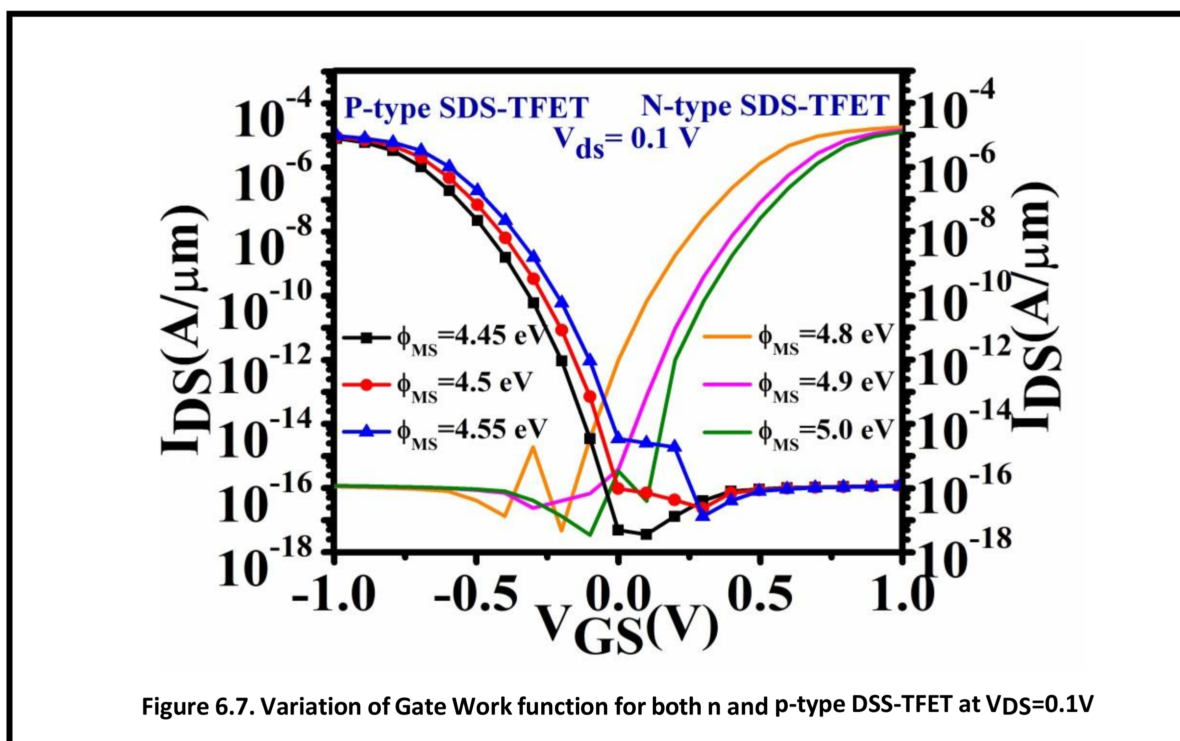


Figure 6.7. Variation of Gate Work function for both n and p-type DSS-TFET at V_{DS}=0.1V

In both n-type and p-type DSS-TFETs, the effect of gate work function variation is seen in Fig 5. Drain-channel tunnelling reduces when gate work function lowers, but source-channel tunnelling rises, as seen in traditional TFETs [11]. According to [18], in order to offer comprehensive CMOS logic functionality, ambipolar current suppression in TFETs is required for circuit design. Fig 5 shows that the proposed DSS-TFET, which has a 13nm gate length and a 2-nm oxide thickness, as well as a work function of 4.95 for n-type and 4.45 for p-type, suppresses the ambipolar current and is thus suitable for TFET inverter design.

6.4.4 Total Current Density & Band to Band Tunneling(BTBT)

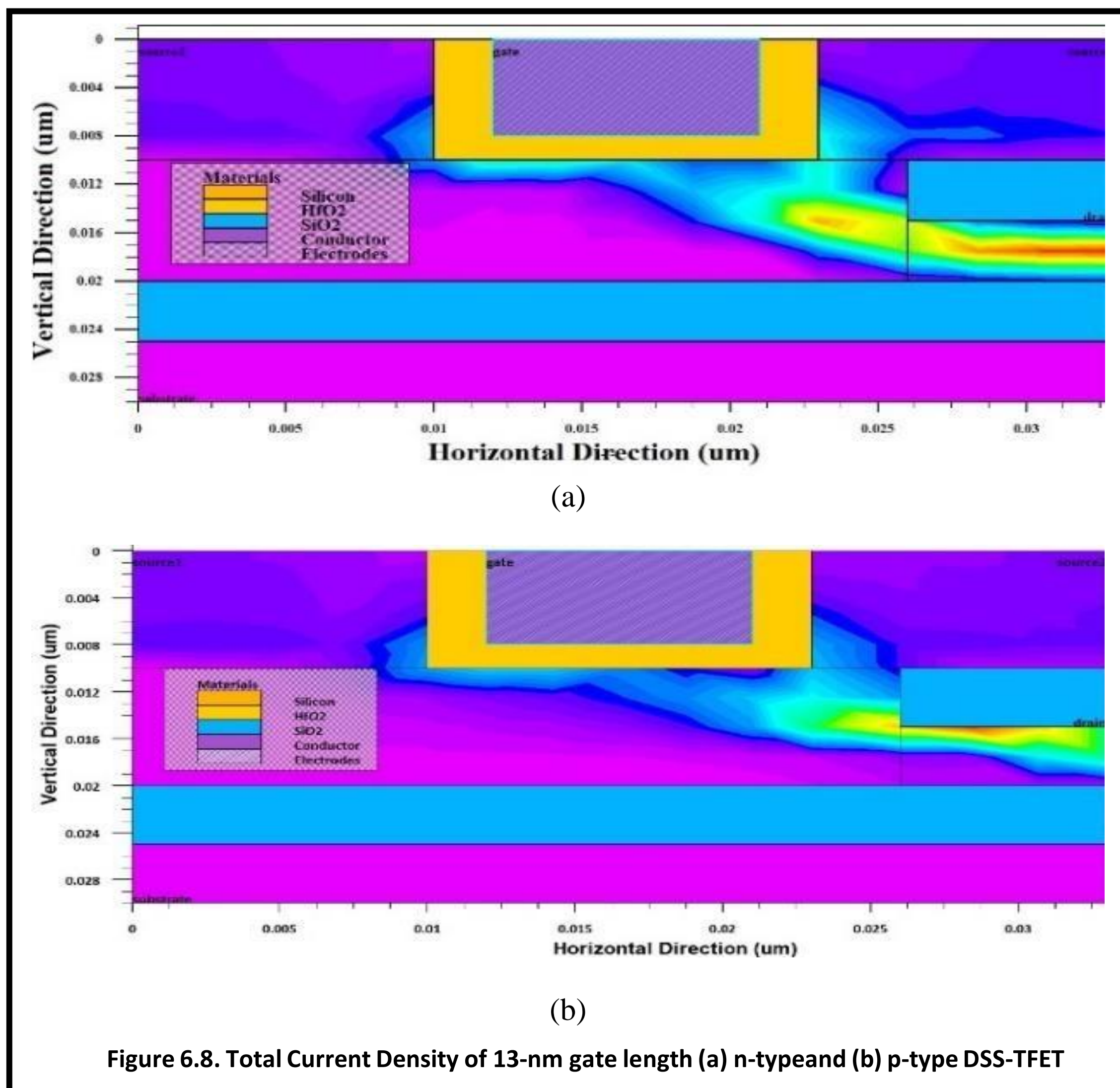
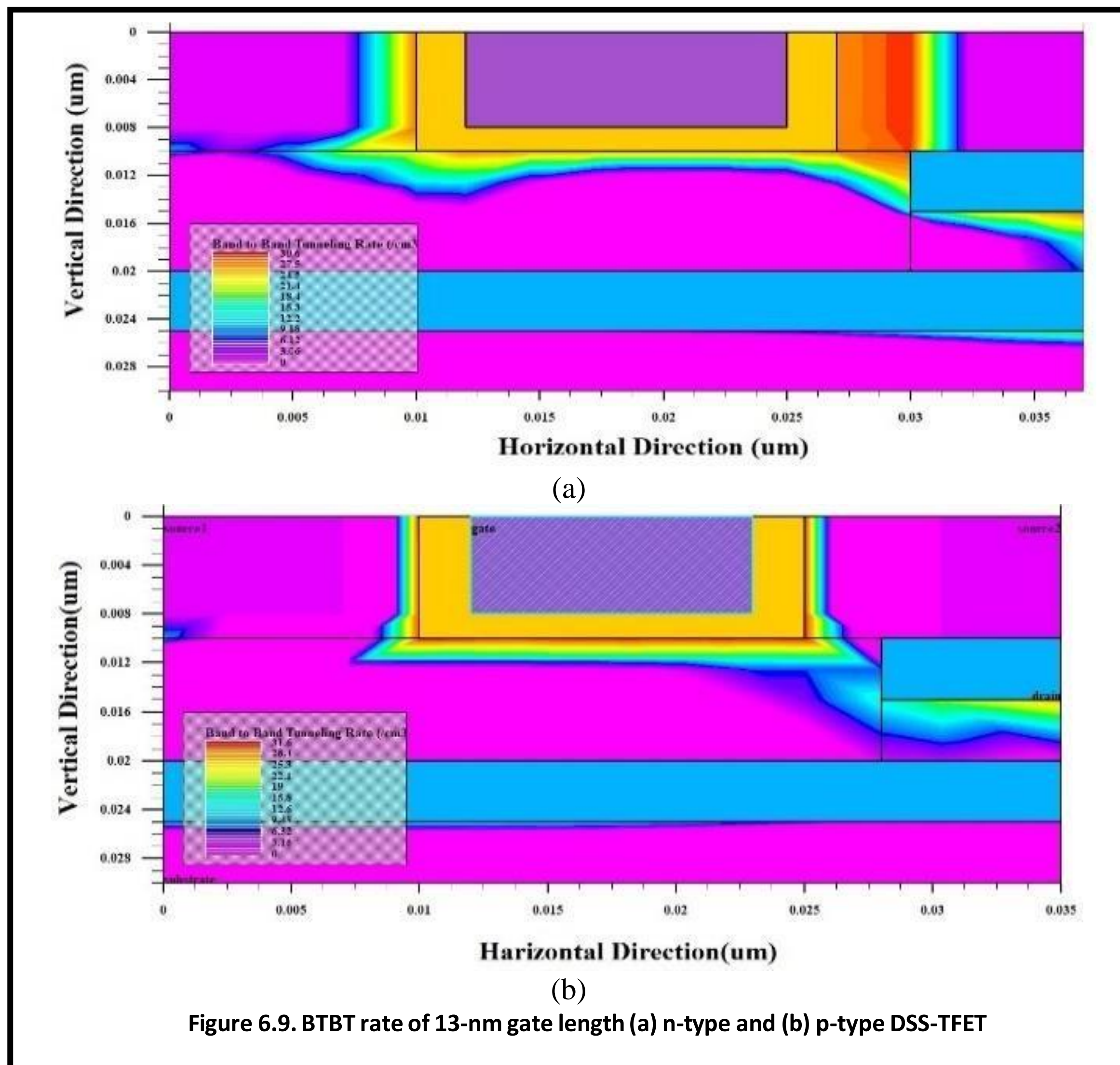


Figure 6.8. Total Current Density of 13-nm gate length (a) n-typeand (b) p-type DSS-TFET

Figs 8 and 9 show contour plots of total current densities for both DSS-TFETs. The tunnelling may be seen coming from both the source and channel junctions. Tunneling is more common between source-2 and channel junction than between source-1 and channel junction.

This is due to the fact that the drain is located directly under the source- 2. So, for this DSS-TFET, source 2 can be regarded the main source. Source-1 is acting as a buried source, providing additional bust to enhance I_{ON} and therefore give device structural stability, as evidenced by the low fluctuation in slope of the transfer characteristics displayed in Fig 2. Fig 7. depict BTBT for both the DSS-TFETs at a 13-nm gate length, where source-2 functions as the principal source and source-1 acts as a buried source to offer added bust to tunnelling processes.



(a)

(b)

Figure 6.9. BTBT rate of 13-nm gate length (a) n-type and (b) p-type DSS-TFET

6.4.5 Output Characteristics of proposed DSS-TFETs

Fig 10 shows the output characteristics of p-type and n-type DSS-TFETs at various V_{GS}. When compared to the current of a p-type DSS-TFET at the same V_{GS}, the n-type DSS-TFET has approximately three times the amplification. As a result, the width of the source of p-type DSS-TFET must be expanded by three times [12] in order to obtain the same amplification for an appropriate inverter design.

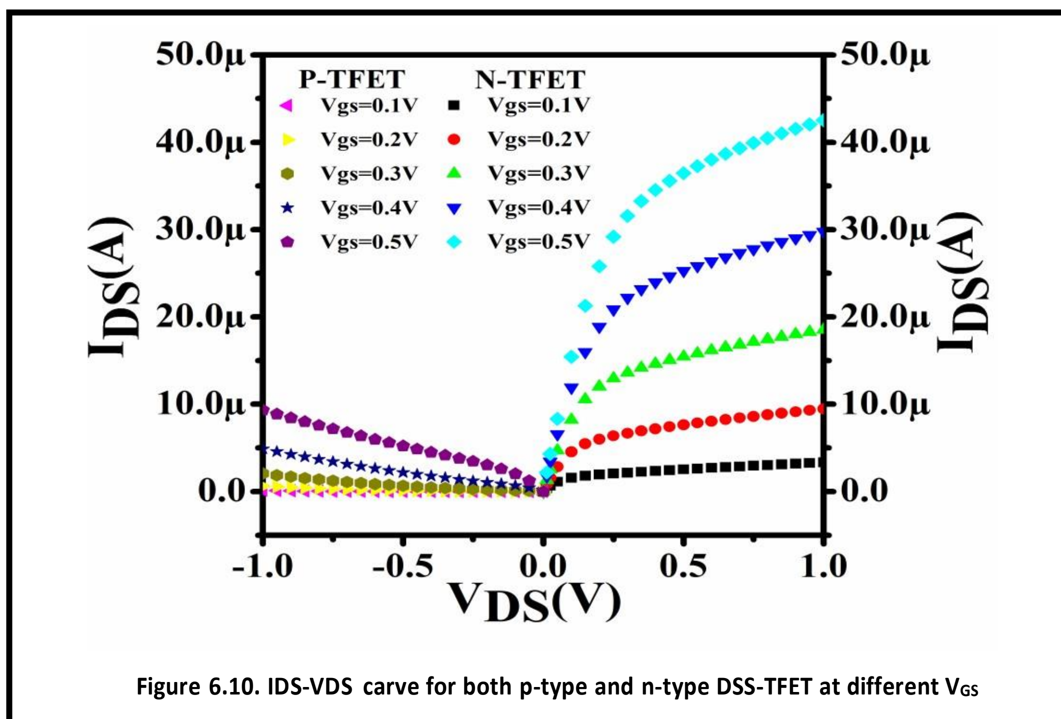
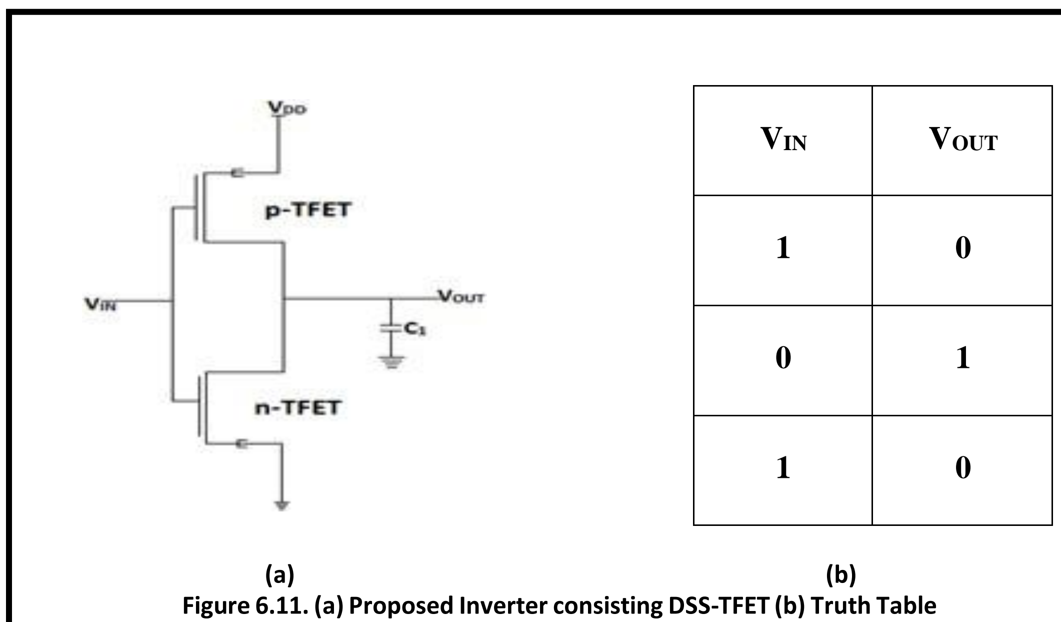


Figure 6.10. IDS-VDS carve for both p-type and n-type DSS-TFET at different V_{GS}

6.4 Circuit-level Analysis



V_{IN}	V_{OUT}
1	0
0	1
1	0

(a) (b)

Figure 6.11. (a) Proposed Inverter consisting DSS-TFET (b) Truth Table

A basic digital inverter using the proposed n and p-type DSS-TFETs has been designed. In order to test the feasibility of the proposed devices in circuit applications, two sets of lookup tables of current and capacitances which includes I_{DS} (V_{GS}- V_{DS}), C_{GD} (V_{GS}- V_{DS}), C_{GS} (V_{GS}- V_{DS}) are constructed using the data exported from SILVACO TCAD. The lookup tables are then implemented in SPICE with the help of Verilog-A model. At first the inverter is investigated thoroughly with the help of these models. Then, logic gates such as NAND and

NOR, have been designed and investigated in terms of power and delay at a particular supply voltage.

Figure 6.11(b) depicts the inverter's schematic. Both transistors have a channel length of 13 nm. The n-TFET transistor has a width of 10 nm, whereas the p-TFET transistor has a width of 30 nm [6.17]. With a supply voltage ranging from 0.2 V to 0.5 V, the inverter circuit's DC performance is measured in terms of noise margin (NM). The noise margin is the difference between the input and output thresholds.

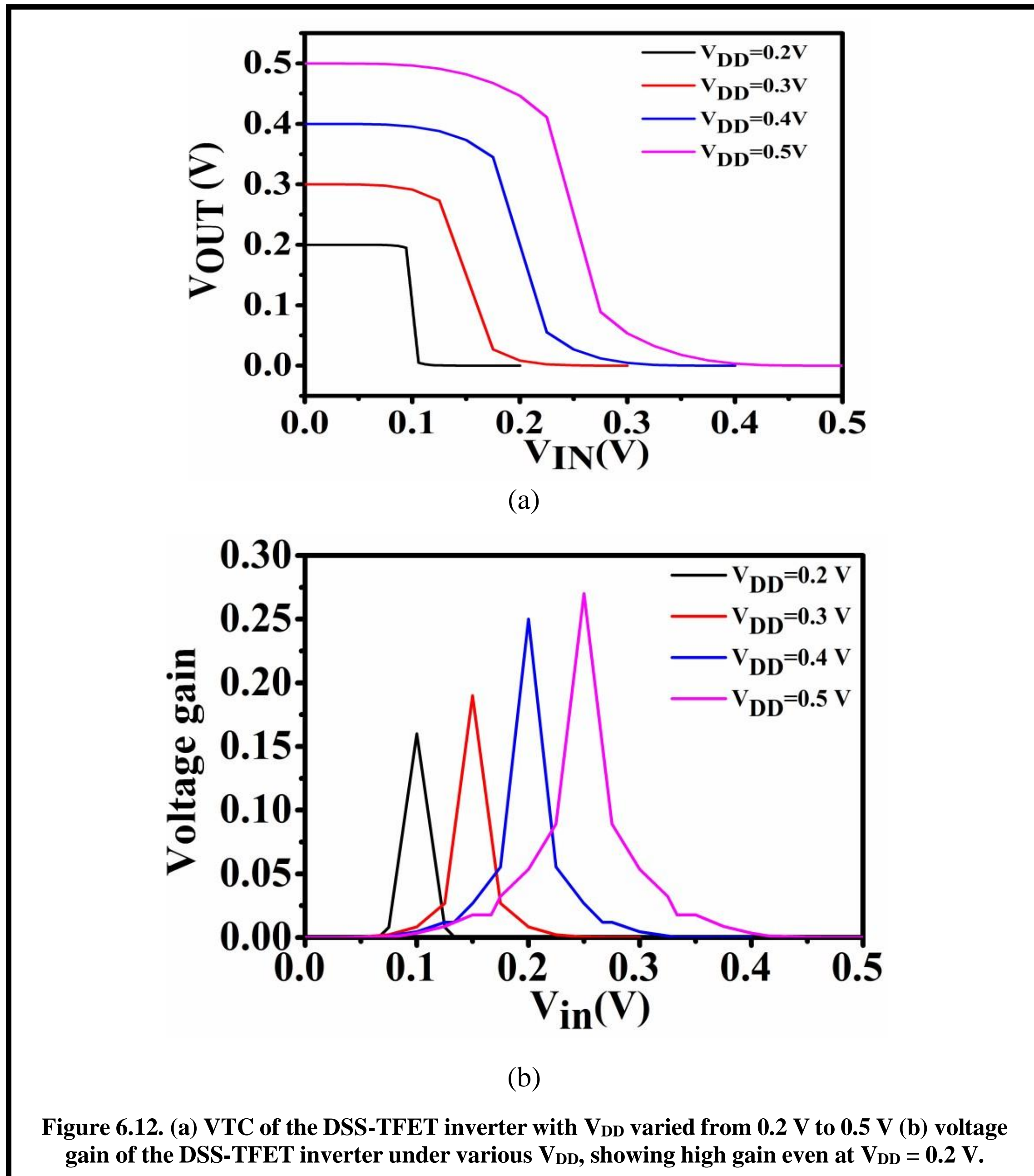


Figure 6.12. (a) VTC of the DSS-TFET inverter with V_{DD} varied from 0.2 V to 0.5 V (b) voltage gain of the DSS-TFET inverter under various V_{DD}, showing high gain even at V_{DD} = 0.2 V.

According to figure 6.12. (a), as V_{DD} decreases, the proposed inverter's VTC shape approaches that of a perfect CMOS inverter, and at V_{DD}=0.2V, it is nearly identical to a CMOS inverter. This is due to the fact that as electric field increases the gate lies in the linear region and when the gate moves in the saturation or in the deep saturation region and that leads to degradation of mobility of the carriers and degrades the performance of the device and deviates from ideality. When the V_{DD} is more, the depletion capacitance at the drain side is expected to be more, and that gives rise to increase rise time and fall time. That leads to non-ideality with the variation of V_{DD}The simulated VTC indicates that the inverter's transition voltage is approximately $V_{DD}/2$ and that the high and low levels are clearly separated, indicating that both devices are operational. The suggested inverter's voltage gain (V_{OUT}/V_{IN}) is shown in Figure 6.12. (b). Because of the higher I_{ON} and improved ambipolarity, a voltage gain of 16 is nevertheless attained at V_{DD}=0.2V, indicating a great potential for low power applications [6.17- 6.18].

Figure 6.13 illustrates the VTC of the proposed DSS-TFET inverter at V_{DD}=0.2V in order to evaluate the noise margin. The values V_{IL} and V_{IH} represent the input voltages for which the inverter's voltage gain dV_{OUT}/dV_{IN} =-1. The output voltages V_{OL} and V_{OH} may also be determined from the transfer characteristics by taking into account the minimum and maximum voltage values. The formulae below can be used to determine the low noise margin (NM_L) and high noise margin (NM_H),

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

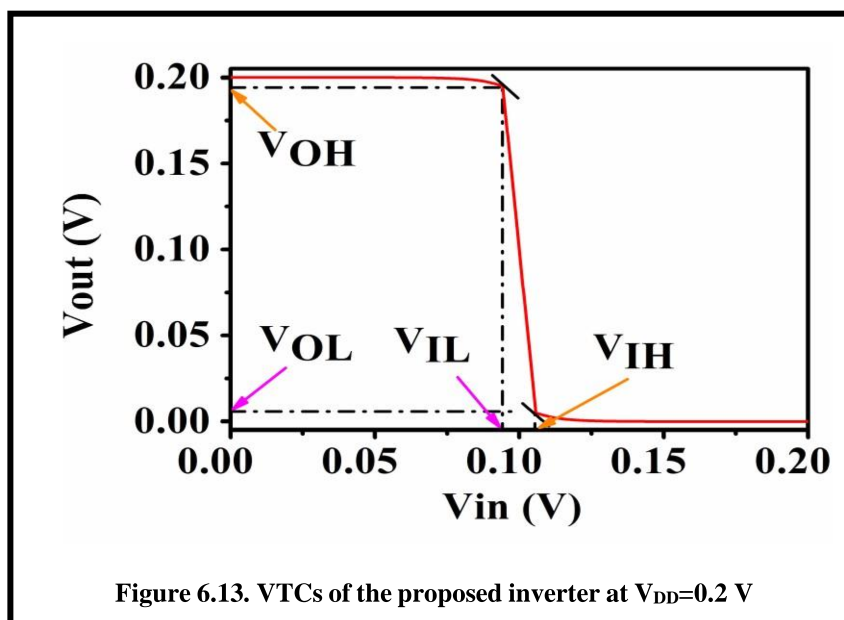


Figure 6.13. VTCs of the proposed inverter at V_{DD}=0.2 V

Parameters	DC value
V_{IL}	94.31mV
V_{OL}	4.99 mV
V_{IH}	105.75mV
V_{OH}	194mV
$NM_L=V_{IL}-V_{OL}$	89.32mV
$NM_H= V_{OH}-V_{IH}$	88.25mV

Table 6.1. Different DC parameters of the inverter based on our proposed structure of TFET

Table 6.1 lists the DC parameters associated to VTC. The proposed inverter has a high to low noise margin around 97% at V_{DD}=0.2 volt, which indicates that it almost behaves like an Ideal CMOS inverter.

The operation of the NOT gate has been performed at a supply voltage V_{DD}=0.2 Volts. The output of the NOT gate is depicted in figure 6.14. The input A has been considered as 101 and as an output 010 has been achieved, which is nothing but the truth table of NOT gate figure 6.

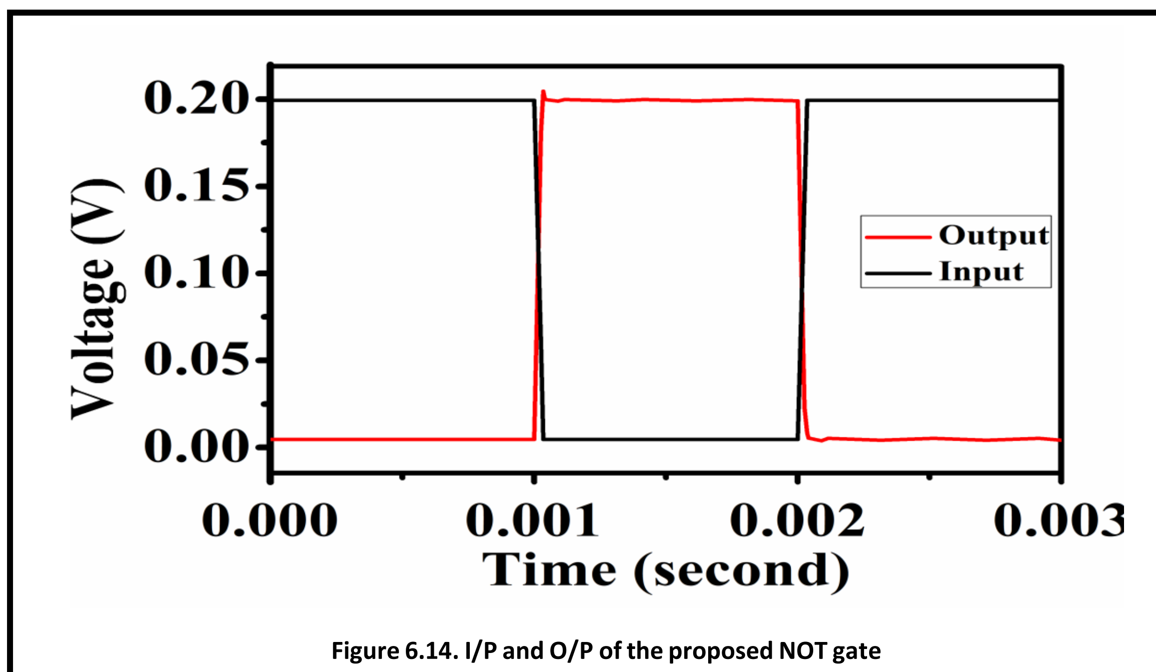


Figure 6.14. I/P and O/P of the proposed NOT gate

11(a). Delay (T_d) and power dissipation (pd) has been measured and also compared [19] with the existing TFETs which have been provided in Table – 1.

Device	pd	T_d
Proposed TFET	**1.69.nW**	**19.13ps**
Compared TFET [19]	**86nW**	**36.41ps**

Table 6.2. Calculated the power of the inverter based on our proposed structure of TFET.

Similarly, a two-input NAND gate has been designed and investigated at a V_{DD}=0.2V. The circuit diagram and the truth table has been depicted in figure 6.15. For performance analysis, the first input (A) has been considered as 0011 and the second input (B) as 0101. The achieved output is 1110 which can be noticed in figure 6.16. T_d and pd of the proposed NAND gate has also been compared with existing TFET based NAND gates [36] and is being provided in table – 2.

It is evident from table -2, that the proposed NAND gate is superior in terms of T_d, but pd is more as compared to existing TFET. However, in terms of PDP the proposed NAND gate ($3.65x10^{-19}$J) is superior than compared NAND gate ($2x10^{-18}$J).

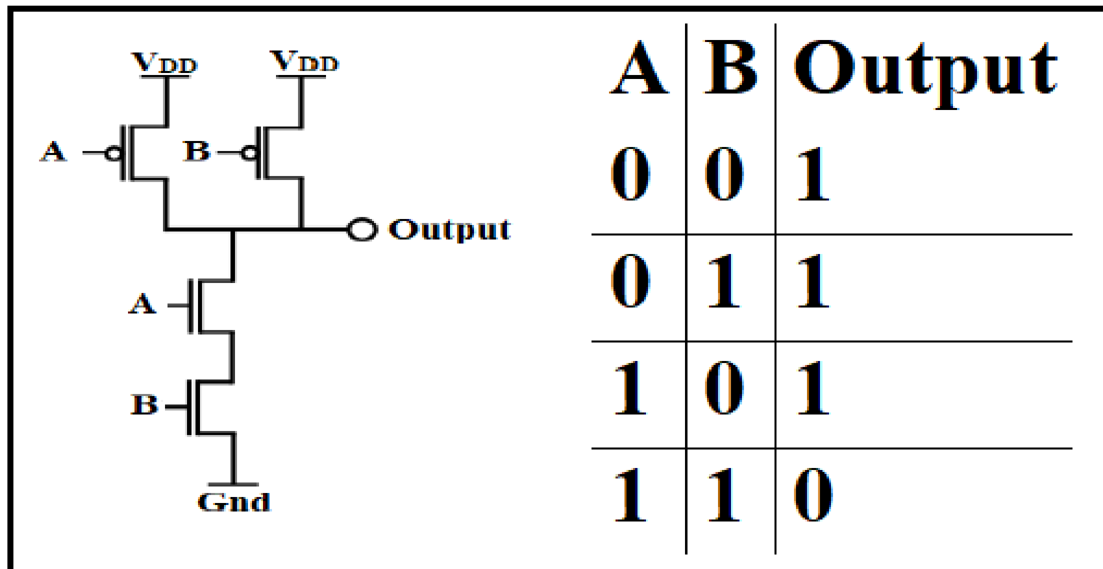


Figure 6.15. NAND gate (a) circuit connection (b) Truth Table

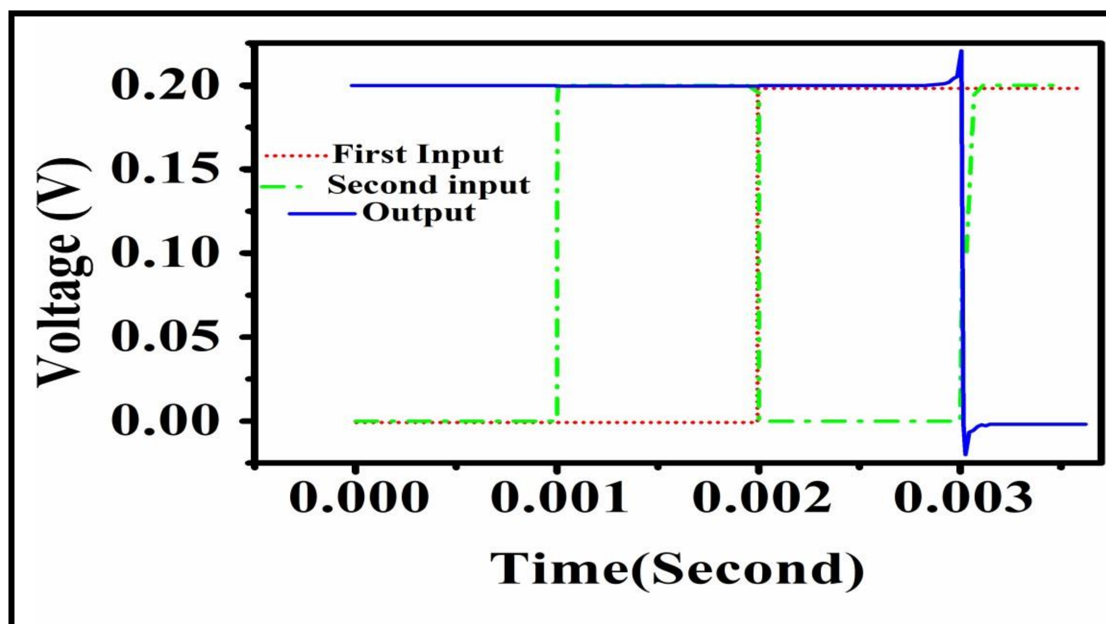


Figure 6.16. I/P and O/P of the proposed NAND gate

Device	pd	T_d
Proposed TFET	15.8nW	23.13ps
Compared TFET [20]	79.46pW	25.23ns

Table 6.3. Power-delay comparison of the proposed and compared NAND gates

Implementation of two i/p NOR gate has been done as per the circuit diagram shown in figure 6.17(a). A V_{DD} of 0.2V has been considered for the logic gate study. The first input has been taken as 0011 and the second input has been considered as 0101 and the achieved output is 0001 which is nothing but the truth table of a NOR gate which is shown in Figure 6.17(b). Figure 6.18. shows the i/p – o/p characteristics of the proposed NOR gate.

The achieved T_d and pd also been compared with the existing TFET-based NOR gate [36] and the results are given in table-3. It is evident that the proposed NOR gate has consumed more power than the compared NOR gate. But the proposed NOR gate is superior when the delay is considered. Therefore, in terms of PDP, the proposed NOR gate (3.55×10^{-19}J) is better in performance than the compared NOR gate (4×10^{-19}J).

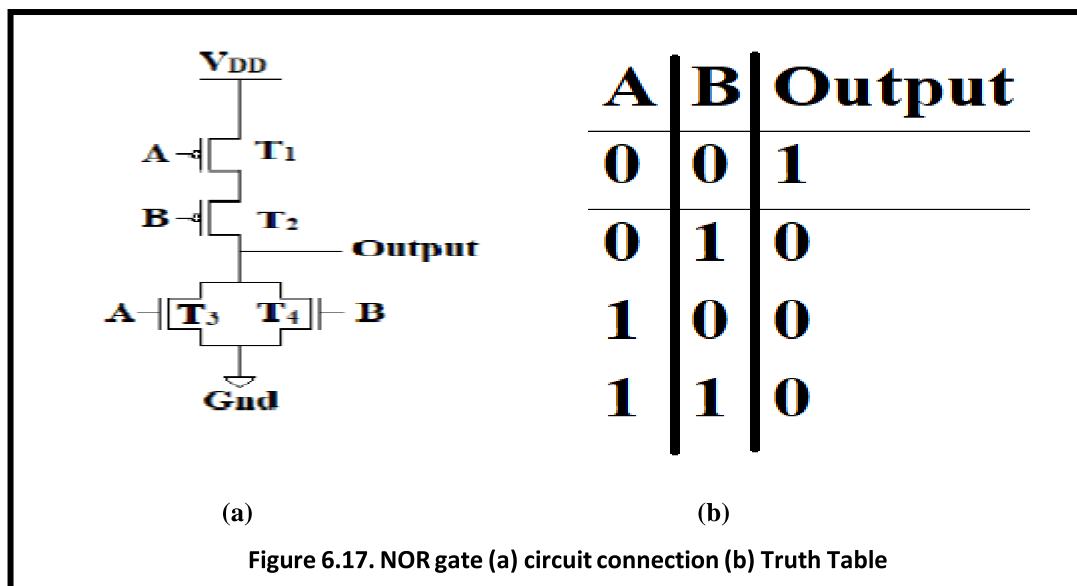


Figure 6.17. NOR gate (a) circuit connection (b) Truth Table

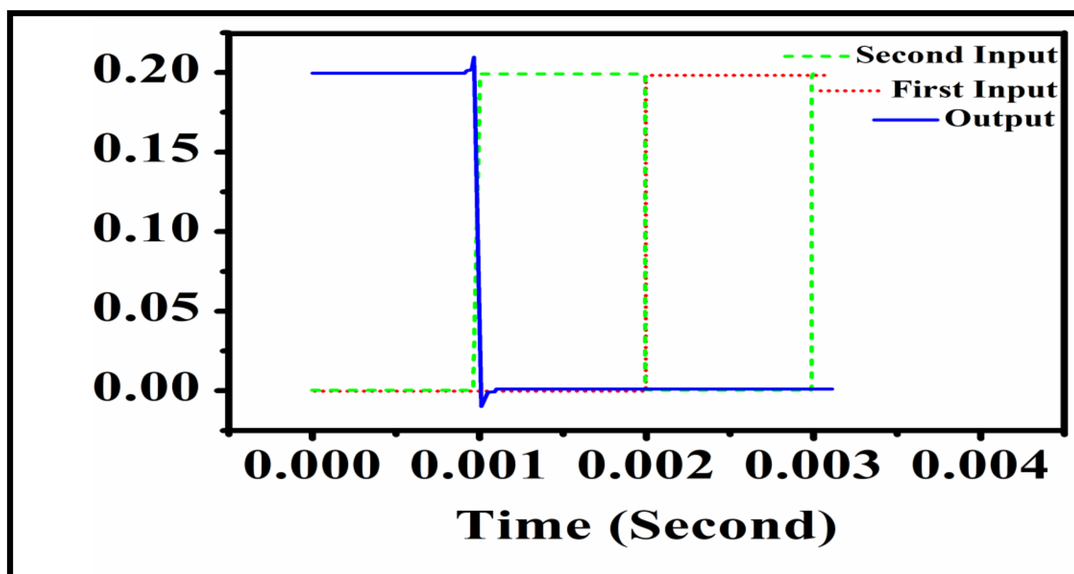


Figure 6.18. I/P and O/P of the proposed NOR gate.

Device	*pd*	T_d
Proposed TFET	**18.5nW**	**19.23ps**
Compared TFET [36]	**3.01nW**	**132.71ps**

Table 6.4. Power-delay comparison of the proposed and compared NOR gates

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Chapter:7

Chapter-7: Gate Centric Extended Source SOI-TFET for Low Power Circuit Application

7.1 Introduction 196
7.2 Literature Survey 197
7.3 Device structure and Parameters 201
7.4 Simulation Setup and Model Descriptions 202
7.5 Tunneling Mechanism 203
7.5.1 Point Tunneling 203
7.5.2 Line Tunneling 205
7.6 Results and discussions 207
7.6.1 Optimum VDS 207
7.6.2 Centric Source Extension 207
7.6.3 Position of Source and Drain Contact 208
7.6.4 Band Diagram 209
7.6.5 Electric Field 209
7.6.6 Surface Potential 210
7.6.7 Transfer Characteristics 210
7.7 Quantum Confinement 211
7.7.1 Transfer Characteristics 211
7.7.2 Electron Concentration 212
7.7.3 Comparison of Subthreshold Slope 213
7.8 GCES SOI TFET Inverter 214
References 216

7.1 Introduction

In the last decade, there has been gradual deduction in the dimension of the devices, and deduction of dimension leads to the short channel effect (SCE) in MOSFET. Researchers tried to overcome those SCE to improve the performance of the devices. However, all these problems have not been solved, partially they are been mitigated but fully it is not been possible. Moreover, the MOSFET is little power consumption. Several techniques such as silicon-on-insulator (SOIs), nanowire devices, and FinFETs devices are used to improve device performance. However, this device engineering encourages parasitic resistance and enhances the process complexity. Further, the drift-diffusion current of the device is the main difficulty

that essentially confines scaling supply voltage and power dissipation. Tunnel Field Effect Transistor (TFET), a non-conventional device with almost similar geometry, has emerged in the research lime limelight possible successor for bulk MOSFET, so to overcome the SCE and can reduce the power dissipation. Tunnel FET working on the principle of band-to-band tunneling mechanism through a barrier instead of modulating thermionic emission over a barrier as in traditional MOSFETs, has the advantages of going below the limit of 60mV/decade sub-threshold slope, yielding higher I_{ON}/I_{OFF} at lower V_{DD}, lower leakage current, and thus capable of reducing the power consumption, and achieving energy-efficient fast switching transistors. Conventional TFET devices exhibit low I_{ON} which can be improved by modifying the device dimension, doping concentration etc. Si-based TFET structures are advantageous over other new material variations as they are consistent and can be integrated with CMOS processes. Also In order to increase the I_{ON} of TFETs, structural modification needs to be incorporated into a conventional TFET so that both Point tunnelling and line tunnelling the two principle tunnelling mechanism will occur. Point tunneling is the most common type of carrier generation method in a TFET. The maximum carrier generation rate is almost confined to a point and occurred mainly at the source-channel junction region, in which the carriers at the high energy tail of the Fermi–Dirac distribution are filtered by a tunneling window and it gives the prime contribution is localized in a small area. However, for line tunnelling, a gate overlap region needs to be created over the source region. The electric field thus formed has to be in a direction that aids tunnelling. The electrons from the inner parts of the source tunnel to the inversion region formed near the surface of the source (for n-TFET). The carrier generation takes place in a line, near the source-gate oxide interface, hence the name is line tunnelling. Since the carrier generation, area/ dimension is larger than point tunnelling, the I_{ON} increases. As subthreshold current is not limited by the Boltzmann distribution of the carrier, an ultra-steep SS of less than 60 mV/dec at room temperature can theoretically be obtained, resulting in high on- I_{ON}/I_{OFF} ratios at low voltages. TFET can also operate with a larger transconductance to-current ratio than traditional FET in the sub-threshold region [4.7]. In addition, the higher output resistance offered by TFET-based designs allows for achieving significantly higher intrinsic voltage gain and higher maximum-oscillation frequency at low current levels. Moreover, TFET- exhibits superior performance advantages in track-and-hold [4.8], ambient radio-frequency power scavenging [4.9], and digital to analog converter [4.10]. All these findings indicate that the TFET has a good application prospect in

low-power devices [4.11]. However, due to the characteristics of the structure in the TFET, there are still some challenges in circuit design using TFETs.

7.2 Literature Survey

Tunnel field-effect transistors are potential successors of metal-oxide-semiconductor FETs because they promise characteristics though in general have low ON current. Also, the output characteristics of TFETs are poorly understood, and sometimes a superliner onset is undesirable for circuit design. The TFET current can be decomposed into two components referred to as point tunneling and line tunneling. Several device structures [7.1-7.5] have been proposed and fabricated to study the impact of point tunneling and line tunneling such as source extension which increases tunneling area by incorporating line tunneling along with point tunneling due to source gate overlap on TFETs.

Sharmistha et al [7.1] present the quantum analytical model, based on the 1-D Schrödinger equation and 2-D Poisson's equation for a DMDG silicon-on-nothing MOSFET structure and analyze the QMEs on device performance like the electric field, transconductance, drain conductance, and voltage gain.

Upasana et al [7.2] used the Lambert-W function to formulate a drain current model for Double Gate (DG) p-n-i-n Tunnel FET (TFET) which includes the impact of mobile charges, gate dielectric thickness, and channel thickness on quasi fermi level, gate threshold voltage (VTG), onset voltage and Tunneling Barrier Width (TBW) over the entire operating range i.e. accumulation to inversion state.

Padilla et al [7.3] analysis of an Heterogate EHBTFET with partially doped channels to verify the effects on TDM and occupancy probabilities.

Kumar et al[7.4] proposed a compact analytical model for electrical characteristics of DG TFETs with a SiO_2/High-k stacked gate-oxide structure resulting in higher I_{ON} at lower V_{DS}

Alper et al [7.5] validate a design methodology for logic circuits that exploit the conduction mechanism and the presence of two independently biased gates ("n-gate" and "p-gate") of the EHB-TFET. It is designed to conduct under certain conditions and allowed to implement certain logic gates having less number of transistors compared to a conventional CMOS logic.

Bhattacharjee et al[7.6] proposed analytical modeling and simulation of drain doping engineered splitted drain structured TFET. The splitted drain structure exhibits a major reduction in ambipolar conduction due to an increase of the tunnelling width at the channel-drain junction.

Kumar et al[7.7] had developed an analytical model of surface potential, electric field, drain current shows better SS and V_{th} on a DM-DG-TFETs with SiO2/HfO2 stacked gate-oxide structure.

Saheli et al [7.8] incorporated the concept of gate engineering, by continuously varying mole fraction in a BMA gate electrode along the horizontal direction into a conventional TFET. The buried oxide layer helps to tune the barrier at the source-channel junction, thus enhancing BTBT at a significant rate, thereby increasing I_{ON}.

M. Kimet et al [7.9] demonstrate the SS of Si-NWTFETs by varying both the channel diameter from 10 nm to 40 nm and the gate coverage ratio from 30% to 100%. Si-NWTFETs show that the magnitude of the I_{ON} depends linearly on the gate coverage ratio and that the I_{DS} increases with a decrease in the channel diameter.

M. Lee et al[7.10] obtained p-i-n configured SiNWs from a Si wafer using a conventional top-down CMOS-compatible technology and then transferred them onto the SiNW-based TFET on flexible plastic substrates.

Khatami et al [7.11] proposed n- and p-type TFETs based on heterostructure Si/intrinsic-SiGe channel layer, which exhibit very small SS, as well as low V_{TH} .This TFET exhibit extremely low I_{OFF} on the order of 1 fA and is substantially higher I_{ON} compared to conventional TFET devices.

Krishnamohan, et al [7.12], demonstrated a Double-Gate strained-Ge heterostructure TFET that exhibits very high I_{ON} and less SS, due to the small bandgap of the strained-Ge heterostructure TFET.

Wirthset et al [7.13] propose two low direct bandgap group IV compounds, GeSn and highly tensely strained Ge in combination with ternary SiGeSn alloyed TFET where strained Ge acts as a channel and Ge1−xSnx source, resulting in a direct bandgap engineering, significantly increases the tunneling probability.

Ram et al [7.14] demonstrated that the energy bandgap on the source side can be modulated to create an N + source pocket using a DM-gate in doping less PNPN TFET with a hetero-gate dielectric for low power and low-cost applications.

Abdi et al [7.15] use the charge plasma technique to realize an in-built N+ pocket without the need for separate implantation as an N+ pocket increase the fabrication complexity.

Ahish et al [7.16] investigated the effects of uniform and Gaussian drain doping profiles on the dc characteristics as well on analog/RF performances for different channel lengths TFETs.

Sola et al [7.17] propose CSC-TFETs with trench gate structures. The CSC-TFET inverter was implemented which results in a high frequency compare to convention TFET.

Hongliang et al [7.18] combined energy-band engineering of InAs/Si heterojunction and source-pocket concept in a single TFET to extensively boost the I_{ON} as compared to a conventional TFET.

Vandenberghe et al [7.18], show that there are two current components in a TFET which are referred to as point tunneling and line tunneling. Also he proposed an analytical model for point and line tunneling in a TFET devices.

Verhulst, et al [7. 20] implement the impact of the drain voltage on the TFET performance by analyzing an analytical model, as TFETs output characteristics of are poorly understood and sometimes a superlinear onset, undesirable for circuit design.

This source-gate overlap in the low dimensional device may cause SCE like DIBL and to avoid the same such specific region variation has been considered. The gate length of the proposed structure has been varied and output characteristics have been examined by performing simulations using Silvaco, Atlas. Simulations are performed considering quantum and without quantum effects and a comparative study of both has been presented in this work. Source and gate overlap regions create a modification in the understanding of tunneling at source and channel junctions. The area covered includes line tunneling as well as point tunneling [7.21] at the mentioned interface.

When quantum effects [7.22] are considered in device operation, the conduction and valence energy bands no more remain continuous and become a discrete spectrum of energy. Therefore tunneling will only be possible between the first energy states available for electrons and holes. This results in an increase in tunneling width that causes a reduction in BTBT probability along with a reduction in ON current.

Going to implementing any digital/analog application, the basic requirement is to design an inverter. But to comply with the CMOS characteristics on a TFET, both N-TFET and

P-TFET should be designed properly by suppressing the ambipolar current for complementary performance [7.23-7.26].

7.3 Device Structures and Parameters

Gate Centric Extended Source SOI TFET structure has been considered in this work. The proposed structure shown in figure 7.1 has an extended source part which overlaps under the trench gate. Channel region is intrinsic and the effective channel length increases due to the LDD. Two different oxides namely HfO_2 and SiO_2 have been used as gate dielectric. As the proposed structure has a trench gate, therefore the dielectric covers three sides of the gate as shown in the figure 7.1 The source along with its extended portion is of P^+ type with doping

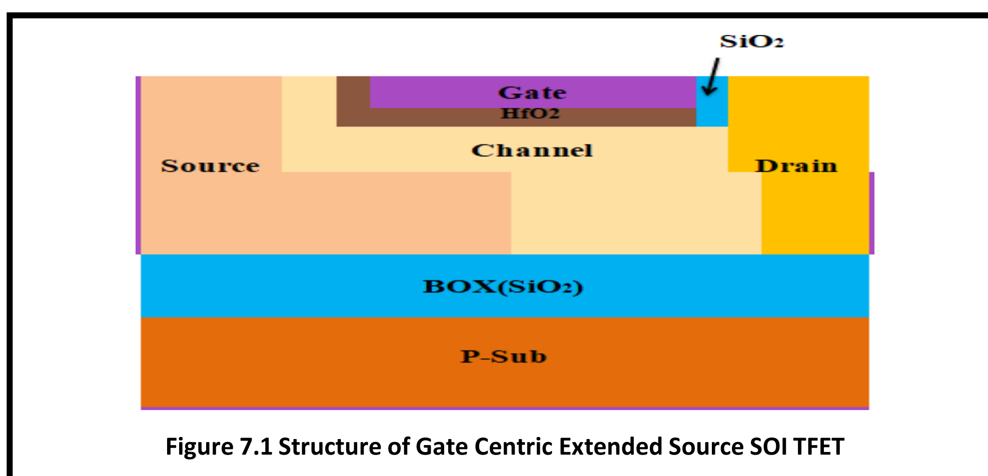


Figure 7.1 Structure of Gate Centric Extended Source SOI TFET

concentration of 10^{20} cm^{-3} whereas drain doping is of N-type with concentration of 10^{17} cm^{-3}. The channel region as well as the lower-left part of drain is kept intrinsic (10^{12} cm^{-3}). A P type substrate below the buried oxide (SiO2) layer is considered for the proposed SOI structure in order to ease the process of fabrication as well as to avail other advantages offered by SOI such as less parasitic capacitance, less leakage current, more firm and stable structure. The work function of gate of the device has been considered as 4.85eV.

The device has three variations in gate length specifically 10nm, 7nm and 5nm. For 10 nm gate, length source region has a dimension of 12 nm × 10 nm with an extended part of area 7 nm × 5 nm. The drain has a low-doped intrinsic segment at the lower left part with dimension of 2 nm × 5 nm whereas the upper part of this segment has higher doping concentration and dimension same as the lower one. The rest of the drain has a dimension of 10 nm × 10 nm. Channel starts from the left side of trench gate, goes underneath the gate till the low-doped intrinsic drain segment. Gate oxide SiO_2 is 2 nm thick and has a dimension of 2 nm × 2 nm at

the left part of gate and 10 nm × 2 nm under the gate. HfO_2 on the other hand is present at the right of gate having dimension of 2 nm × 2 nm. The trench gate is 1nm deep and has a variation in length of 10 nm, 7 nm and 5 nm. The objective of this gate length variation is to investigate the suitable gate length for such small dimensional device structure.

Fabrication of the proposed device requires growing the structure layer by layer on top of silicon substrate. SiO_2 (BOX) layer can be grown on P type Si substrate by the method of oxidation. An intrinsic layer of Si is deposited on top of it. This layer is doped (left side P type for source and right side N type for drain) by the process of proper masking according to specific regions followed by diffusion of dopants. The same procedures of Si deposition, masking and diffusion could be carried out in accordance with specific region definition that would work as source, channel and drain. The channel region is then etched by photolithographic process and oxides (HfO2 and SiO2) are deposited in the etched area. The oxide is then etched according to its thickness required and gate metal is deposited in the etched area forming a trench gate structure. Source and drain contacts are at the two sides of the device along with one body contact below the substrate. Gate contact is taken from the top of the device on the gate metal. The fabrication steps are briefly illustrated in the figure 7.2.

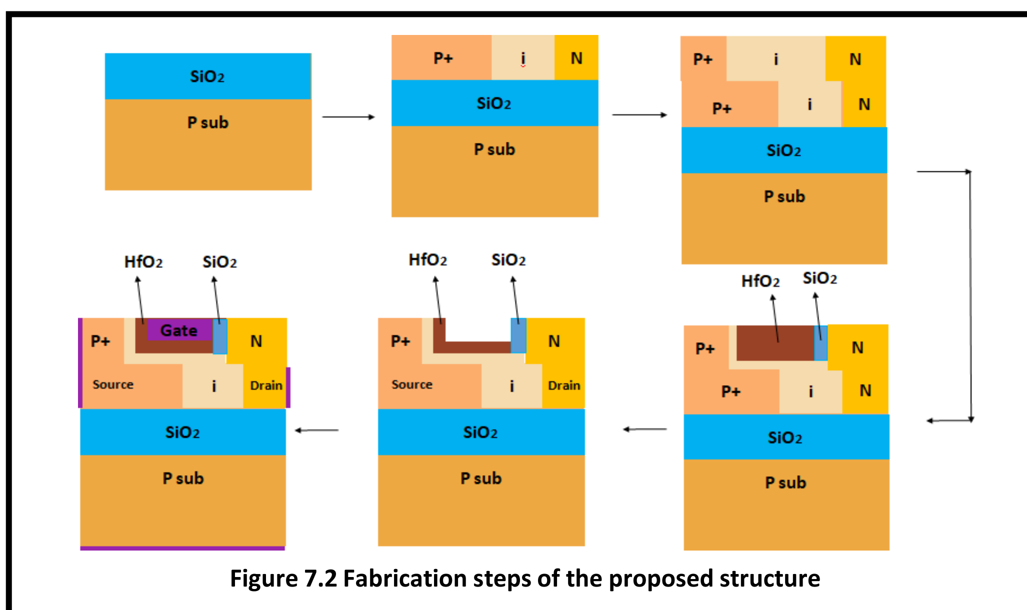


Figure 7.2 Fabrication steps of the proposed structure

7.4 Simulation Setup And Model Descriptions

Silvaco Atlas based simulation has been performed considering quantum mechanical description along with quantization in sub-band transition using self-consistent Schrodinger Poisson model and classical model simulation that includes non-local BTBT, bandgap

narrowing model, Fermi Dirac statistics, Auger and SRH (Shockley Read Hall) recombination models.

7.5 Tunneling Mechanism

The rate of generation can be calculated using Kane's model for known tunneling distance and is given by

$$G = A\frac{E_G^{D-1/2}}{q^D l^D}\exp(-Bq\sqrt{E_G}l) \tag{1}$$

Integrating this generation rate over the entire volume we get the total current as

$$I = q\int GdV \tag{2}$$

7.5.1 Point Tunneling

Now for the proposed structure we assume the following boundary conditions. Also the charge density $\rho = 0$ at the gate oxide and intrinsic semiconductor. Hence the Poisson's equation $\nabla^2\psi = -\frac{\rho}{\varepsilon_s}$ reduces to Laplace equation $\nabla^2\psi = 0$.

For an applied gate voltage we have $\psi_g = V_{gs} - V_{FB}$ and we considered $\psi_s = 0$ where V_{FB} is Flat band voltage. We assume the semiconductor extending to infinity by taking x>0 and z>0 and hence potential for point tunneling can easily be calculated using polar coordinates as it is evident from the curved electric field lines from source edge to gate depcted in figure7.3. Incorporating polar coordinates we assume x=rsinθ and z=rcosθ where θ ranges from 0 to π /2 (evident from figure 7.3)

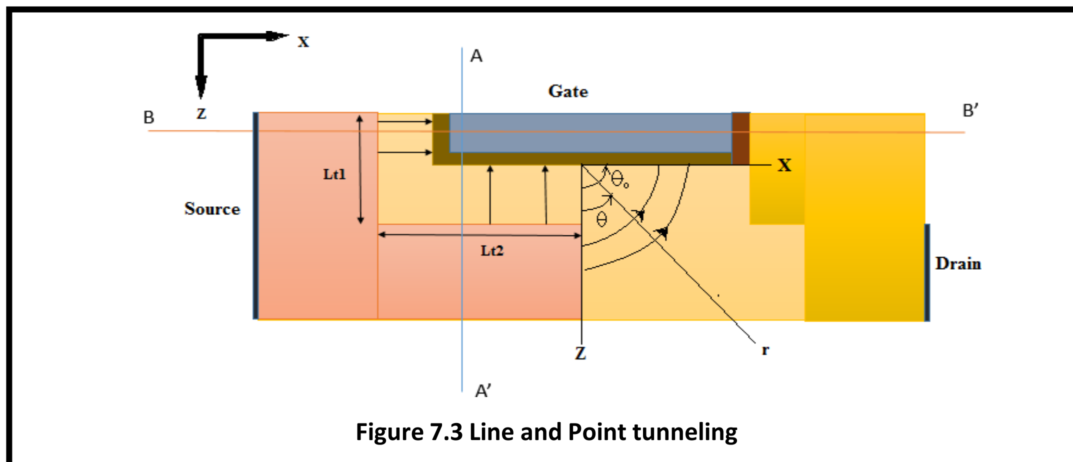


Figure 7.3 Line and Point tunneling

Hence $\psi(x,z) = \psi_g(\frac{2}{\pi}\theta)$ and tunneling path length can be calculated along the arc of electric field lines $l = r\theta_0$ where angle between equipotential lines $\theta_0 = \frac{\pi}{2}(\frac{E_g}{q})\frac{1}{\psi_g}$ as $\frac{E_g}{q}$ is the potential difference.

Now the total current for point tunneling can be calculated by integrating the generation rate from Kane's model over the entire tunneling area depicted in figure 7.3 and the same is given by

$$I = qW\int_{r_0}^{\infty}\int_{\theta_0}^{\cos^{-1}\frac{t'_{ox}}{r}} A\frac{E_G^{D-1/2}}{q^D (r\theta_0)^D}\exp(-Bq\sqrt{E_g}\, r\theta_0)\, r\,d\theta\, dr \tag{3}$$

Where $r_0 = t'_{ox}/\cos\theta_0$ and equivalent thickness of semiconductor $t'_{ox} = t_{ox}(\frac{\varepsilon_s}{\varepsilon_{ox}})$.

Integrating over θ and on simplification we get

$$I = AW\int_{r_0}^{\infty}\frac{E_G^{D-1/2}\, e^{(-Bq\sqrt{E_g}\, r\theta_0)}}{q^{D-1} r^{D-1}\theta_0^{D}}\left(\cos^{-1}\frac{t'_{ox}}{r}-\theta_0\right) r\,dr \tag{4}$$

Now first order Taylor expansion is performed to solve this integration around $r = r_0$ and we have

$$f(r) = f(r_0) + f'(r_0)(r-r_0) \tag{5}$$

Differentiating $f(r_0)$ with respect to r_0 and multiplying the same with $(r-r_0)$ we get

$$(r-r_0)f'(r_0) = \frac{WAE_G^{D-1/2}}{q^{D-1}r^{D-1}\theta_0^{D}}\begin{bmatrix} -\theta_0\, e^{(-Bq\sqrt{E_g}r_0\theta_0)} \\ -\frac{1}{\sqrt{1-\left(\frac{t'_{ox}}{r_0}\right)^2}}(r-r_0)\,e^{(-Bq\sqrt{E_g}r_0\theta_0)} \\ +\theta_0^{2}Bq\sqrt{E_g}(r-r_0)\,e^{(-Bq\sqrt{E_g}r_0\theta_0)} \\ -\theta_0(r-r_0)\,e^{(-Bq\sqrt{E_g}r_0\theta_0)} \end{bmatrix} \tag{6}$$

Here we have assumed $\cos\theta_0 = 1$ and therefore $\cos^{-1}\frac{t'_{ox}}{r_0}$ is 0. Again this implies $\theta_0 = 0$ and the equation for I reduces to

$$I \approx \frac{WAE_G^{D-1/2}}{q^{D-1} r^{D-1} \theta_0^D} \int_{r_0}^{\infty} \left[\frac{t'_{ox}(r-r_0)\, e^{(-Bq\sqrt{E_g} r_0 \theta_0)}}{\sqrt{1-\left(\frac{t'_{ox}}{r_0}\right)^2 r_0}} dr \right] \tag{7}$$

The integration with respect to dr is solved and simplified as

$$I \approx \frac{WAE_G^{D-3/2} t'_{ox}}{q^{D-1} B^2} \frac{1}{\theta_0^{D+2} r^{D+1}} e^{(-Bq\sqrt{E_g} r_0 \theta_0)} \tag{8}$$

We know for small value of θ, sinθ ≈θ. Hence it can be written that

$$\cos\theta_0 = \sin\left(\frac{\pi}{2} - \theta_0\right)$$

r_0 can be approximated as the function of gate voltage which can be expressed as

$$r_0 = t'_{ox} / \sin\left(\frac{\pi(q\psi_g - E_G)}{2q\psi_g}\right) = \sin\left(\frac{\pi}{2} - \frac{\pi E_G}{2q\psi_g}\right) \tag{9}$$

Hence $\theta_0 = \frac{\pi E_G}{2q\psi_g}$ and taking the value of D=2 as the default value the expression of the current due to point tunneling is found to be

$$I_p = W \frac{2A\sqrt{E_G}}{\pi q^3 B^2 t'^2_{ox}} \frac{q\psi_g}{E_G} \left(\frac{q\psi_g}{E_G} - 1\right)^2 e^{\frac{-Bq\sqrt{E_g} t'_{ox}}{\left(\frac{q\psi_g}{E_G}-1\right)}} \tag{10}$$

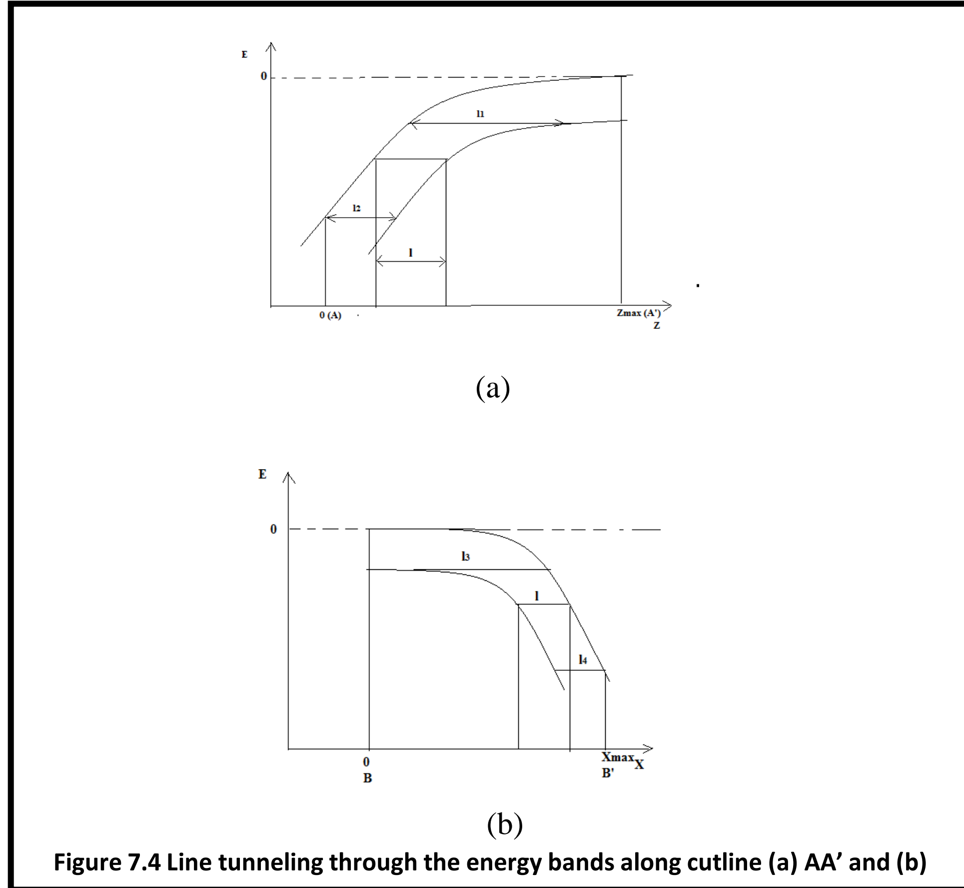
7.5.2 Line Tunneling

Line tunneling occurs at the area where gate and source overlap. As the gate is trench gate therefore line tunneling will occur in two directions along Lt1 and Lt2 shown in figure 7.4. Line tunneling along two cut lines with the band diagrams are shown below:

From [10] the line tunneling current is calculated for the region L_{t1} and L_{t2} as the integration over total BTBT generation of charge which is given by

$$I_l = \frac{qWLA}{2}\left[\int_{l_1}^{l_2} P(l)dl + \int_{l_3}^{l_4} P(l)dl\right] \tag{11}$$

Where $P(l) = \frac{E_G^{D-1/2}}{q^D l^D} e^{(-Bq\sqrt{E_g}\, rl)} \left(1 - \frac{2E\varepsilon_s}{q^2 N_a l^2}\right)$ (12)



(a)

(b)

Figure 7.4 Line tunneling through the energy bands along cutline (a) AA' and (b)

Here l is length of tunneling from l_1 to l_2 for L_{t2} and l_3 to l_4 for L_{t1}, L is the length of source covered by gate which is summation of L_{t1} and L_{t2} ($L=L_{t1}+L_{t1}$) as the trench gate covers source in two dimensions both vertically and horizontally. Doping concentration is defined by N_a.

Next it is assumed that variation of l have greater impact on the exponential terms over polynomial terns and value of D is taken to be 2 (default) along with V_{onset} as a function of gate voltage V_{gs} and $V_{onset} = V_{FB} + E_g$.

Current due to line tunneling is then approximated as

$$I_l \approx WLq^{1/2}\frac{A}{B}\frac{N_a}{2\varepsilon_s}\sqrt{\frac{1}{E_G\gamma}}(V_{gs}-V_{onset})\, e^{(-BqE_g\sqrt{2\varepsilon_s}/\sqrt{q^2N_a})+(Bq\sqrt{\frac{2E_G\varepsilon_s}{qN_a}\frac{1}{\gamma}})\sqrt{V_{gs}-V_{onset}}} \tag{13}$$

where $V_{onset} = V_{FB} + \frac{E_G}{q}\left(1+2t'_{ox}\sqrt{\frac{q^2N_a}{2E_g\varepsilon_s}}\right)$ and $\gamma = 1+t'_{ox}\sqrt{\frac{q^2N_a}{2E_g\varepsilon_s}}$

The total current can be calculated as the summation of point tunneling current (12) and line tunneling current (15) at the source side of the device that is given by

$$|I| = |I_p| + |I_l| \tag{14}$$

7.6 Results and Discussions

In this section the outcome of the simulation considering classical behavior has been studied and the results in terms of transfer characteristics, band diagrams, electric field and potential along with contour diagrams are thoroughly investigated. Analytical current modelling which is performed in section IV has also been validated based on the simulation result in this section.

7.6.1 Optimum V_{DS}

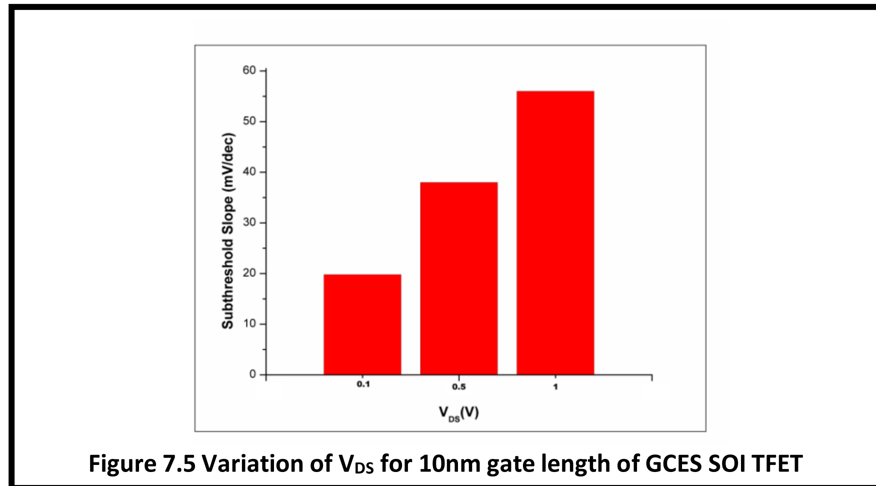


Figure 7.5 Variation of V_{DS} for 10nm gate length of GCES SOI TFET

The drain voltage of GCES SOI TFET has been varied for the gate length of 10nm. The subthreshold slopes are examined for three different V_{DS} values specifically 1V, 0.5V and 0.1V. The results found at different V_{DS} values are presented in the following figure 7.5. It is noticeable that 0.1V is optimum value for V_{DS} in this structure as it provides lowest SS.

7.6.2 Centric Source Extension

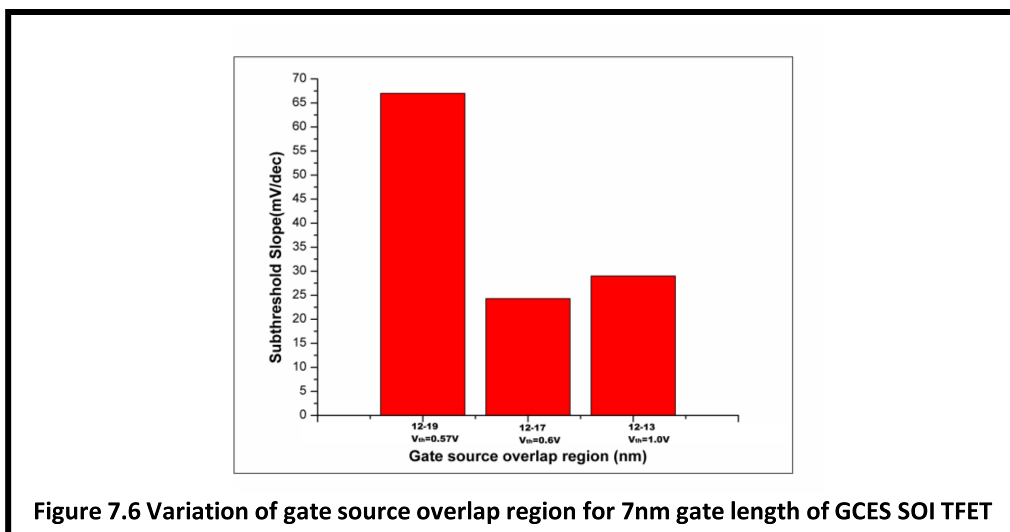


Figure 7.6 Variation of gate source overlap region for 7nm gate length of GCES SOI TFET

From the comparison explained in the figure 7.6 it is evident that center position (12-17nm) of gate length is optimum for source extension where both the threshold voltage and subthreshold slope are found to be suitable for device operation unlike for the other two cases where either the SS is high or the threshold voltage requirement is high which is not desirable. Thus, we optimize the structure by taking V_{DS} as 0.1V and optimum source extension up to center position of gate for all the gate lengths of 10nm, 7nm and 5nm respectively.

7.6.3 Position of Source and Drain Contact

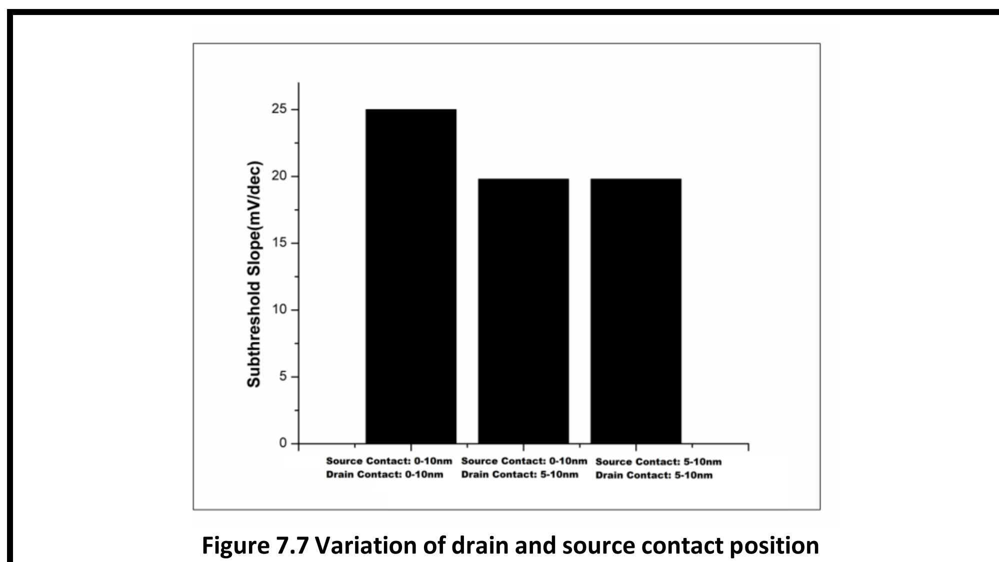


Figure 7.7 Variation of drain and source contact position

Drain and source contact positions have been varied and it is observed that specifically for drain contact position variation there is a change in subthreshold slope but the overall ON and OFF current are found to be similar whereas variation of source contact position does not create much impact on the device parameters. The variations are shown in figure 7.7.

7.6.4 Band Diagram

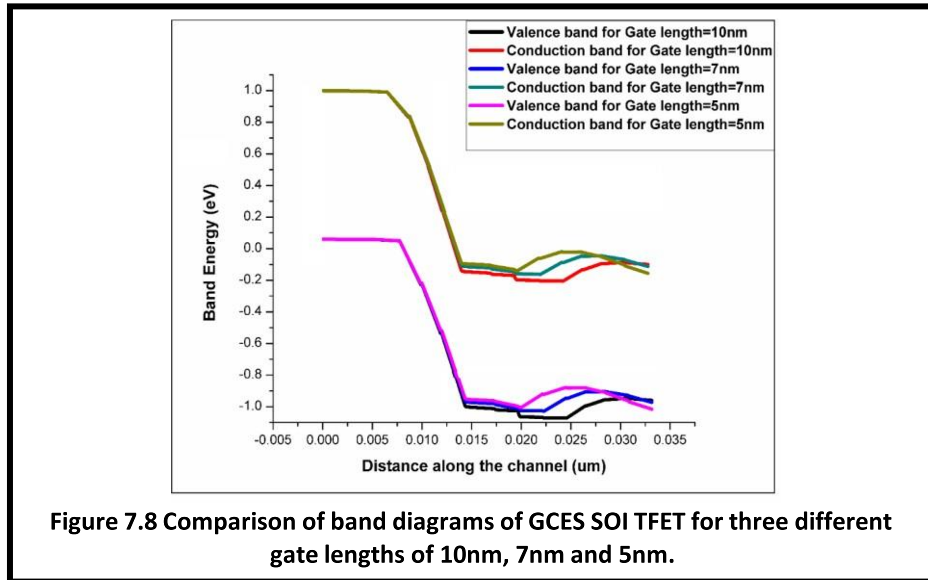


Figure 7.8 Comparison of band diagrams of GCES SOI TFET for three different gate lengths of 10nm, 7nm and 5nm.

The energy bands for each of the gate lengths are compared and it is evident from the graph figure 7.8. that for 10nm gate length, tunneling is better at the source channel interface to some extent. Simultaneously it can also be visible that in the channel-drain junction there are overshoot. This justifies that there is less probability of reverse tunnelling or ambipolar current flow in this devise structure.

7.6.5 Electric Field

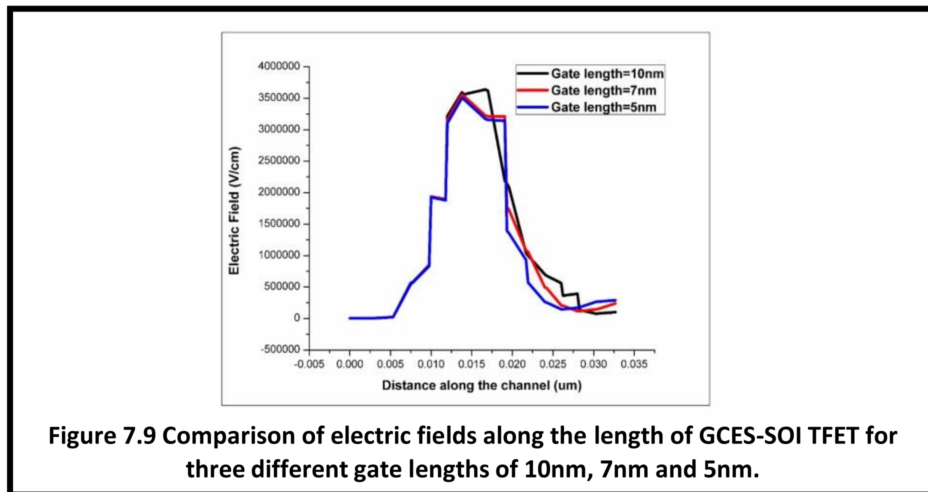


Figure 7.9 Comparison of electric fields along the length of GCES-SOI TFET for three different gate lengths of 10nm, 7nm and 5nm.

It is evident from the figure 7.9 that the electric field for 10nm gate length is slightly higher then 7nm and 5nm gate length in the source-channel junction. In the drain channel junction it is visible the for 10 nm gate length there is a small inclination in electric field compare to the 7nm and 5nm gate length, which is also reverse to a conventional TFET. This justifies the three is very less probability of reverse tunnelling in this structure.

7.6.6 Surface Potential

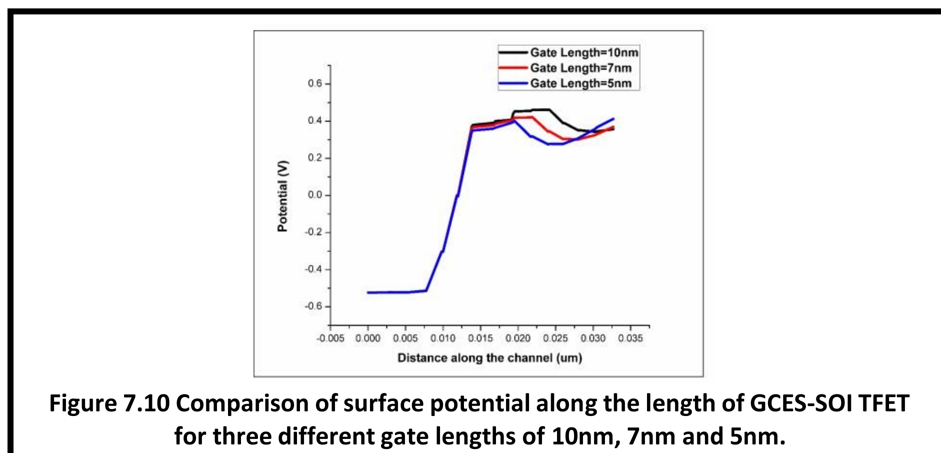


Figure 7.10 Comparison of surface potential along the length of GCES-SOI TFET for three different gate lengths of 10nm, 7nm and 5nm.

In figure 7.10 the three graphs depict almost similar results. In all three cases, potential of the proposed structure without considering quantum confinement has a larger value of surface potential than the quantum effects.

7.6.7 Transfer Characteristics

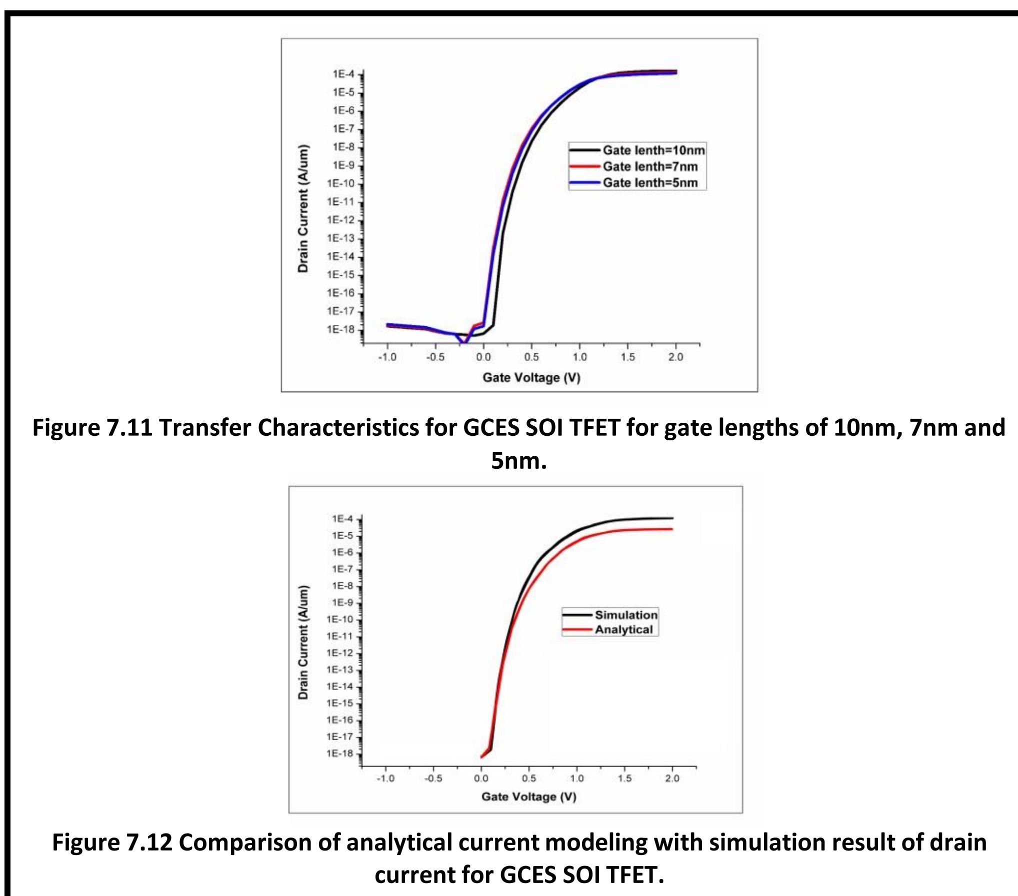


Figure 7.11 Transfer Characteristics for GCES SOI TFET for gate lengths of 10nm, 7nm and 5nm.

Figure 7.12 Comparison of analytical current modeling with simulation result of drain current for GCES SOI TFET.

It is evident from the figure 7.11 that the curves differ from each other due to variation of subthreshold slope (SS) while the ON and OFF currents remain the same. Form figure 7.11 is

can be seen that of 10nm gate length higher than other two gate length . The comparison of current characteristics derived from analytical current modeling and simulation considering 10nm gate length dimension has been illustrated in figure 7.12. It is prominent from the figure that the current graphs of analytical model and simulation are analogous and hence the analytical current model has been validated.

7.7 Quantum Confinement

In this section quantum confinement due to low dimensional device structure has been considered and outcomes of the same have been comparatively studied with results of classical behaviour.

7.7.1 Transfer Characteristics

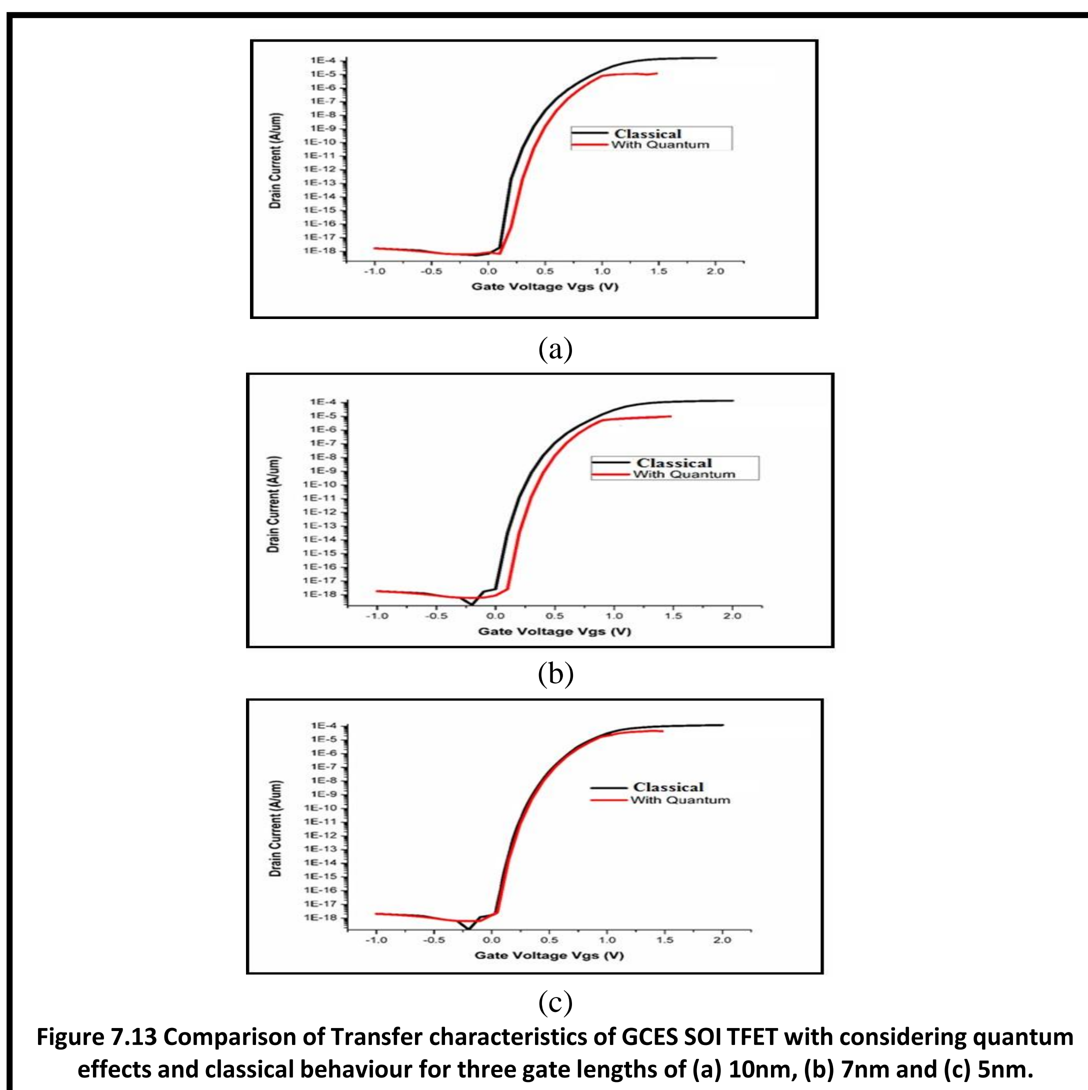


Figure 7.13 Comparison of Transfer characteristics of GCES SOI TFET with considering quantum effects and classical behaviour for three gate lengths of (a) 10nm, (b) 7nm and (c) 5nm.

It is evident from the figure 7.13 that for three different gate lengths the ON current is higher (10^{-4} A/um) for classical approach that for quantum approach. The reason behind lower ON current for quantum confined results is the discretization of the energy bands at the source

channel interface and thus the electrons can only tunnel through the first available empty energy state between the interfaces. There is no ambipolar conduction in all the cases taken into account and thus the device has the capability for low power applications. All the curves indicate the comparative performance between classical and quantum models.

7.7.2 Electron Concentration

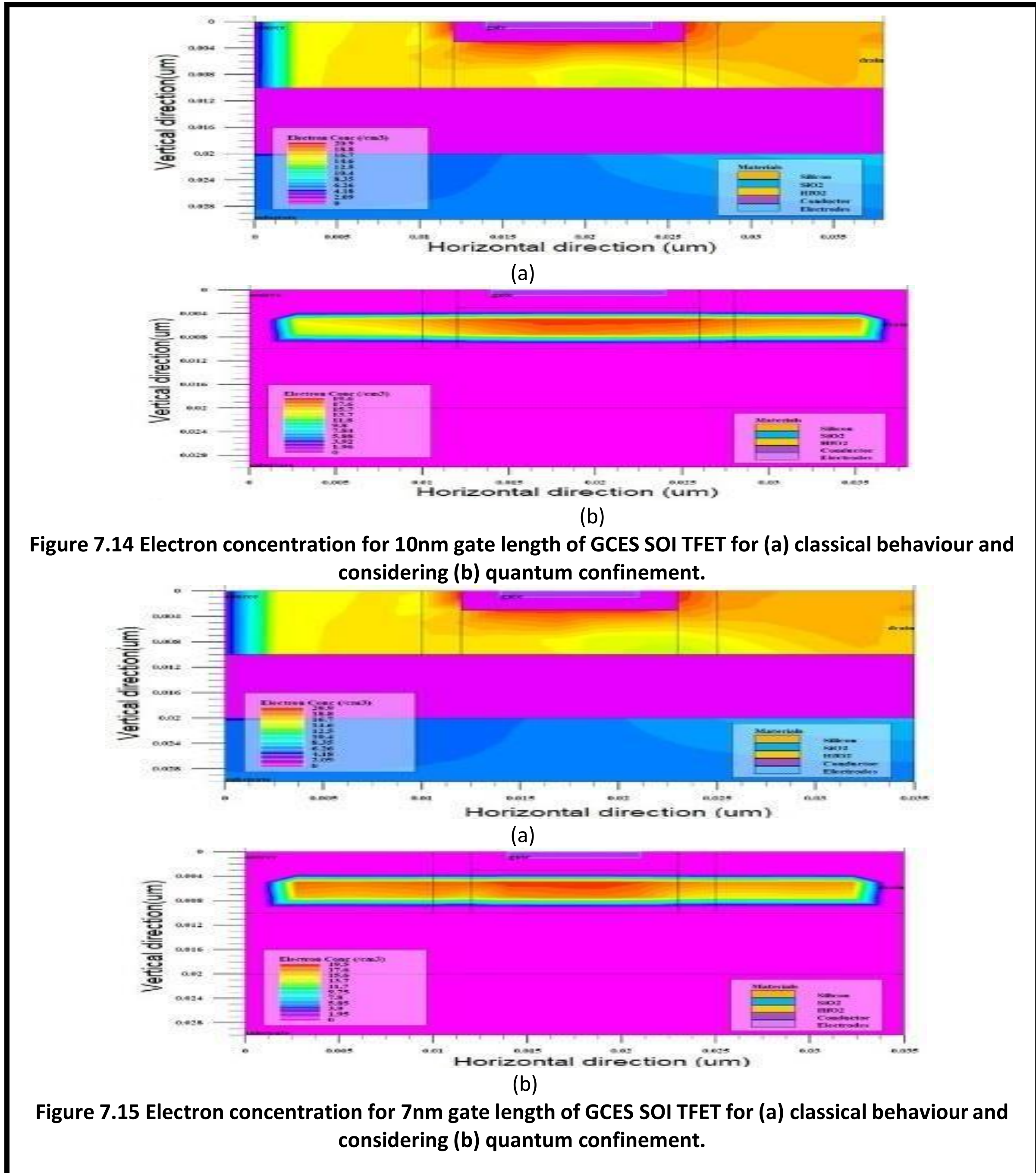
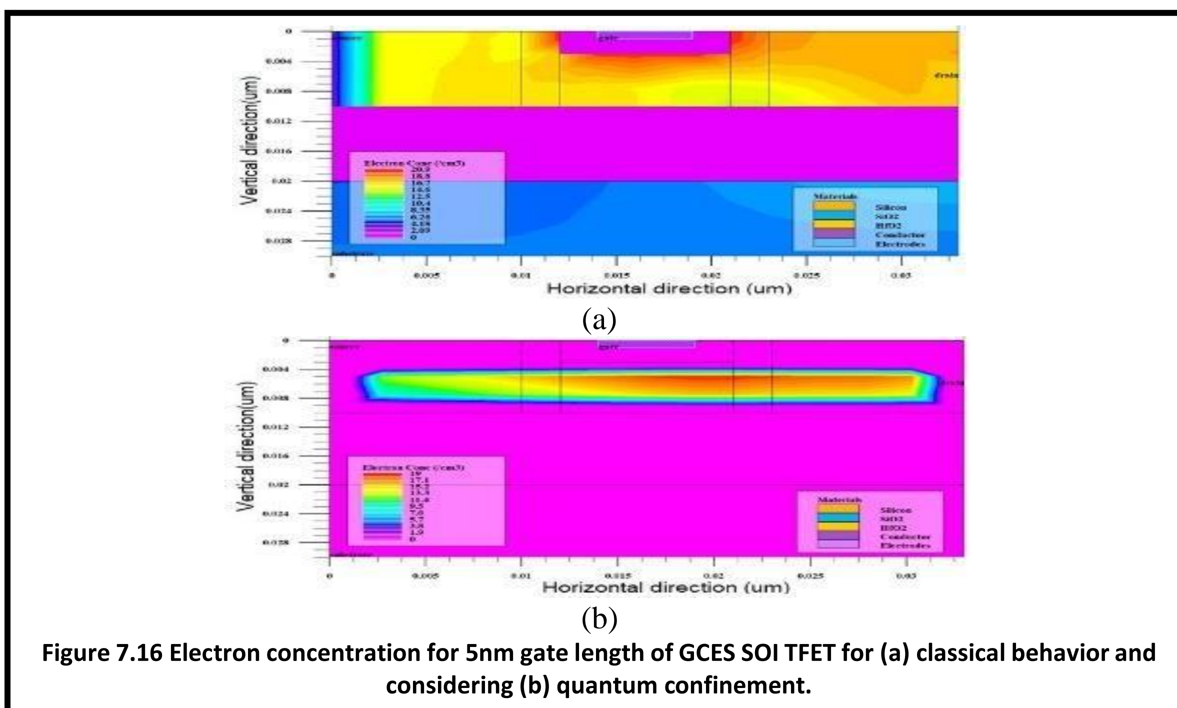


Figure 7.14 Electron concentration for 10nm gate length of GCES SOI TFET for (a) classical behaviour and considering (b) quantum confinement.

Figure 7.15 Electron concentration for 7nm gate length of GCES SOI TFET for (a) classical behaviour and considering (b) quantum confinement.



(a)

(b)

Figure 7.16 Electron concentration for 5nm gate length of GCES SOI TFET for (a) classical behavior and considering (b) quantum confinement.

Electron concentration area within the device for quantum and without quantum are different. It is illustrated and clearly visible from the contour diagrams that for all the three gate lengths of 10nm, 7nm and 5nm, electrons are confined within a particular area when quantum confinement has been considered whereas this confinement of electrons are absent in case of the same structures without quantum effects. The contour diagrams for the same are presented below in figure 7.14, 7.15 and 7.16.

7.7.3Comparison of Subthreshold Slope

The SS for three different gate lengths such as 10 nm, 7 nm and 5 nm have been compared and illustrated in the following figure 7.17 where it is prominent that SS with considering quantum confinement is less on than that of classical behaviour.

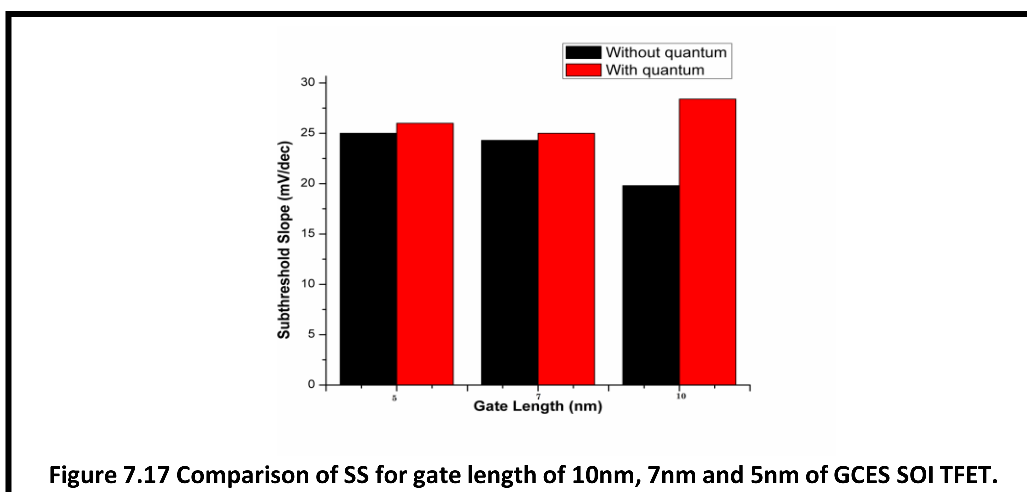


Figure 7.17 Comparison of SS for gate length of 10nm, 7nm and 5nm of GCES SOI TFET.

7.8 GCES SOI TFET Inverter

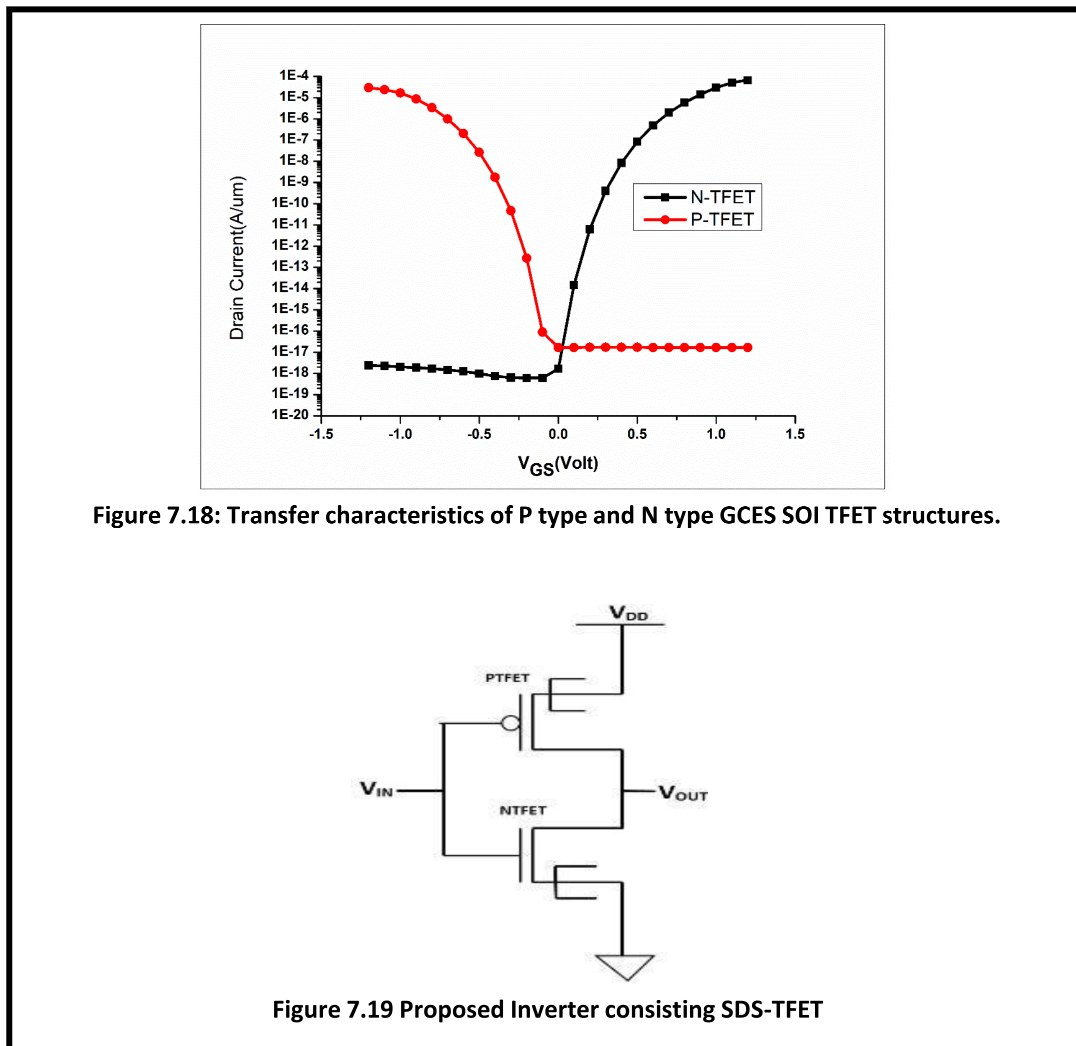
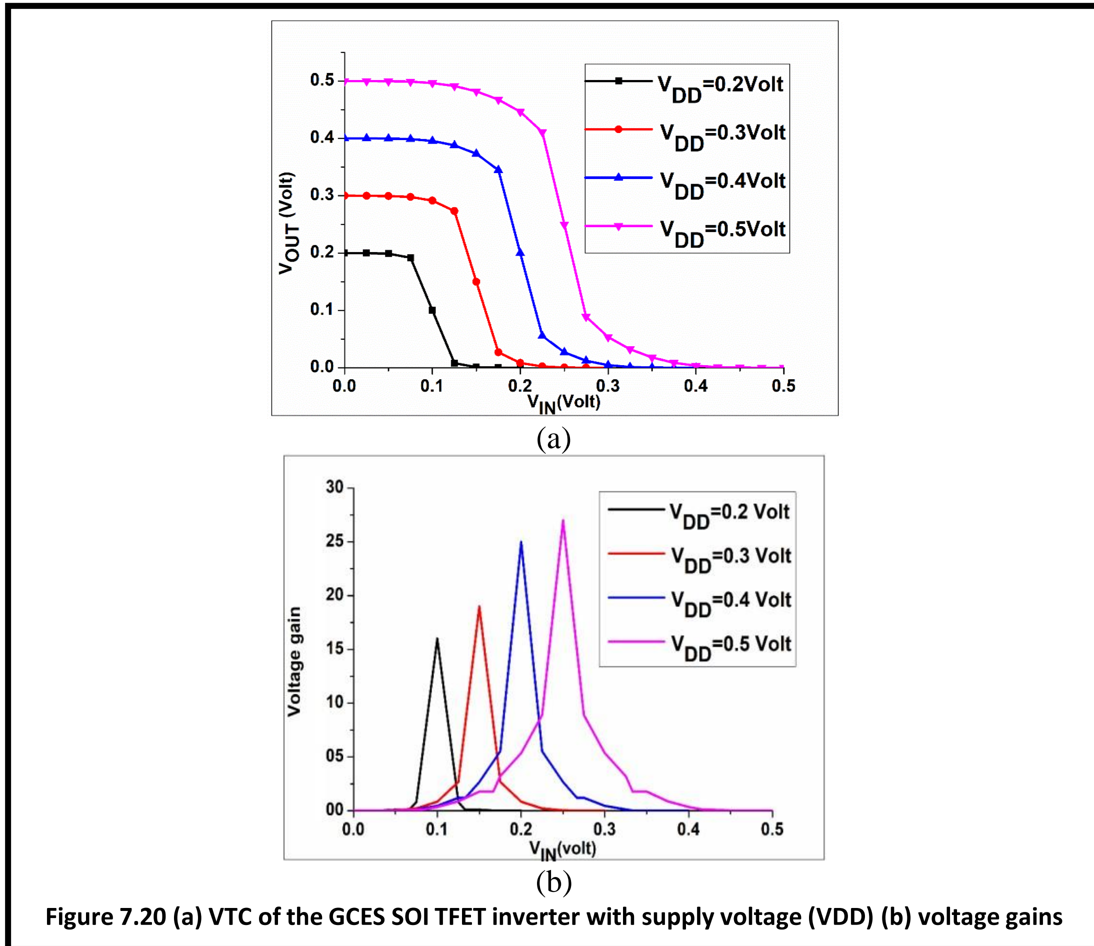


Figure 7.18: Transfer characteristics of P type and N type GCES SOI TFET structures.

Figure 7.19 Proposed Inverter consisting SDS-TFET

The n-type and the p-type GCES SOI TFET transfer characteristics are presented for same V_{DS}=0.1V and it is evident from the figure 7.18 that the currents almost mirror each other for both the types and hence is suitable for inverter circuit simulation.

Figure 7.19 shows the sematic design Proposed Inverter consisting SDS-TFEt. Figure 7.20 shows the proposed inverter has better gain at V_{DD} = 0.2 V [7.23][7.24] because of larger I_{ON} and suppressed ambipolarity. The simulated VTC shows that the transition voltage of the inverter is located around V_{DD}/2 and a clearly separation between the high and the low levels, indicating both devices are working properly. High voltage gains (V_{OUT}/V_{IN}) is also achieved as shown in figure 7.20(b) at lower V_{DD} = 0.2V. A voltage gain as high as 16 is obtained at lower V_{DD} = 0.2V, demonstrating high potential for future low power applications. from 0.2 V to 0.5 V. (b) voltage gain of the GCES SOI TFET inverter under various V_{DD}, showing high gain even at V_{DD} = 0.2 V.



(a)

(b)

Figure 7.20 (a) VTC of the GCES SOI TFET inverter with supply voltage (VDD) (b) voltage gains

Further proceeding with lower V_{DD}=0.2V, figure 7.21 shows the transient behavior of GCES SOI TFET inverters simulated for a peak-to-peak voltage of 0.2V for 40 ns without considering any load capacitance [7.26]. It shows that overshoot related to an enhanced Miller capacitance. This transient behaviour of the proposed GCES SOI TFET inverter is promising for future low power digital applications.

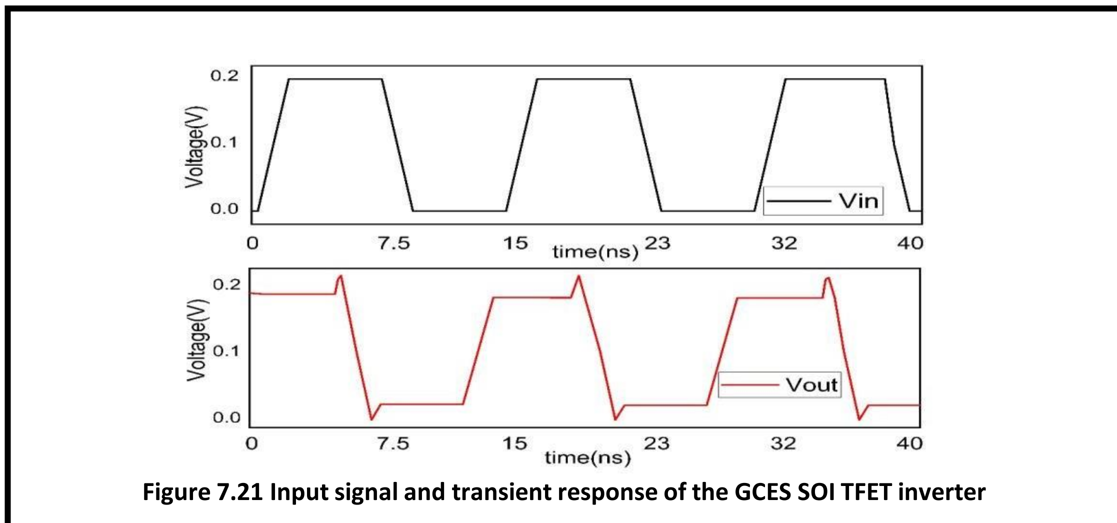


Figure 7.21 Input signal and transient response of the GCES SOI TFET inverter

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Chapter-8: Concluding Remarks and Future Scope

8.1 Concluding Remarks.. 219
8.2 Future scope... 222

8.1. Concluding Remarks:

This chapter summarizes the main contributions of the present dissertation and outlines the scopes of its future extension at the end.

A well-defined introduction of the thesis work is presented Chapter-1, followed by the requirement for low-power devices. The motivation for the current work stems from the shortcomings of the MOSFET, especially when subjected to aggressive scaling. TFETs having sharper ION-IOFF characteristics than the MOSFETs; hence they are a viable replacement for CMOS-based circuits in near future.

Chapter-2, An exhaustive outline of the basics of semiconductor devices right from the conventional MOSFETs to current shortcomings associated with the realization of ultra-low dimensional devices and the need of investigating resurrected FET models to ameliorate the flaw of short channel devices. Begins with the comparison between the basic structures of TFET and MOSFET, followed by a brief discussion on the working principle of TFET. Finally, go through a brief qualitative discussion on various TFET designs. We can broadly classify the vast range of TFET designs for our ease in considering the structural modifications as per requirement. The TFET designs are strongly motivated by two main short-comings of TFET: i. the ambipolar conduction and ii. low ON current. For the reduction of ambipolar conduction multiple dielectrics or using multiple gate metals techniques can be applied. Depending on the ease of fabrication, one can prefer one over other. Although finding a compatible metal with required work-function might be somewhat limiting. Both of these techniques require modification in fabrication process, hence their fabrication might not be cost or time effective. The easier method is to use lightly doped drain method, which is much less complicated. The drawback of lightly doped drain is the increased contact resistance, which might or might not be problem depending upon the application.

In chapter-3 Drain Doping Engineered Splitted Drain tunneling field-effect transistor (TFET) structured is demonstrated which exhibits a major reduction in ambipolar conduction due to an increase in the effective channel length. Four different Drain Doping Engineered split drain structures is executed here and they are named according to the relative position of the drain: Splitted-Drain Single-Gate TFET (SD-SG TFET: total drain is splitted), Top-Splitted-Drain Single-Gate TFET (TSD-SG TFET: splitted-drain in upper location), Mesial-Splitted-Drain Single-Gate TFET (MSD-SG TFET: splitted-drain in middle location), Basal-Splitted-Drain Single-Gate TFET (BSD-SG TFET: splitted-drain in bottom location). All the fundamental device characteristics and parameters are analyzed for all four structures and their merits and drawback are recorded for optimal valuation and detection of better structure(vide Figure 3.1.). An 2D-analytical model is derived and it has been validated with the simulated result. Out of all the four structures, the BSD-SG TFET has highest ON current starting around in the range of 1×10-3 A (vide Figure 3.11) and OFF current starting around in between 1×10-17A (vide Figure 3.11). BSD-SG TFET improved performance with suppressed gate leakage and ambipolarity followed by MSD-SG TFET, TSD-SG TFET then SD-SG TFET, all structures indicate better characterization than conventional TFETs (vide Figure 3.11). Also, the ambipolar conduction is reduced due to the proposed parted drain structure which can be observed from the density of states switch band diagram and electric field of the proposed structures ((vide Figure 3.8 and Figure 3.9).

In chapter 4: A Double Trench Gate Covered Source-Channel TFET (DTG-CSC-TFET) has been simulated and analytically modelled. The configuration of the double trench gate along with the covered source-channel ensures very large tunneling area. Both line tunneling and point tunneling mechanisms contribute to the ON-current. The device parameters such as energy band diagram, electric field, potential profile as well as the transfer characteristics were compared for different values of the extended source length L_S (10nm, 15nm, 20nm). The voltage was optimized at V_{DS}=0.1V (vide Figure 4.7). It was observed that the structural variation with L_S=20nm exhibited highest degree of tunneling and superior subthreshold swing. It is hence, the most optimized structure (vide Figure 4.8). This is expected, as increasing L_S increases the tunneling area. The BTBT is observed to be lowest along cutline 2. The SS obtained for the optimized structure is 23mV/decade and the I_{ON}/I_{OFF} ratio is 10^{12}(vide Figure 4.8). The structure exhibits excellent SS, high I_{ON}/I_{OFF}, high ON-current of about 10^5A/μm, whilst operating at a very low drain bias of 0.1V(vide Figure 4.13). The device can be adopted for both n-type and p-type devices for the inverter implementation. The inverter has a higher

voltage gain of 24 at lower V_{DD}=0.2V, and has a power dissipation of 69.7 nW (vide Figure 4.18). Hence proposed structure is a promising candidate for the next generation low power applications

Chapter 5: Incorporation of CA-PNPN-DG TFET and TB-PNPN-DG TFET structures are executed analytically and the analytical result is compared with the SILVACO ATLAS simulated result. The two structure shows improvement then to a conventional TFET. But the CA-PNPN-DG TFET shows lesser SS and lower V_{th} (vide Figure 5.16). Furthermore, the frequency analysis is performed to find out the transconductance generation factor .and the transconductance frequency product. An inverter is implemented using this device here which shows lesser power dissipation of 47.3nw and delay of 56.28ps (vide Table 5.1).

Chapter 6: A 2D TFET with centrally aligned source pocket doping has been executed which can be used as a low-power VLSI design alternative to today's CMOS technology. At a lower V_{DS}=0.1volt, both n-type and p-type DSS-TFETs generate greater I_{ON}/I_{OFF} ratios of 10^{13} for n-type and 10^{12} for p-type respectively, with the minimal ambipolar current (vide Figure 6.4). Because the difference in SS is almost negligible for different channel lengths, both TFETs are extremely scalable. As a result of, the 13nm n-type and 5nm p-type DSSTFETs may be incorporated during circuit design, resulting in a decrease in chip area. This is the primary benefit of the proposed device. From the VTC curve of the proposed inverter, it is evident that the high to low noise margin is of 97% which justifies the proposed inverter is almost identical to a CMOS inverter and a having a higher voltage gain of 16 at a supply voltage of 0.2V (vide Figure 6.12). Also, from the power consumption, delay and PDP point of view, the proposed logic gates are superior than the compared TFET-based logic gates.

Chapter 7: A GCES-SOI TFET with three different gate lengths is compared considering quantum confinements that of neglecting quantum effects. The device is optimized with an extended source part aligned with the center position of the gate, and drain contact position at the lower part of the vertical dimension to the right side with an optimized V_{DS} value of 0.1V. The device transfer characteristics, electric field, potential distributions, and band diagrams are extensively investigated and compared for different gate lengths. The comparative outcomes conclude that the 10nm gate length structure is optimum for improved device performance in terms of parameters like SS, Vth, and I_{ON}/I_{OFF} ratio (vide Figure 7.11). Considering quantum confinement it was evident that the device ON current decreases along

with an increase in SS due to discretization of the energy bands (vide Figure 7.13 and Figure 7.17). The device can be adopted for both n-type and p-type devices for an inverter implementation. The inverter has a higher voltage gain of 16 at V_{DD}=0.2V (vide Figure 7.20) and has a high potential for future low-power applications.

8.2 Future scope

The analytical results manifested in this thesis, based on TFET employing concepts of drain engineering, dielectric engineering, channel engineering, and metal work function engineering, source engineering will have a considerable impact on future ultra-low dimensional device research. Such study may open up numerous new areas of nanoelectronics device applications, e.g., sensors, oscillators, etc. At the same time, there is enough room for further research direction to enhance the accuracy of the presented results.

With continuous downscaling of device dimensions for achieving an enhanced speed of operation and reduction of circuit power consumption, there is a need and scope to incorporate quantum confinement effects in such highly miniaturized devices (sub-20 nm node) to optimize the proposed TFET configurations for suitable circuit applications.

It has become a never-ending process proposing renovative and innovative FET models fitting in the current scenario to battle with SCEs methodically ensuring upgraded performance since we are not completely out of short channel issues. Thus, there is still the galore purview of delve for modeling further composite hybrid structures with aid of new geometry to solve low ON current and lessen ambipolar current without degrading the device performance toward a possible search of green nanotechnology.

Bijoy Goswami
16/08/2022