Abstract

In the last decade, there has been a gradual reduction in the dimension of the devices, and the reduction of dimension leads to the short channel effect in MOSFET. Researchers tried to overcome those short channel effects by incorporating geometrical modification of device structures including Silicon On Insulator (SOI) and Silicon On Nothing (SON) MOSFET which focused significant research limelight. Owing to the superior scalability and much reduced parasitic capacitive effects, they emerge as improved structures over traditional MOSFETs which exhibit higher circuit speed, better subthreshold behaviors, and subdued SCEs. However, in spite of all these benefits, SOI/SON technology faces two crucial challenges to further scaling. Firstly, the downscaling of the channel length causes the gate to lose its electrostatic control over the channel potential thus degrading the device electrostatics significantly. The second one being the most critical is the scaling constraint of supply voltage owing to the thermionic limitation of the steepness of sub-threshold swing which leads to increased power consumption.

That has created a path for a new type of device structure an innovative structure called TFET (Tunnelling Field–Effect Transistors) where we can overcome the short channel effect and we can reduce the power dissipation. The predominant benefit of TFETs is current conduction through modulation of quantum mechanical Band-to-Band Tunnelling (BTBT), which is a result of finite but non-zero probability of tunneling through a potential barrier, a process in which electrons tunnel from the valence band through the semiconductor bandgap to the conduction band or vice versa without any trap assistance. This attribute carries forward the advantages over the thermionic injection across an energy barrier for carrier transport in MOSFET. Thus, due to its built-in tunnel barrier, where the channel current in TFET is

controlled by the tunneling mechanism from the source, the TFET device is resistant to the short channel effect and allows TFETs to have SS as low as 25 mv/decade, which is a root cause of designing of low power devices. Again, it may be pointed out that TFETs differ from the MOSFET only in the type of source doping, so f the TFET fabrication process is not much different from the MOSFET fabrication process.

The primary constraints concerning TFET devices are ambipolar conduction which originates from the BTBT at the drain–channel junction and the other is low I_{ON}, which is considerably poorer than MOSFETs. Hence there is a need for a structural modification methodology that reduces the ambipolarity of TFETs without compromising the I_{ON} as well as improving SS has been to be introduced and examined by researchers. Various modifications such as the multi-gate device geometry e.g., double gate (DG), tri-gate (TG), quadruple gate (QG), gate all around (GAA) TFET have been to mitigate these limitations faced by the conventional TFET.

The aim of the work herein presented in this thesis is to explore the physical phenomena and mechanisms to be studied for a precise understanding and description of the different innovative TFET device structures. Identification of the existing limitations, incompatibilities, and problems that arise during simulation processes, using the SILVACO ATLAS. Use of a high-*k* gate dielectric or a low-*k* spacer to reduce the barrier at the source-channel interface boosting the tunneling current and keeping the bandgap in other regions large to subdue the ambipolar behaviour and elevate the I_{ON} of the conventional TFET. Development of analytical modeling to pursue a better comprehensive study of device physics for its further improvement. The analytical results obtained are further validated with relevant simulated data for substantiating the accuracy of the resultant model and facilitating implementation in low-power circuit-level analysis.