

**Jadavpur University**  
**Master of Power Engg. 1<sup>st</sup> Semester 2017**  
**Digital Systems**

Time: 3hrs  
 Full Marks: 100

**Answer any Five**

1. Using FSM concepts, design a 4 bit synchronous down counter. 15  
 Assuming a propagation delay of 40ns per F/F calculate the maximum clock frequency at which you can operate a 4-bit ripple counter. 5
2. With a suitable circuit deduce an expression for duty cycle and time period of a 555 timer connected to external resistances  $R_a, R_b$  and a capacitance  $C$  in an astable multi-vibrator mode. Is it possible to set the duty cycle to any value in this mode? Substantiate your answer. 15+5
3. For a TTL gate, with suitable representative values of  $I_{IH}, I_{IL}, I_{OH}, I_{OL}$  and  $V_{IH}, V_{IL}, V_{OH}, V_{OL}$  calculate the (i) Fan out and (ii) noise margin. 10  
 Assuming these values design a pull up resistor for a TTL gate 10
4. Obtain the Z transform for  $f(t) = e^{-at}$  sampled at an interval  $T$  and hence deduce the ROC. 5  
 If  $F(z)$  represents the Z transform for a discrete function  $f(kT)$  deduce the Z-transform for the time-shifted function  $f(k-N)T$ . 5  
 State and prove the final value theorem in discrete domain. 10
5. Deduce a mapping from s plane to z-plane using bilinear transformation (derive the transformation) 10  
 Using this transformation can you deduce how does a point  $z = 1.2$  map into the s plane? 10
6. Deduce the Fourier Transform of a time-shifted rectangular pulse of height  $H$  and width  $T$  10  
 If  $F(\omega)$  be the Fourier Transform of  $f(t)$  prove that  $f(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(\omega) e^{i\omega t} d\omega$  10
7. State and prove sampling theorem. 15  
 Consider a signal  $x(t) = 3\cos 200\pi t$   
 a. Determine the minimum sampling rate required to avoid aliasing. 1+4  
 b. Suppose that the signal is sampled at the rate of  $F_s = 200$  Hz, what is the discrete-time signal obtained after sampling?
8. Sketch the Manchester Coded signal for the bit sequence 11001010 5  
 If bit stuffing is used for the bit sequence of 64 consecutive logical 1s, how will the bitwise efficiency change. 5  
 Is it possible implement ring topology over a star connectivity of computer nodes? Explain 5  
 A serial communication uses 8 bit data with no parity and 1 stop bit and has a speed of 4800 bps. How much time will this link take to transmit 1 MB? 5