MASTER OF ELECTRONICS & TELE-COMMUNICATION ENGINEERING

EXAMINATION, 2017

(1st Year, 2nd Semester)

VLSI DESIGN

Time : Three hours   Full Marks : 100

Answer *any five* questions

1.(a) We want to design a little game with an seven segment display(SSD). The system should contain two inputs (clock and stop) and one output. Assume that clock frequency is 1KHz. The circuit should cause a continuous anticlockwise movement of the SSD segments. The sequence should be [a →fa→ef→e →de →d →cd →c →bc →b →ab →a]. If stop is asserted, the circuit should return to state 'a' and remain so until stop is turned low again. Design the system.   12

Q1b) Design an asynchronous sequential logic circuits and Explain fundamental mode & pulse mode operation with examples.   08

2a) Design a sequential logic circuit that controls and maneuvers a mobile toy car lawn mower. It is equipped with a light sensor and an obstacle sensor. The light sensor detects the ambient light intensity. The other sensor detects obstacles in its path.

Write the algorithms and explain the steps. Draw with proper explanation for i) Sensor signals, ii) relation between control signals and toy car movement, iii) mealy machine steps designer with proper explanations, iv) states of the toy car controller, v) state table for toy car controller.

Write the final expressions for the toy car movement. Report the same using a more machine technique. Determine the maximum clock frequency of which your design operates correctly. Provide a reset function. 12

Q2b) Design the control circuit for a bank locker opener. A signal push button controls the opening and closing of the locker. Pressing the push button opens a closed locker or closes an opened locker. In order to provide safety, the direction of the moving part of the locks door showed be reversed immediately if the button is pressed. 08
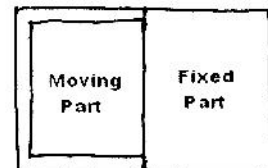
Q3a)   Using twos complement arithmetic, a number 'A' is stored in a 5-bit register. The number is scaled to replace the registar of A by B, where B=A/4. The error caused discarding the two least significant bits may be larger than the one-half the numerical significance of the least significant remaining bit. For example , if A=01111=15,then B=00011=3, while the correct result is 15/4=3.75. Rounding off the correct answer should yield 4=00100. Design a logic system which rounds off B to the nearest integer.   Draw the circuit diagram   10

Q3b). Design a combinational circuit based digital bank locker opener with three buttons,1,2 and R. In order to enter a code, the numerical buttons are to be pressed and the push button 'R' is used for reset purpose. For opening the locks a user should first push the reset button 'R' and then enter a code of three digits. R button is to be used to start over again in case of any mistake in entering the code. To

[Turn over

open the locker your circuit should produce an output of 'O' after the correct code has been entered and draw the schematic circuit diagram of the locker for the code 1-2-1.   10

Q4. (a)Design a maximal length sequence generator having a sequence length s=31.   08

(b)Show that the correlation function of any flip-flop output, say $Q_1(K)$, is

$$R_{Q1(i)} = \sum_{K=1}^{31} Q1(K)Q1(K+1) = \begin{cases} 31 & i = 0 \\ -1 & i \neq 0 \end{cases}$$

To obtain this result let 1v represent logic 1 and -1 represent logic '0'.   12

Q5 Design a circuit that takes a serial stream of ASCII characters as input and outputs a '1' whenever the sequence "ap5"occurs.   20
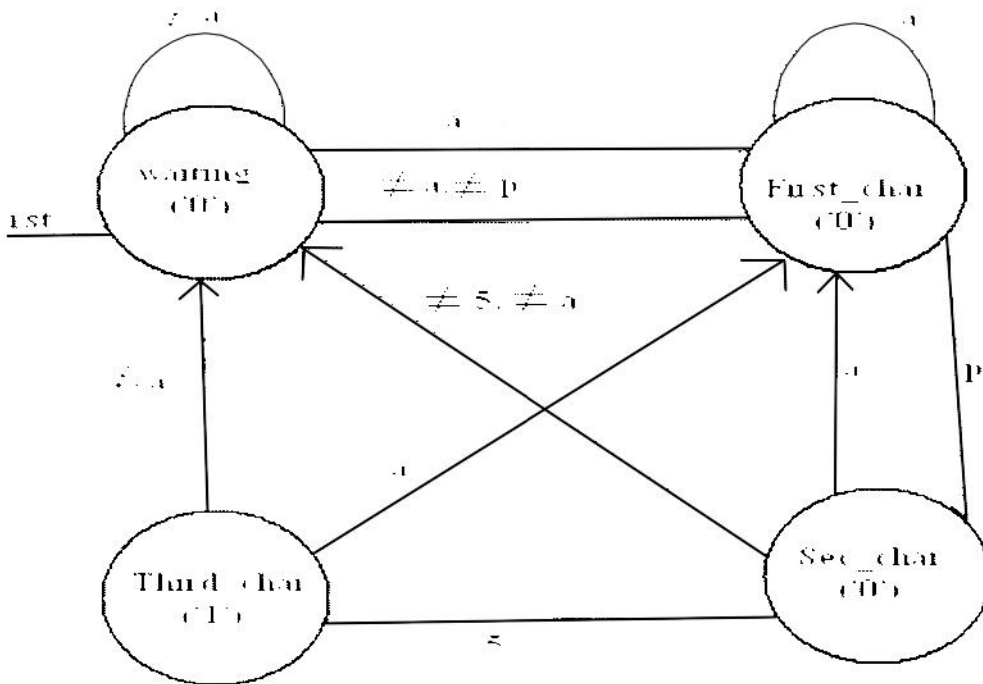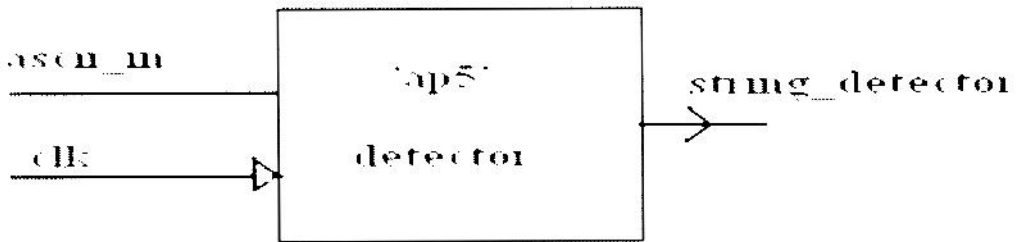
Q6. Design a controller for an electronic metro door which should have, besides clock and reset, four other inputs; remote (= '1', when the remote control is activated), open (= '1', when the door is completely open, provided by a sensor), closed(= '1', when the door is completely closed, also provided by a sensor), and timer (= '1', 30s after open= '1' occurs). At the output, the following signals must be produced: power (when '1' turns the electric motor on) and direction (when '0' the motor rotates in the direction to open the door, when 1 in the direction to close it). The controller shows the following features:

(a)   If remote is pressed while the door is closed, immediately turn the motor on to open it

(b)   **If remote is pressed while the door is open, immediately turn the motor on to close it**

(c)   If remote is pressed while the door is opening or closing, immediately stop it. If pressed again, the remote should cause the door to go in the opposite direction

(d)   The door should not remain open for more than a certain amount of time(for example 30s)this information is provided by an external timer. Design this system using the formal FSM design technique. Indicate, would any glitches be a problem for this system. Also estimate the no. of F/F necessary to implement this circuit. Does the clock frequency affect this number? Why?   20

Q7 a) The error obtained due to scaling can be reduced by using saturation logic. Let B=4A, where A and B are each expressed using 4 information bits and a sign bit. A and B may be positive or negative and are expressed usuing twos complement arithmetic. Design a system and an input A and output B which satisfies the equation :

$$B=\begin{cases} 15 \ for \ A \geq 4 \\ 4A \ for \ |A| \leq 3 \\ -15 \ for \ A \leq -4 \end{cases}$$

As A varies from -15 to +15.

13

Q7 b) E1 buses leave the 8B bus terminal every hour unless there are fewer than 20 passengers or if the driver/conductor is late. If there are fewer than 20 passengers, the bus will wait 10 min or until the number of passengers increase to 20. If the bus leaves on time ,it can travel at 60 Km/hr. If the bus leaves late, or if it rains, it can travel only at 30 Km/hr.

        Under what conditions will the bus travel at 60 Km/hr?
Construct a special purpose computer using AND, OR, and NOT gates, switches, battery, and a light bulb. The bulb should glow if the bus can travel at 60 Km/hr.   07
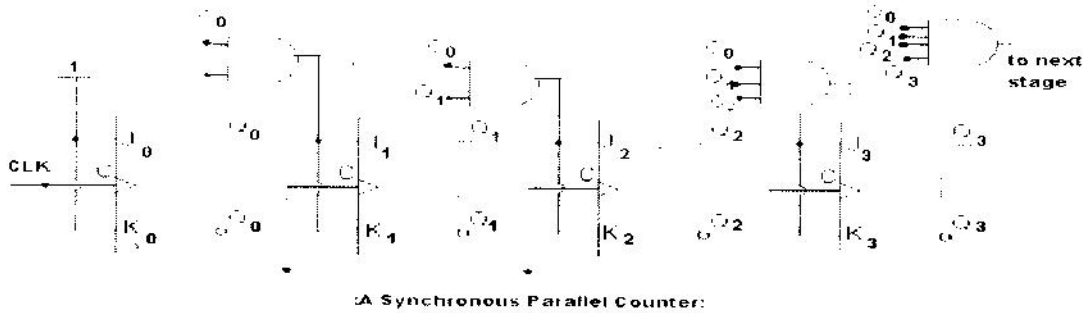
8.a)Consider the synchronous parallel counter as shown in the Fig. below. Assume that the relationship between the propagation delay time and the fan out of any of the flip-flops used is

$$t_d = t_{d0} + \lambda F_0$$

:A Synchronous Parallel Counter:

where λ is a constant of proportionality and F_0 is the required fan out. If an N stage counter is to be designed with a strobing time Γ_s, show that the maximum clock frequency is

$$f_{max} = \frac{1}{td0 + \lambda(N-1) + \Gamma's}$$

10

Q8b) Design a control unit for a simple coin-operated cold drink vending machine. The drink costs Rs. 15, and the machine accepts currency of Rs 5 and Rs 10. Change should be returned if more than Rs 15 is deposited. No more than Rs 20 can be deposited on a single purchase.

Give all steps including state diagram

10