Ref No . **EX/PG/ETCE/T/129F/2017**

MASTER OF ENGINEERING IN
ELECTRONICS & TELE-COMMUNICATION ENGINEERING EXAM -2017

(First Year, 2nd Semester)

ELECTRONIC DESIGN AUTOMATION (ED)

Time : Three Hours **Full Marks : 100**

Answer any four questions.

1.

a. What is test bench? Write test bench program to verify XOR gate . **2+10=12**

b. What is user defined package. Explain it using small code. **6**

c. Explain with example about multiple processes? **7**

2.

a. What is delta delay in VHDL? How Transport and inertial delays are described? **4+6= 10**

b. Explain the effect of inertial delay in signal driver allocation for behavioral model **7**

c. Write a program of 3 bit ripple counter by using structural model. **8**

3.

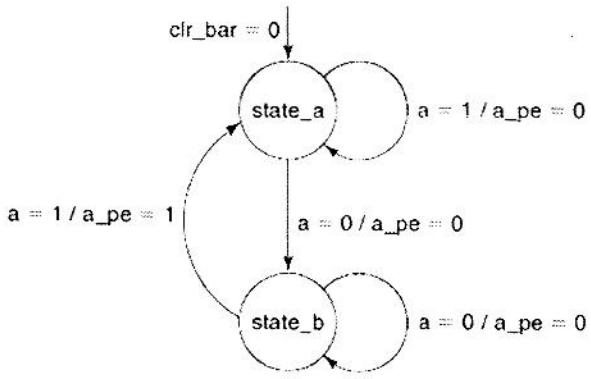
a. What is resolved signal? Write a short code to describe the resolution function **2+8=10**

b. Write a program of D flip flop using behavioral model. **7**

c. Write a program of n input OR gate. **8**

4.

a. Write the VHDL code of Mealy FSM state diagram for a positive edge detector. **12**



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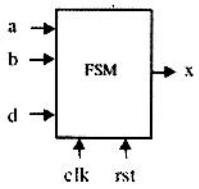
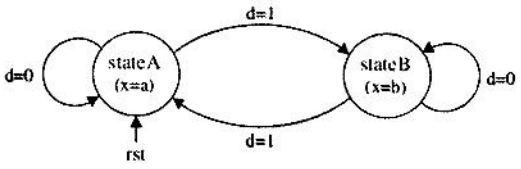
b. Write the VHDL code for the following state machine. **13**





5.

a. Explain the MOS small signal model and describe each terms. **10**

b. What is SPICE Level -1 what are the primary net-list parameters? **7**

c. Describe the operation of MOS capacitor and their behavior in different operational zone **8**

6.

a. What is the requirement of scaling? What is constant field scaling and constant voltage scaling? **3+4=7**

b. Describe the condition of Cox, Id(linear), Id(Sat) , power dissipation, power density, gate delay for both constant field and constant voltage scaling **12**

c. Find the drain current and transconductance for an NMOS transistor operating with $V_{GS} = 2.5$ V, $V_T = 1$ V, and $K' = 1$ mA/V^2. **6**