M. E. (ELECTRICAL) EXAMINATION, 2017
(2nd Semester)

SUBJECT: - DESIGN AND APPLICATION OF EMBEDDED SYSTEMS

Full Marks 100

Time: **Three hours**

No. of Questions		Marks
	*Answer **any five***	
1.	a) Describe briefly the fabrication steps for MOS transistor in VLSI technology.	5
	b) What are the different types of model for calculation of gate delay of CMOS logic gates using parameters as (W/L) ratio, V_{DD}, V_{SS}, channel resistance (Rn or Rp), load capacitance (C_L)?	6
	c) Explain the advantages of MTCMOS logic gate. How can they be operated?	5
	d) Explain how DCSL gate consumes very low power in operation.	4
2.	a) Explain the terms such as i) Event driven simulation, ii) Compiled simulation, iii) Simulation time wheel.	6
	b) Distinguish between Mealy and Moore type Finite State machines.	4
	c) What is the basic purpose of State Machine model for describing behaviour of a system? Why hierarchy and concurrency are incorporated in State Machine model. Give example.	6
	d) Describe the Program-Stat Machine Model for an Elevator control process.	4
3.	a) Explain how the performance of sequential logic circuits can be analyzed with important delay parameters. What is meant by clock skew and how does it affect the performance of sequential logic circuits?	6
	b) What is meant by path delay and critical path delay in logic network? Give illustrations.	4

	c) Compare the operation of interconnect system using SRAM, Antifuse and using Three state buffers.	6
	d) Distinguish between the performance of Transistor based and Look table based configuration of logic elements.	4
4.		
	a) State the basic difference in technology dependent and technology independent logic synthesis in FPGA fabrics.	5
	b) What is meant by logic optimization phases in logic synthesis process?	5
	c) Explain clearly the different methods or algorithm for placement and routing the basic element in FPGA after customization.	6
	d) What is meant by logic factorization and why it is required? Give illustration.	4
5.		
	a) What are the variants of two-memory architectures? Elucidate with appropriate schematic diagram and give example of each type.	8
	b) What are the factors on which design of the clock frequency of a processor depends?	4
	c) Name the different type of reset options available in an embedded processor.	2
	d) What are the different types of addressing modes available in a generalized processor? Explain in brief.	6
6.		
	Present a short comparative study between: (i) Development processor and target processor (ii) Compiler and assembler	5x4

	(iii) Microcontroller and digital signal processor (iv) Synchronous and asynchronous communication (v) Control unit and datapath	
7.		2x10
	Write short notes on any ***two***: i) Watchdog timer ii) LCD interfacing iii) Programmable Array Logic	
8.		
	a) How does a microcell add to the versatility of an embedded hardware? Explain with an example.	8
	b) How can an SRAM cell be constructed using transistors? Explain with an appropriate circuit diagram.	6
	c) Using 16-bit timer / counter develop a 32-bit timer / counter. The timer or counter should be selected by a mode selector. The input clock of the timer should be divided by a prescalar unit. Both of the timer and counter will have a programmable terminal count facility. Draw an appropriate block diagram for the entire hardware and explain your solution.	6