Ref. No.: Ex/ME/ET/T/123/2017 (Old)

B.E. MECHANICAL ENGINEERING FIRST YEAR SECOND SEMESTER EXAM. (Old), 2017

Subject: ELECTRONICS **Time: Three Hours** **Full Marks: 100**

Answer **Q. No. 1** and any **FOUR** from the REST.
(Questions must be answered serially and
All parts of the same question must be answered at one place only)

1. Answer all: **[2 Marks X 10]**
   (i) Silicon is an _____ band-gap semiconductor.
   (ii) pn-junction diodes are used as _____.
   (iii) State TRUE or FALSE: The peak inverse voltage of a bridge rectifier is double that of a full-wave rectifier.
   (iv) State TRUE or FALSE: The base of a BJT has higher doping concentration than the emitter region.
   (v) How is h_{ie} defined for a BJT?
   (vi) The positions of the capacitor and resistor must be interchanged while making differentiator and _____ circuits using an OPAMP.
   (vii) State TRUE or FALSE: The value of CMRR of an ideal OPAMP is zero.
   (viii) State TRUE or FALSE: JFET is a voltage controlled device.
   (ix) By using the method of 1's complement, subtract 1001 from 1101.
   (x) State De Morgan's theorem.

2. (a) Define i) ripple factor and ii) rectification efficiency.
   (b) Derive their expressions.
   (c) Evaluate them for a half-wave and a full-wave rectifier and compare.
   (d) The saturation current density of a Ge p-n diode at 27°C is 300 mA/m^2. What voltage must be applied to the diode to yield a forward current density of $6x10^5$ A/m^2?
   (2+2)+(1.5+1.5)+(2+2+2+2+1)+4=20

3. (a) Explain the working principle of a Light Emitting Diode with the help of a neat diagram.
   (b) A vacuum diode, the forward resistance of which is 400 ohm, supplies power o a load resistance 1200 ohm from a 250 V (rms) mains. Calculate (i) the dc load current, (ii) the ac load current, (iii) the dc voltage across the diode, (iv) the dc output power, (v) the conversion efficiency, and (vi) the percentage regulation.
   (c) Briefly explain using proper circuit and analysis, the voltage regulation performance of a zener diode. 3+(2x6)+5=20

4. (a) What do you mean by thermal runaway? How can you prevent it by self-bias circuit arrangement?

[Turn over

(b) What is the role of emitter bypass capacitor in the self-bias circuit for CE mode?

(c) Describe the performance of a common collector amplifier. Why this circuit is called an emitter-follower?

(d) A CE amplifier uses a transistor with $h_{ie} = 1k\Omega, h_{fe} = 100, h_{re} = 5\times10^{-4}$ and $h_{oe} = 25\times10^{-6}\Omega^{-1}$. The load resistance is $5k\Omega$. Find the current amplification and the overall voltage and power gains for a source resistance of $1k\Omega$. Derive the formulae you use.

(2+2)+2+(3+1)+(3x2)+4=20

5. (a) Derive the expressions for voltage gain for one stage of an RC coupled CE amplifier for all frequency ranges. Explain it graphically. Clearly mention the assumptions.

(b) Define upper and lower half power frequencies.

(c) **An RC-coupled amplifier employs two identical transistors, each having** $h_{fe} = 100$, $h_{ie} = 2k\Omega$ and $C_{ob} = 2pF$. The coupling capacitor has a capacitance $C = 0.4\mu F$. The load resistance for each transistor is $R_L = 8k\Omega$. Taking the wiring capacitance as $C_W = 10pF$, calculate the lower and upper half-power frequencies. (3x3+1+2)+2+6=20

6. (a) Define pinch-off voltage of a JFET.

(b) Explain the operation of an enhancement type MOSFET. How can we operate it in depletion mode as well? How the transfer characteristic curves would look in that case?

(c) Define FET parameters μ, r_d and g_m. Derive and draw the small signal a.c. equivalent circuit of a FET.

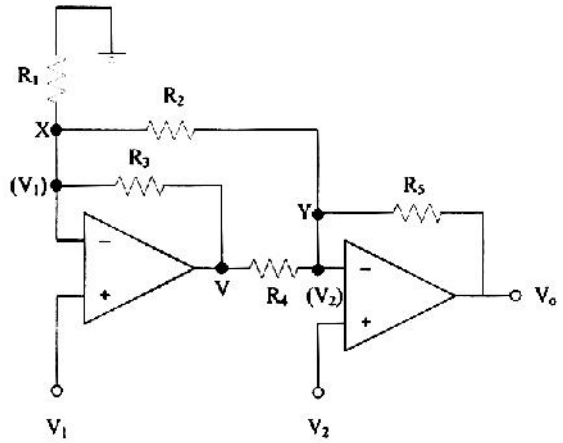
(d) Compare between JFET and MOSFET. 2+(3+2+1)+(6+3)+3=20

7. (a) State the characteristics of an ideal OPAMP.

(b) Define Common Mode Rejection Ratio. What are difference mode and common mode gains?

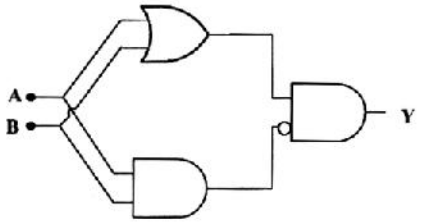
(c) Draw an adder circuit using OPAMP and explain its action.

(d) In the following circuit $R_1 = R_3 = R_4 = R_5 = 10k\Omega$ and $R_2 = 100\Omega$. Find the differential mode gain $A = \frac{V_0}{V_1 - V_2}$.



6+(2+2)+4+6=20

8. (a) Write the Boolean expression for the output Y and find the truth table. Hence identify the gate.



(b) How can NOT operation be implemented using a XOR gate?

(c) Draw a logic circuit using NOR gates to implement the Boolean expression $AB + \overline{B\overline{C}}$.

(d) The Boolean expressions of the two variables X and Y in terms of the three inputs A, B and C are given by,

$$X = ABC + A\overline{B}\overline{C} + \overline{A}B\overline{C}$$

$$Y = \left(\overline{A} + \overline{B} + \overline{C}\right).\left(\overline{A} + B + C\right).\left(A + \overline{B} + C\right)$$

What is the relation between X and Y?

(e) Prove the identities:

i) $\overline{A}BC + A\overline{B}\overline{C} + ABC + AB\overline{C} = BC + A\overline{C}$

ii) $\left(A \oplus B\right) \oplus C = A \oplus \left(B \oplus C\right)$

(2+2+1)+2+3+4+3x2=20