Ex/IT/IEE/T/123/2017

JADAVPUR UNIVERSITY

B.E. INFORMATION TECHNOLOGY

1st Year, 2nd Semester Examination - 2017

DIGITAL LOGIC & DIGITAL CIRCUIT **Time : 3 hours** **Full Marks : 100**

General instructions (read carefully)

1. Special credit will be given to answers which are brief and to the point.
2. **Answer to every question should start on a new page.**
3. **Do not write answers to various parts of a question at different locations of your answer-script.**
4. The final answer (numerical values with unit) should be underlined **or** enclosed within a box.
5. Do not write on the front back cover of your answer booklet.

Question No. 1 is compulsory. Answer any 4 (four) from the rest.

Each question carries 20 marks. Question for each sub-part is mentioned at the right margin of a part question or set of part questions.

1. Answer ***any 10 (ten)*** of the following questions. Be specific and very brief in answering each question. (10 X 2)

i) What is $(0.375)_{10}$ in binary number system ?
ii) What is the signed 2's complement representation of $(-15)_{10}$?
iii) If $(84)_x$ in base x number system is equal to $(64)_y$ in base y number system, then what are the possible values of x and y ?
iv) Simplify $A' \oplus B'$.
v) What is the max term corresponding to decimal 12 ?
vi) The output Y of a 2-bit comparator is logic 1 whenever the 2-bit input A is greater than the 2-bit input B. The number of combinations for which the output is logic 1 is ?
vii) The revamped Eden Gardens has a capacity of 66,349 spectators. We need to design a ripple counter using JK flip-flops to count the number of spectators attending a cricket match. How many such flip-flops are required ?
viii) What is the effect of the CLEAR signal on the output of a JK flip-flop ? Why is it called an overriding input ?
ix) A 5 bit modulo 32 ripple counter uses D flip-flops. If the propagation delay of each flip-flop is 25 ns, what is the maximum clock frequency that can be used ?

x) A 4 bit synchronous counter uses flip-flops with propagation delay of 2 ns each. What is the maximum time required for change of state ?

xi) The present state, Q of an edge triggered JK flip-flop is logic 0. If J = 1, then what will be the next state Q^+ ?

xii) Distinguish between volatile and non-volatile memory with examples.

xiii) Which digital logic family has the highest speed ? At the expense of what other parameter (any one) ?

xiv) In recent times, which digital logic family is most extensively used to build VLSI devices and why (any three points) ?

2. i) Simplify the following functions using Karnaugh map, and design the circuit using basic fundamental gates. List the inventory required in the implementation. (2 X 7)

a) $F(A, B, C, D) = \sum m(1, 3, 4, 5, 9, 11, 14, 15) + \sum d(2, 6, 7, 8)$

b) $F(A, B, C, D) = \prod M(0, 1, 3, 8, 10, 15) . \prod d(11, 13, 14)$

ii) Explain why we use Gray code instead of natural binary code while minimizing logic circuits using Karnaugh map. (2)

iii) Distinguish between implicant, prime implicant and essential prime implicant. (3)

iv) Which minimization method is used, when the number of variables is more than six ? (1)

3. i) The multiplexer shown in Fig. 1 is a 4 x 1 multiplexer. What is the output Z in terms of A, B, C (after simplification using Boolean algebra) ? (4)

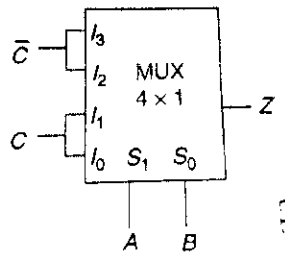

Fig 1

ii) Implement a 4-bit adder-subtractor using Full Adders. (4)

iii) Implement the digital circuit of a full subtractor using (12)

a) only logic gates
b) 4 X 1 multiplexer
c) 3 to 8 decoder.

4. i) Design an asynchronous modulo 10 (decade) counter using JK flip-flops. (8)

ii) Draw the circuit diagram of a JK master-slave flip-flop and explain its operation. How is racing avoided in such a flip-flop ? (8)

iii) Mention any two applications of flip-flops. (2)

iv) Mention any two applications of shift registers. (2)

5.

(5 X 4)

i) Consider the circuit in Fig. 2. What is the next state Q^+ in terms of P and Q ? Hint : For all possible combinations of P and Q, make a table of S, R and Q^+. Find how Q^+ is related to P and Q from the table.

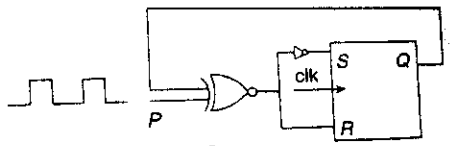

Fig. 2

ii) The counter shown in the Fig. 3 has initially $Q_2\ Q_1\ Q_0 = 0\ 0\ 0$. What will be the status of $Q_2\ Q_1\ Q_0$ after the first pulse ?

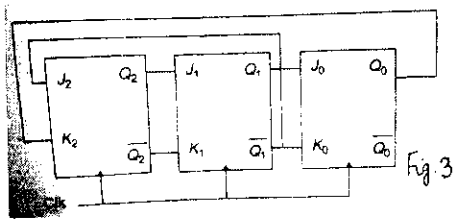

Fig. 3

iii) In the modulo 6 ripple counter shown in the Fig. 4, the output of the 2-input gate is used to clear the JK flip-flops. What gate is the 2-input gate ?

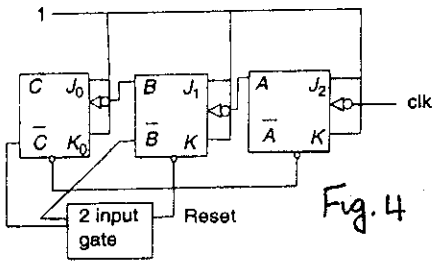

Fig. 4

iv) For a shift register as shown in Fig. 5, X = 1 0 1 1. With initially all the flip-flops cleared, what will be the value of ABC after 3 (three) clock pulses ?

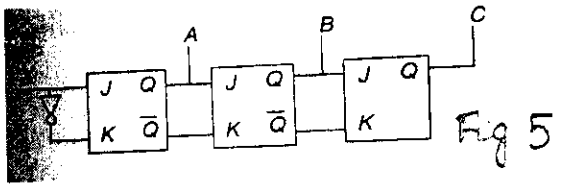

Fig 5

v) Fig. 6 is that of a ripple counter using positive edge triggered flip-flops. If the present state of the counters is $Q_2\ Q_1\ Q_0 = 0\ 1\ 1$, what will be the next state of $Q_2\ Q_1\ Q_0$?

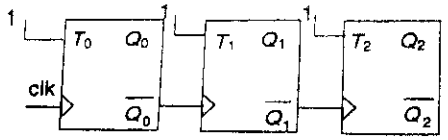

Fig. 6

6. i) Draw and explain the generalized model of a state machine using D flip-flops. (6)

ii) Implement an arbitrary sequence counter to count 1, 4, 3, 5, 2, 6 using the generalized model of a state machine using JK flip-flops. Draw the state graph / diagram, write the state table and transition table. Design the combinational / steering circuit. (14)

7. i) Minimization of digital logic circuits results in reduced hardware. What are the benefits associated with reduced hardware in a digital system ?

ii) Draw the symbol, logical equation and truth table of a coincidence (or equivalence) gate.

iii) What is DeMorgan's Theorem ?

iv) Design a 16 X 1 multiplexer using only 4 X 1 multiplexers.

v) What are tri-state gates ?

vi) Draw the circuit diagram and write the characteristic table for S'R' latch using NAND gates.

vii) How does PROM, PLA and PAL vary in terms of fixed and programmable AND and OR gate arrays ?

viii) Distinguish between ROM, EPROM, E^2PROM and flash memory. (8 X 2.5)

8. Write short notes on ***(any five)*** (5 X 4)

i) Implementation of NOT, AND and OR function using any of the universal gates.
ii) 3 (three) bit binary to gray code converter.
iii) Full adder.
iv) Excitation table and state diagram of a SR flip-flop.
v) PLA (Programmable Logic Array).
vi) Fan out.
vii) Noise margin.

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