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EX/ET/T/414/2017(S)

B. ETCE 4TH YEAR 1ST SEMESTER SUPPLEMENTARY EXAMINATION 2017

VLSI DESIGN Time: Three Hours Full Marks: 100

Answer any ***Five*** questions.
All questions carry equal marks.

1. a) Discuss about the salient features of the VTC of CMOS inverter and hence explain how the same could be achieved experimentally in the laboratory. 10 + 6

   b) Determine the power dissipated in a CMOS inverter having a supply voltage of 5V operating at 25 MHz with a load capacitance of 0.05 pF. 4

2. a) Draw the logic diagram of 5-input CMOS NAND gate and also the corresponding stick representation. 3 + 3

   b) Write down the Truth Table for 3-input Majority Function and hence justify the name "Majority Function". 2 + 2

   c) Derive the CMOS network for the Majority Function and justify the functionality of the derived network in the light of Part 'b'. 6 + 4

3. a) Discuss about the structure of CMOS network for arbitrary combinational function. 8

   b) Explain the procedure to derive the CMOS network for the function f = a'b'c' + a'bc + ab'c' + ab'c + abc and also draw the derived CMOS network. 7 + 5

4. a) Explain how a 2 X 1 MUX could be realized out of a CMOS inverter. 6

   b) What is CMOS 2-input Universal Logic Module? Explain how different combinational logic functions could be realized by the Universal Logic Module. 3 + 11

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5. a) Explain the basic features of 2n-bit input and n-bit output Barrel Shifter. 10

b) Discuss about the algorithm for the implementation of 4 X 4 Barrel Shifter with wraparound feature having four control inputs. 10

6. a) Convert the function $f = \overline{[\,(ab + c).(d + e\,)]}$ into Bubbled-input form. 5

b) Convert the CMOS static circuit realizing AND-OR-INVERT function into corresponding NMOS based dynamic counterpart. 8

c) Explain the functionality of Two Phase dynamic NMOS inverter. 7

7. a) Discuss about the reasons and also the effect of Clock Skew in CMOS Dynamic circuits. 12

b) Explain how Domino CMOS circuit could be utilized to solve for Clock Skew problem. 8

8. Write short notes on any ***Two*** of the following: 10 + 10

a) Systolic Array Multiplier

b) Charge sharing problem

c) Arrangement of operands in 2-D Systolic Array

d) CMOS Transmission Gate