B. ETCE 3RD YEAR 2ND SEMESTER EXAMINATION-2017

Subject: IC DESIGN Time: 3 Hours Full Marks: 100

All parts of the same question must be answered at one place only

Model parameters for NMOS and PMOS device

Parameters	NMOS	PMOS
L_{min}	180nm	180nm
W_{min}	240nm	240nm
V_{th}	0.7V	-0.8V
λ (V^{-1})	0.1	0.2
μ (cm^2/Vs)	350	100
C_{ox} ($fF/\mu m^2$)	6	6

PART-I

1. Answer **any Five** Questions: [Marks: 5×8=40]

A) What is body effect? How does it influence the threshold voltage of a MOS transistor?

B) What is channel length modulation effect? How the voltage current characteristics are affected because of this effect?

C) What is trans-conductance of a MOS transistor? Explain its role in the operation of the transistor.

D) Draw the ideal characteristics of a CMOS inverter and explain the different parts of the characteristic based on the operation point of those MOSFETs

E) What is the inversion voltage of an inverter? Find out the expression of the inversion voltage of a CMOS inverter.

F) Explain why the structures shown below cannot operate as a current source even though the transistors are in saturation.

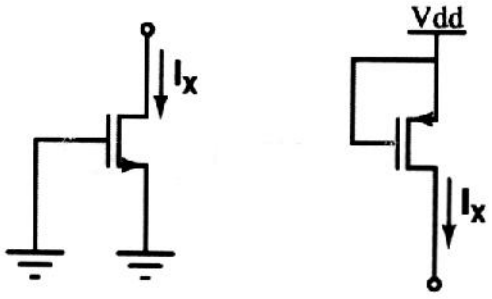

Figure 1

PART-II

(Answer any Three)

2. Find the gain expressions of the amplifier circuits shown below. [Marks: 2×10 =20]

A) Consider $\lambda \neq 0$ and $\eta \neq 0$.

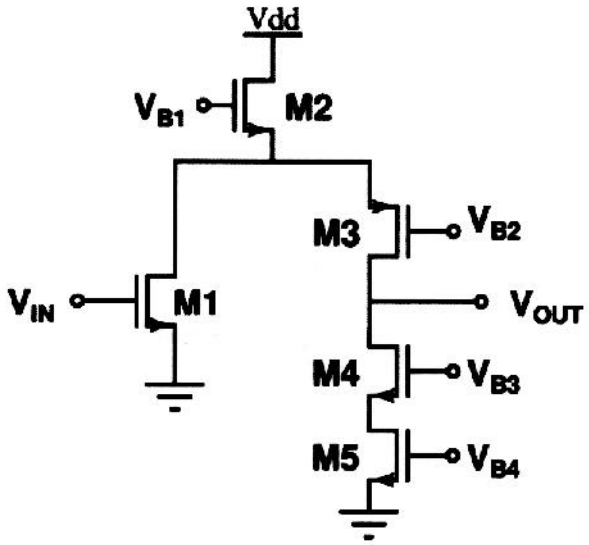

Figure 2

B) Consider $\lambda \neq 0$ and $\eta = 0$.

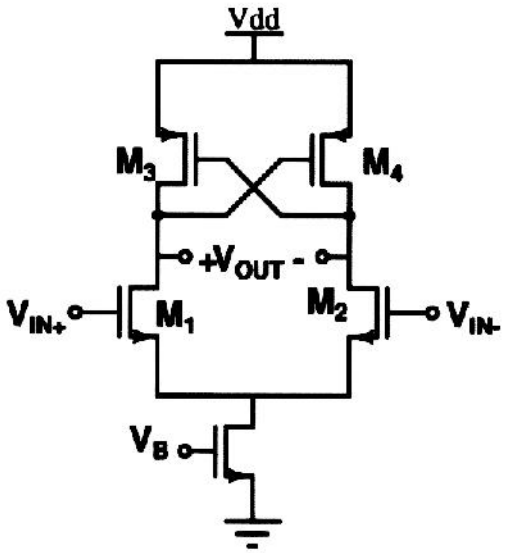

Figure 3

3. A) Design one cascode current mirror with output resistance not less than 1 MΩ. Find the maximum voltage variation at the output node of the current mirror. [Marks: 13+2=15]
   B) Sketch $\mathbf{V_X}$ and $\mathbf{V_Y}$ as a function of V_{DD} for the circuit shown below. Assume the transistors in the circuit are identical. [Marks: 5]

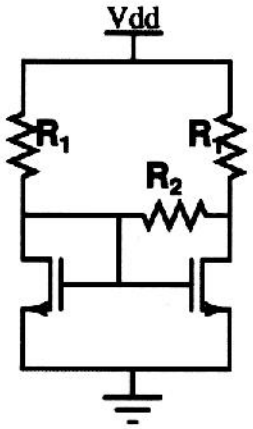

Figure 4

4. Find $\mathbf{I_X}$ vs $\mathbf{V_X}$ plot of the circuit shown below. Where V_X is varied from 0V to 3V *(Consider supply voltage V_{dd}= 3V)* [Marks: 2×10 =20]
   A)

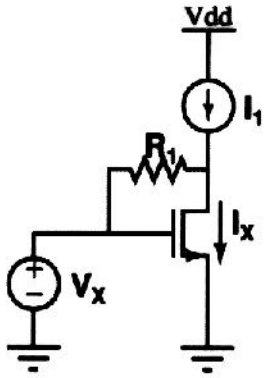

Figure 5

B)

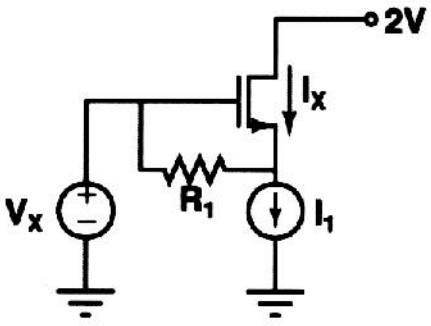

Figure 6

5. Find the Voltage V_X plot of the circuit with respect to time. *(Consider zero charge on the capacitor at t=0).* [Marks: 2×10 =20]

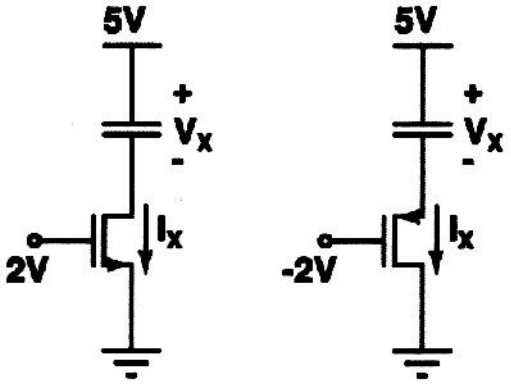

Figure 7

6. Design a cascode amplifier *(as shown below)* with PMOS active load for a voltage gain more than 10000. *(Supply voltage to the circuit is 1.8V)* [Marks: 20]

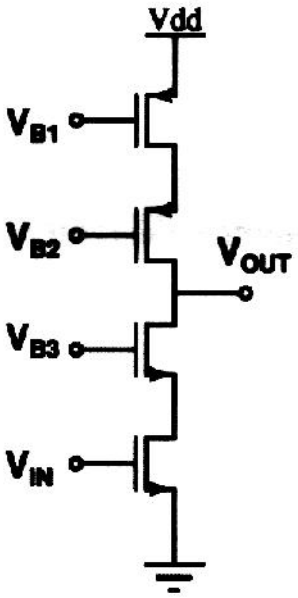

Figure 8