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DIGITAL LOGIC CIRCUITS

Time: 3 hours   Full Marks : 100

Answer any *five* questions
All questions carry equal marks

1. (a) Obtain the maxterm and minterm representations of the following Boolean function.

   $$f(A, B, C) = A' + B + A C$$

   (b) Obtain the simplified expression for the following Boolean function using K-map.

   $$f(A, B, C, D) = \Sigma (5, 6, 7, 9, 10, 11, 13, 14, 15)$$

2. (a) Design a 8:1 Multiplexer using SSI gates and explain its working principle.

   (b) Realize the following Boolean function using multiplexers.

   $$f(A, B, C) = AB + BC + AC$$

3. (a) Design a 4-bit binary adder and explain its working principle.

   (b) Realize the following functions using a decoder and minimum number of SSI gates.

   $$F_1 (A, B, C) = A' C + B C$$

   $$F_2 (A, B, C) = A B + A C$$

4. (a) Design a 5-bit magnitude comparator circuit using one 7485 IC and other SSI gates if required and explain the design steps.

   (b) Design a 10-bit parity checker circuit using one 74180 IC and other SSI gates if required and explain the design steps.

5. (a) Draw the circuit diagram of a SR flip-flop using NAND gates only, explain its operation and hence obtain the truth table.

(b) Convert a T flip-flop into a JK flip-flop. Obtain an expression for f_{max} of the resulting circuit.

6. (a) Design a 3-bit register with LOAD control line and explain its operation.

(b) Design a 3-bit twisted ring counter and explain its operation with the help of a timing diagram. Mention the advantages of a twisted ring counter.

7. (a) Design a mod-6 ripple counter using JK flip-flops. Consider low active CLR lines for your design. How will you modify the design if low active PRESET lines are available?

(b) Design a mod-6 synchronous up / down counter using JK flip-flops.