Ref. No.: Ex/ET/T/221/2017

B.E. ELECTRONICS AND TELE-COMMUNICATION ENGINEERING

SECOND YEAR SECOND SEMESTER EXAM, 2017

ANALOG CIRCUITS- II **Time: Three hours** **Full Marks: 100**

Use a separate Answer-Script for each Part

PART-I

Answer ***Q.1***, any ***four*** from ***the rest*** [10+4×15=70]

1. Answer any ***five*** from the following : [5×2=10]
   a) Why is the biasing of EMOSFET different from DMOSFET?
   b) Write the advantages of RC coupling over transformer coupling.
   c) In which frequency range tuned amplifiers are used? Explain.
   d) Why is the 2nd order harmonic distortion important in an amplifier?
   e) Define line regulation of voltage regulator.
   f) Define quality factor (Q) and skirt selectivity (S) of tuned amplifier.
   g) Define free running frequency of phase locked loop.

2. a) Find the overall voltage gain in dB of the amplifier (Fig.1). Briefly explain how can maximum voltage gain be obtained from the amplifier.
   b) If a transformer coupled loudspeaker (16 Ω) is used as load, find the primary to secondary turns ratio of the transformer output impedance of Q_2 is 10 kΩ.
   c) Why does transformer coupling give poor frequency response ? [8+2+2+3]

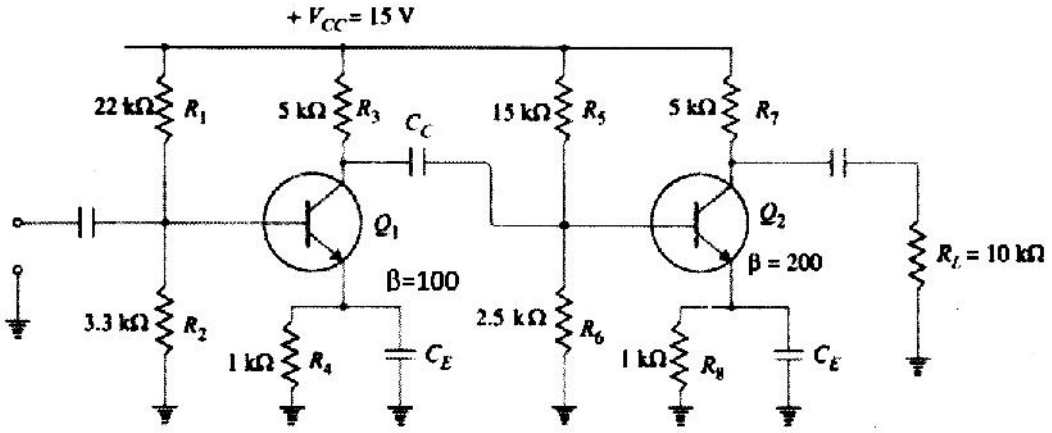

Figure 1

[Turn over

3. a) What do you mean by nonlinear distortion in a transistor amplifier? If the dynamic characteristic is given by a parabolic form ($A_0x+B_0x^2$) and input is a pure sinusoid, how will the output be modified? Derive the form of 2nd order harmonic distortion. [2+4+3]

   b) In an amplifier, fig. 2, the output current I_Y = (35 +17cos w_ot+10cos2w_ot +0.3 cos3w_ot) mA. (i) Tolal distortion D, (ii) Total power delivered to the load of 2.2 KΩ and (iii) power delivered to the load for fundamental frequency. [6]

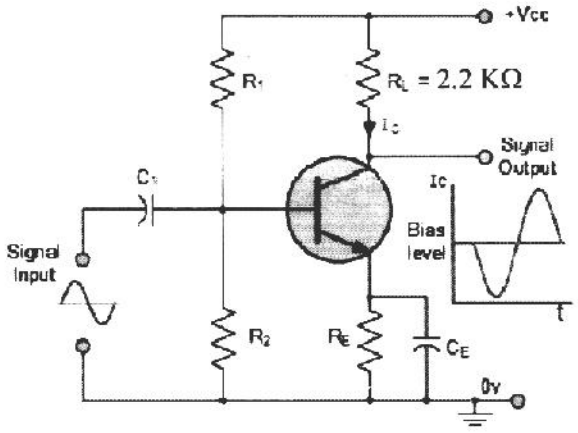

Figure 2

4. a) Define class C power amplifier. Explain the purpose of tuned circuit in class C amplifier. [2+3]

   b) In a class C amplifier (Fig.3), tuned circuit at the collector consists of inductor of value 20 μH and capacitor of 1 μF. The transistor is ON for 1 μs. Icsat=100 mA, V_{CEsat} = 0.2 V. R_L =100 Ω. Determine the efficiency. If an input signal of 1 kHz is used, determine the value of the inductor and efficiency. Comment on it. [3+4+3]

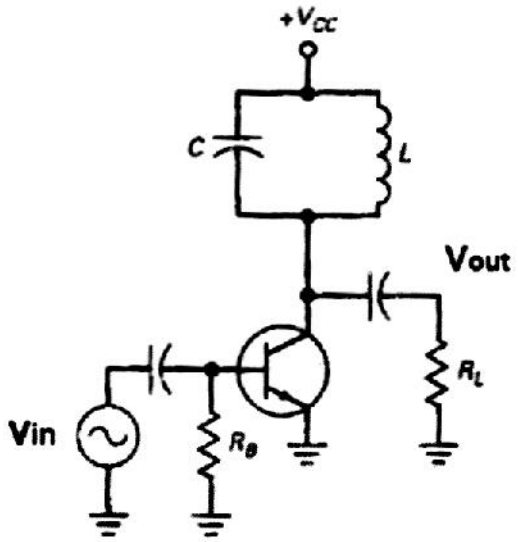

Figure 3

5. a) Give the analysis of step up switching voltage regulator and determine the power efficiency. [8]

   b) Explain the operation of LM317. [4]

   c) In an IC adjustable linear positive voltage regulator V_{outmax} = 37 V, I_{adj} = 50 μA and R_1 = 200Ω. Calculate the maximum value of R_2. [3]

6. a) Explain with circuit diagram the operation of single tuned amplifier. Draw its ac equivalent circuit and calculate voltage gain. [4+6]

   b) Draw and explain the normalized gain vs. frequency curve of double tuned amplifier for different coupling co-efficient. [5]

7. Short note [3×5=15]

   a) Lock –in range and capture range of PLL

   b) Shunt voltage regulator

   c) Cross over distortion

PART-II

Answer any 2 (Two) from the followings: (15×2 =30)

8. Pin diagram of an IC Timer 555 is given below. Draw the **Internal Architecture** of the IC. [Marks:5]

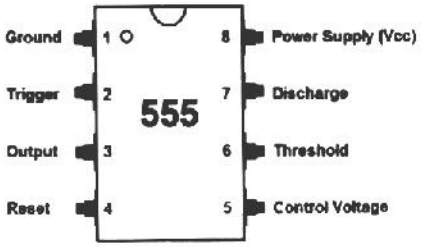

Figure 4

Using 555 **Implement** a monostable multivibrator and plot the following waveforms with explanations: $V_{Trigger}$, V_{Cap}, $V_{ff\text{-}Set}$, $V_{ff\text{-}Reset}$ and V_{Out}. Find the value of external components so that the unstable state sustains for 1msec. *(Assume the SR flip-flop used in the IC is a positive edge trigger FF and the IC is using a 5V supply voltage)* [Marks: 3+5+2]

9. **Explain** the working principle of the voltage controlled oscillator shown in Figure 5. Derive the expression for T_L and T_H. Find the **condition** for 50% duty cycle. If the input voltage to the circuit is 4V and the supply voltage of each Op-amp is ±12V plot V_{Cap} *(voltage across the capacitor)*, V_{Out1} and V_{Out2} with respect to time. [Marks: 4+(2+2)+1+(2x3)=15]

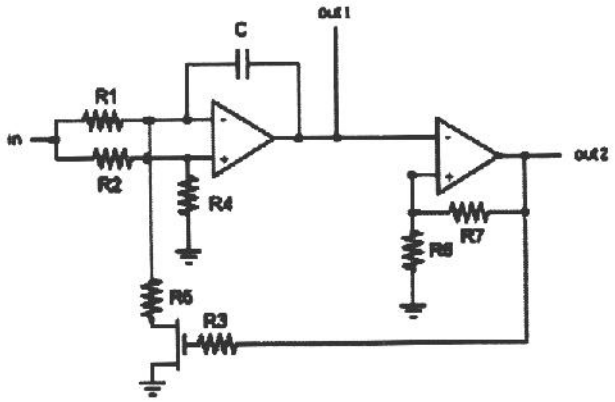

Figure 5

10. A) An astable multivibrator circuit is modified as shown in the figure 6. Assume the diode shown in the figure is ideal. Plot waveforms V_{o1}, V_{o2}, V_{x1} and V_{x2} with respect to time (*use proper labels, shapes and maintain approximate visualization of duty cycle and voltage values in your plot*). Calculate the **time period** and **duty cycle** of the output waveform V_{o2}.

[Marks: (2+2+2+2)+(1+1)=8]

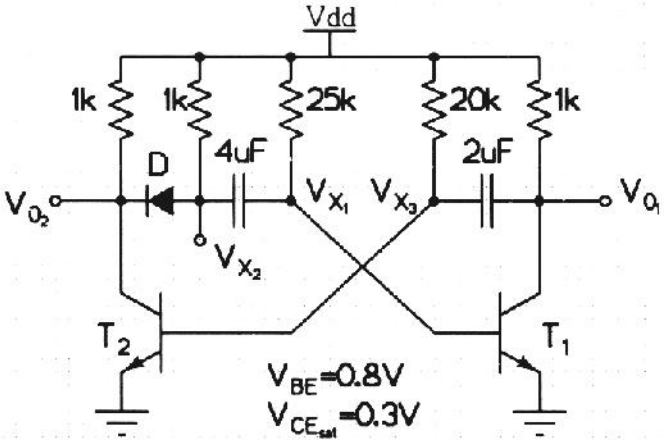

Figure 6

B) For the circuit shown below determine the **oscillation frequency** and **amplifier gain** for sustained oscillation. *(Amplifiers are ideal and identical)* [Marks: 5]

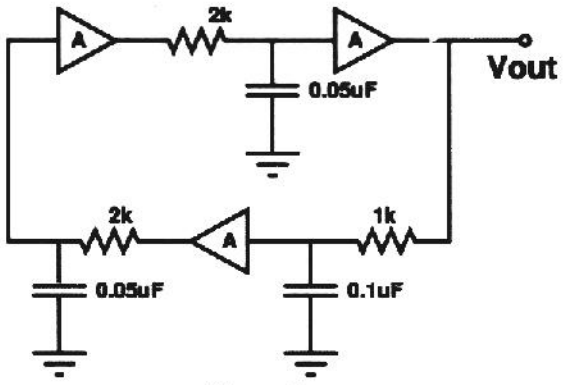

Figure 7