Ref. No.: EX/ET/T/215/2017(4)

# B. ETCE 2<sup>ND</sup> YEAR 1<sup>ST</sup> SEMESTER SUPPLEMENTARY EXAMINATION 2017

**Subject: ANALOG CIRCUITS-I** 

Time: 3 Hours

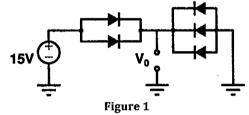
Full Marks: 100

All parts of the same question must be answered at one place only
Use separate answer script for each PART

### PART-I

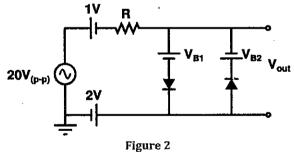
### (Answer any Five Questions)

- 1. Explain the working principle of a voltage multiplier with proper circuit diagram. [Marks: 10]
- 2. Explain the working principle of a half wave rectifier. Find  $V_{dc}$ ,  $V_{rms}$  and efficiency( $\eta$ ) of a half wave rectifier. [Marks: 10]
- 3. Find the output voltage  $V_0$  of the diode circuit shown below and **plot** the output voltage for a temperature range 0 to  $100^{\circ}$ C. [All diodes are real and identical] [Marks: 6+4=10]



- 4. A) Draw the output waveform of the circuit shown below. ( $V_{B1}=2V$ ,  $V_{B2}=3V$  and diodes are real)
  - B) Determine the minimum or maximum value of  $V_{B1}$  and  $V_{B2}$  to avoid the clipping of output waveform.

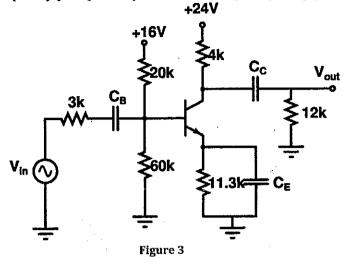
    [Marks: 6+4=10]



- 5. Determine the expression of stability factor S(Ico) for a voltage divider network. [Marks: 10]
- **6.** Explain the function of a current mirror circuit. Design one current mirror with  $1\mu A$  current in primary branch and  $0.75 \,\mu A$  in secondary branch. (Available transistors are identical with  $\beta$ =1000 and  $V_{BE}$  =0.7V. Supply voltage 3V)

- 7. One CE amplifier with proper biasing arrangement is shown below. Find the following parameters:  $[\beta = 100, C_E = C_C = C_B = 1 \, \mu F \, and \, neglect \, r_o]$ 
  - A) All low frequency poles and zeros due to coupling capacitor and lower cut-off frequency.
  - B) Gain versus frequency plot (for very low to mid frequency range)

[Marks: 7+3=10]



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## B. ETCE 2<sup>ND</sup> YEAR 1<sup>ST</sup> SEMESTER SUPPLEMENTARY EXAMINATION-2017

Subject: ANALOG CIRCUITS - I

Time: 3 Hours

Full Marks: 100

### **PART-II**

### Answer any FIVE.

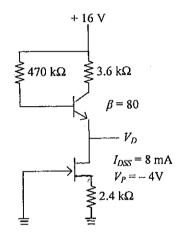
All parts of the same question must be answered at one place only.

1. Explain the operation of an n-channel JFET.

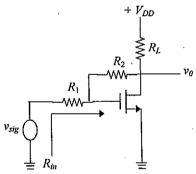
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2. Determine  $V_D$ .

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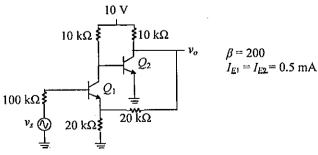


3. Find  $v_0/v_{sig}$  and  $R_{in}$  of the following circuit with  $g_m=1$  mA/V,  $r_0=100$  k $\Omega$ ,  $R_L=10$  k $\Omega$ ,  $R_1=500$  k $\Omega$ ,  $R_2=1$  M $\Omega$ .

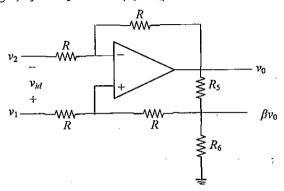


4. Determine the feedback configuration of the following circuit and hence quantitatively explain how the feedback connection helps in improving the behavior of the circuit as an ideal source.

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- 5. Explain how a differential amplifier with active load and Wilson current mirror can achieve a near ideal value of CMRR.
- 6. Assume that  $R_5$  and  $R_6$  of the following circuit are much smaller than R so that the current through R is much lower than the current in the voltage divider, so that  $\beta = R_6/(R_5 + R_6)$ . Show that the differential gain is given by  $A_d = 1/(1-\beta)$ . Also design the circuit to obtain  $A_d = 10$ ,  $R_{id} = 2 \text{ M}\Omega$  by selecting R,  $R_5$  and  $R_6$  such that  $(R_5 + R_6) \leq R/100$ .



7. Explain the operation of a monostable multivibrator.

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