B. ETCE. ENGG. EXAMINATION 2017

(1st Year, 2nd Semester)

ELECTRON DEVICE

Full Marks : 100 Time : Three hours

The figures in the margin indicate full marks.

Answer ***any five*** questions.

(*All parts of the same question must be answered together*)

1.(a) What is the Ideal diode approximation? Describe how the *I-V* relation for an ideal diode gets modified in case of a real one. 2+8

(b) Discuss influence of temperature variation on the diode forward and reverse characteristics. 6

(c) Derive an expression for built-in potential for a *pn* junction. 4

2. Sketch the following:

(a) Minority carrier distribution across a p^+n junction under 12

(i) equilibrium
(ii) forward bias
(iii) reverse bias

in addition to the corresponding energy band diagrams.

(b) Minority carrier distribution in a *pnp* transistor biased to operate in 8

(i) cut-off
(ii) active
(iii) saturation regions.

3.(a) For an *npn* transistor, draw and explain the static input and output characteristics with different regions labeled on them. 5+7

(b) Determine the biasing condition of a *Si npn* transistor if 8

(i) $V_{BE} = V_{CE} = 0.7$ V

(ii) $V_{BE} = 0.7$ V and $V_{CE} = 0$ V

(iii) $V_{CE} = V_{CC}$

Draw an appropriate diagram and locate the Q - point in each case.

4. (a) Define and classify Heterojunction. 8

(b) Describe how heterojunction can be employed in improving performance of 5+7

(i) LED

(ii) BJT

Specify what type of heterojunction is useful in each of the above cases.

5. (a) Compare the following devices along with their equivalent circuits: 5+8

(i) *pn* junction diode and Schottky diode

(ii) BJT and FET

(b) Explain how the channel gets pinched off in a 3+4

(i) JFET

(ii) MOSFET.

6.(a) Derive the general expression for the current flowing through an *n*-channel JFET. Make approximation necessary for that. 10

(b) Describe the structure and operation of a power POSFET. Explain how it becomes fast. 7+3

7.(a) Explain the working principle of: 2x4

(i) Photodiode

(ii) Opto-isolator.

(b) Draw the schematic structure and *I-V* characteristic (no explanation required) of: 4x3

(i) Shockley diode

(ii) DIAC

(iii) PUT

(iv) UJT.

8. Write notes on (**any two**): 2x10

(a) Technique for single crystal growth

(b) Tunnel diode

(c) UJT

(d) CMOS Inverter.