Ref No: Ex/EE/5/T/222/2017

B.E. ELECTRICAL ENGINEERING (PART TIME) - SECOND YEAR - SECOND SEMESTER

~~(1st-~~/ 2nd Semester/~~Repeat/Supplementary/Annual/Bi-Annual)~~

SUBJECT: - SEQUENTIAL SYSTEMS AND MICROPROCESSOR

Full Marks 100

Time: Three hours (50 marks for each part)

Use a separate Answer-Script for each part

No. of Questions	PART I	Marks
	Answer any three Questions Two marks are for neat and systematic answers	
Q1.	a) Enumerate the advantages of programmable logic over a relay logic based system.	4
	b) A system is described by, Y=A(B+C)+B.(A+AB) i) Simplify the system using Boolean Algebra ii) Implement the simplified expression through ladder diagram. iii) Implement the original expression through ladder diagram.	2+4+6
Q2.	a) Draw the block diagram of a Moore machine and describe the functions of each block. Enumerate the differences between Moore and Mealy Machine.	8
	b) Draw and explain the block diagram of a 4-bit shift left register using D-FF having serial loading facility.	8
Q3.	a) What is the difference between the excitation table and truth table? With help of truth tables develop the excitation tables of J-K and S-R FFs.	4+6
	b) What is state diagram? Explain different symbols that are used to draw state diagram of a sequential system.	6
Q4.	a) Define Read Cycle time, Write Cycle time and Access time in the context of the specifications of a memory chip.	8
	b) A 512X8 bit Read and Write Memory (RWM) is to be designed for using 512X4 bit memory chips. Sketch the connection diagram for the designed memory chip and the possible page address.	8

[Turn over

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No. of Questions	PART I	Marks
Q5.	a) Draw the PLC Ladder diagram for a DOL starter with forward/reverse option for three phase induction motor having the following description: The motor will be ON in forward mode when START button is pressed. The system is having a STOP switch and an overload protection for safety purpose. The motor can be run in reverse direction when reverse button is pressed. Indicate the inputs and outputs to the PLC system and also draw the power circuit diagram for the system. b) What are field switches? Name four field switches that are used in PLC based system.	12 4

Ex / EE / 5 / T / 222 / 2017

BACHELOR OF ELECTRICAL ENGINEERING (PART TIME) EXAMINATION – 2017
(2nd Year, 2nd Semester)

SEQUENTIAL SYSTEMS AND MICROPROCESSOR

Time: **3** hours (**50** marks for each Part) Full marks: **100**
Use a separate Answer-Script for each Part

PART-II

*Answer any **three** questions.*
***Two marks** are reserved for neatness and well organized answers.*

1. (a) Draw the functional pin diagram of the 8085 microprocessor. **[8]**
   (b) Describe the control and status signals in the 8085 microprocessor mentioning the functionality of each one of them. **[8]**

2. (a) What are the different machine cycles available in the 8085 microprocessor? **[3]**
   (b) Describe how the status signals IO/$\bar{M}$, S0 and S1 are used in identifying the individual machine cycles. **[5]**
   (c) With a functional block diagram and the corresponding timing diagram, discuss the Opcode Fetch cycle associated with the instruction `MOV B,A`. **[8]**

3. (a) How are the data and the lower order address buses demultiplexed in the 8085 microprocessor? **[6]**
   (b) Discuss the sequence of operations that take place when the CALL instruction is executed in the 8085 microprocessor. **[5]**
   (c) What will be the clock frequency of an 8085 microprocessor if a 2 MHz crystal oscillator is connected across its pin-1 and pin-2? Under this condition, what will be the execution time for the instruction `LXI H, C050`? **[1 + 4]**

4. (a) Describe the operating modes of 8255. **[5]**
   (b) Discuss the control word format in the BSR mode of 8255. Explain how the different ports and control words are selected for 8255. **[3 + 5]**
   (c) Write a BSR control word to set bits PC7 and PC0 and to reset them after 1 second delay. The address of control word register (CWR) is 83H. **[3]**

5. (a) Write an assembly language programme for the 8085 microprocessor to multiply two 8-bit unsigned integers where the product is expected to be 16-bit by implementing bit-shift operations. **[8]**
   (b) Write an assembly language programme for the 8085 microprocessor to generate the first thirteen numbers in the Fibonacci series and store them in consecutive memory locations starting from C050. **[8]**