Ref No: Ex/EE/5/T/222/2017

B.E. ELECTRICAL ENGINEERING (PART TIME) - SECOND YEAR - SECOND SEMESTER (OLD)
(1st / 2nd Semester/Repeat/Supplementary/Annual/Bi-Annual)

SUBJECT: - PROG. LOGIC AND SEQUENTIAL SYSTEMS

Time: Three hours

Full Marks 100
(50 marks for each part)

Use a separate Answer-Script for each part

No. of Questions	PART I	Marks
	Answer any three Questions Two marks are for neat and systematic answers	
Q1.	a) Describe Rung, Timer and Counter operation in the context of Ladder diagram.	4
	b) Simplify and realize through relay logic the system described by Y=A+B.(B+C+A).	6
	c) Explain propagation delay time, Set-up time and Hold time with respect to operation of a FF.	6
Q2.	a) Draw and describe the structure of the Moore Machine model and enumerate its difference with Mealy machine.	8
	b) Describe with suitable block diagram how a D-FF can be realized with he help of a state machine model. Also mention the type of the state machine equivalent to the D-FF.	8
Q3.	a) Describe the operation a 4-bit Shift Register with parallel and serial loading capability with suitable circuit diagram.	8
	b) Describe state diagram and state table. Explain different symbols that are used to draw state diagram of a sequential system.	4+6
Q4.	a) Define Read Cycle time, Write Cycle time and Access time with respect to the specification of memory chip.	6
	b) Design a 1024X8 bit Read and Write Memory (RWM) chip using 256X4 bit memory chips. Draw and explain necessary circuit diagram.	10

[Turn over

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No. of Questions	PART I	Marks
Q5.	a) Draw a Ladder diagram to implement through a PLC system the DOL starter of three phase induction motor. The starter is also fitted with STOP and OVERLOAD protection.	10
	b) Name two field switches that can be connected to PLC Digital Input Modules and two field devices that can be connected to PLC Analog Input Modules.	6

EX/EE/5/T/222/2017(OLD)

BACHELOR OF ELECTRICAL ENGINEERING (PART TIME) EXAMINATION, 2017(OLD)

(2nd Year, 2nd Semester)

PROGRAMMABLE LOGIC AND SEQUENTIAL SYSTEMS

Time: Three hours (50 marks for each part) Full Marks: 100

Use a separate Answer-Script for each part

PART - II

Answer question no. 1 and any *two* form the rest of the questions.

1. Answer any five of the following questions. (5 x 2)
   I. What is Fixed Function IC?
   II. Name different switching techniques employed in configurable hardware.
   III. What are the programming techniques available for CPLDs?
   IV. What is JTAG port?
   V. What is Macrocell?
   VI. Name different technologies adopted in FPGA.

2. (a) Describe the FAMOS technology for the fabrication of programmable memories. (10)

   (b) Write down the advantages and disadvantages of Fixed Function ICs and ASICs. (10)

3. (a) Illustrate with relevant circuits the operation of a PAL device. (10)

   (b) Develop a full adder by using PLA device. (10)

4. (a) Discuss the functionality of different stages for simulation and synthesis in a typical CAD system (10)

   (b) Implement a logic function $f= ab+\bar{c}$ using transistor pair logic and basic small gates employed in FPGA. (10)

5. (a) Develop an AND gate by using VHDL program. Draw approximate timing diagram of the input signals which can be applied in the AND gate. Write a test bench program to these input signals. Draw the waveform of output signal. (15)

   (b) Name the different states available in VHDL as per IEEE standard. (5)