Ref No: Ex/EE/T/226/2017

B.E. ELECTRICAL ENGINEERING - SECOND YEAR - SECOND SEMESTER (OLD)

(1st / 2nd Semester/~~Repeat/Supplementary/Annual/Bi-Annual~~)

SUBJECT: - PROGRAMMABLE LOGIC AND SEQUENTIAL SYSTEMS

Full Marks 100

Time: Three hours (50 marks for each part)

Use a separate Answer-Script for each part

No. of Questions	PART I	Marks
	Answer any three Questions Two marks are for neat and systematic answers	
Q1.	a) A system is described by, Y=AB+A.((A+B)+AB) i) Implement the simplified expression through digital circuit. ii) Implement the above expression through ladder diagram. iii) Implement the simplified expression through ladder diagram.	6+6+2
	b) What are field switches? Name four field switches that are used in PLC based system.	4
Q2.	a) Draw the basic block diagram of a Mealy machine and describe the functions of each block.	8
	b) Draw and explain the block diagram of a 4-bit controlled shift left register using D-FF.	8
Q3.	a) Show with suitable sketch how a common bus can be shared for data transfer between three different 4-bit registers. Show the instructions to transfer a data of 1001 between any two registers sharing a common bus.	4+4
	b) Explain the functions of different symbols that are used to draw state diagram of a sequential system.	8
Q4.	a) Define Read Cycle time, Write Cycle time and Access time with respect to the specification of a memory chip.	6
	b) Design a 1024X8 bit Read and Write Memory (RWM) chip using 512X4 bit memory chips. Sketch the final memory system taking any starting address.	8
	c) Explain the function of Chip Select signal with respect to a memory chip.	2

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No. of Questions	PART I	Marks
Q5.	a) Draw the Ladder diagram to implement a forward/reverse starter of a DC motor having following functions: The motor will run forward when FWD button is pressed and will run in reverse direction when REV button is pressed. The system is fitted with STOP button to stop the rotation while running in any direction and overload protection for safety purpose.	10
	b) Draw power circuit diagram and indicate the inputs and outputs to PLC for the above system.	6

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B. E. ELETRICAL ENGG SECOND YEAR SECOND SEMESTER
EXAMINATION 2017 (OLD)

PROGRAMMABLE LOGIC AND SEQUENTIAL SYSTEM

Time: Three hours Full Marks: 50

(50 marks for each part)
Use separate answer script for each part.
PART II
Answer **any five** questions.
Figures in the margin indicate full marks

1. How does the SRAM cell work on one bit data for read-write operation? Explain with proper circuit. (10)

2.(a) Illustrate with relevant circuits the principle of operation of an OR matrix within a PLA device. (6)

(b) Write a program in VHDL to implement an AND gate. (4)

3. Using a suitable example describe the multiplexer based architecture of FPGA logic block. (10)

4. Describe the FAMOS technology adopted in EEPROM. Explain the operation of EEPROM. (10)

5. How does a macrocell add to the versatility of a configurable hardware? Explain with example. (10)

6. What do you understand by bit shift operation? Discuss about different bit shift operations available in VHDL. Consider a bit_vector, A= "101001". Discuss how the command 'A **srl** 2' will be executed. (10)

7. What is a CAD system? Write the advantages of a CAD system. Discuss about the different stages of a CAD system. (10)