Ref No. Ex/EE/ET/T214/2017 (S)

B. ELECTRICAL ENGINEERING 2ND YEAR 1ST SEMESTER SUPPLE EXAMINATION, 2017

ELECTRONICS-II

Time: 3 Hours **Full Marks: 100**

Use separate Answer - Script for each Part

50 marks for each part

PART - I

Answer any **Five (5)** Questions from the followings: 10×5

1. Give the circuit diagram of a ***Wien-bridge oscillator*** using ***OPAMP***. Explain how oscillation principle is satisfied in this circuit? How the frequency of oscillation is determined for such oscillator?

(2+3+5)

2. Explain the operation of ***Monostable multivibrator*** using ***555 IC*** with necessary circuit diagram. Write down expression of expressions of width (W), time period (T), frequency (f) and duty cycle (D) of output waveform.

(3+3+4)

3. Describe with a suitable circuit diagram how a ***transistorized shunt voltage regulator*** provides a stable dc output voltage against the input voltage fluctuation?

(4+6)

4. Give the circuit diagram of IC 7805 voltage regulator. Explain the operation of this circuit.

(4+6)

5. Give the circuit diagram of integrated ***current mirror circuit*** using two ***BJTs***. Clearly explain why this circuit is called the ***current mirror circuit.***

(5+5)

6. What do you meant by constant current sources? Explain with suitable circuit diagram how a ***BJT*** circuit provides a constant current?

(2+3+5)

7. Give the circuit diagram of complementary ***MOSFET (CMOS) NAND*** circuit. Explain how the logic of *NAND* Gate is verified with this circuit.

(5+5)

8. Write short note (any two of the followings): 2×5
   a. Darlinton transistor
   b. Schmitt trigger circuit
   c. TTL circuit
   d. Bootstrap circuit

[Turn over

Ref. No.: EE/ET/T214/2017(S)

B. ELE ENGG. 2ND YEAR 1ST SEMESTER SUPPLE EXAMINATION-2017

Subject: ELECTRONICS – II Time: 3 Hours Full Marks: 100

PART-II

Answer Q.1 and any FOUR from the rest.

All parts of the same question must be answered at one place only.

1.(a) Fill in the blank: $(243.62)_7 = (?)_9$

(b) What is the advantage of Gray code?

(c) Implement XNOR function using minimum number of NOR gates.

3+3+4=10

2. Explain the functionality of a carry look-ahead adder.

10

3. Design a priority encoder and explain its operation

10

4. Design a 4-bit full adder-subtractor circuit.

10

5. Explain the operation of a TTL NAND gate indicating the significance of the totem-pole arrangement.

10

6. Explain how a master-slave configuration helps to eliminate the race-around problem.

10

7. Design a self-correcting 4-bit ring counter.

10

8. Design a 4-bit universal shift register.

10