B. E. ELE. ENGG. 1ST YEAR 2ND SEMESTER EXAM, 2017

ELECTRONICS – I **Time: Three hours** **Full Marks: 100**

Use a separate Answer-Script for each Part (50 marks for each Part)

PART-I

Answer ***Q.1*** and any ***two*** questions from the rest [10+2×20=50]

1. Answer any ***four*** from the following : [4×2$\frac{1}{2}$=10]
   a) Write names of two direct band gap and two indirect band gap semiconductor. Where are they used?
   b) What happens to the avalanche breakdown and Zener breakdown voltages when the temperature is increased?
   c) Write the differences between general purpose p-n junction diode and Schottky diode.
   d) "A BJT is current controlled device and FET is voltage controlled device." Justify.
   e) Define load line and Q- point of transistor amplifier.
   f) Compare CC and CB mode bipolar junction transistor with respect to input impedance, current gain, voltage gain and output impedance.

2. a) Sketch the Fermi Dirac distribution function at absolute zero temperature (0 K), T= 150 K and room temperature (300 K). (Qualitative hand writing) Explain. [3+3]
   b) Show different current components in a p-n junction diode and explain origin of each current component. [6]
   c) Consider a uniformly doped silicon p-n junction with doping concentration $N_A=5x10^{17}cm^{-3}$ in the p region and $N_D=10^{17}cm^{-3}$ in the n region. Calculate the value of V_{bi} (built in potential barrier) at T = 300K. Draw the energy band diagram and calculate the depletion width within p and n regions when a reverse bias of 2 V is applied across the p-n junction. The intrinsic carrier concentration (n_i) is $1.5\times10^{10}\,cm^{-3}$ and bandgap (E_g) =1.2 eVat 300 K. [8]

3. a) Derive the expression and calculate the value for (i) dc load current, (ii) ripple factor and (iii) rectification efficiency of a center tapped full wave rectifier. [12]

b) Draw a positive diode clamper circuit. Explain its operation. [5]

c) A 10 V peak sinusoidal voltage is applied to the input of a positive diode limiter. Draw the circuit with proper bias to limit the output to +5 V. [3]

4. a) Explain the stability of the circuit shown in Fig. 1.(qualitative) [4]

b) Determine stability factor with respect reverse saturation current (S) for Fig. 1. [6]

c)R_1=10 KΩ, R_2=4.6 KΩ, R_C=1 KΩ R_E= 560Ω and β=100 in Fig. 1. Determine the Q point. [5]

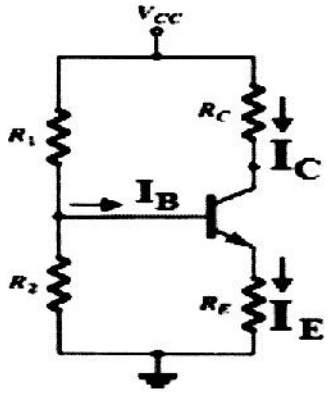

Figure 1

d) With the help of proper diagram explain the pinch-off phenomenon in n-channel JFET. [5]

5. a) Draw and explain the operation of a transformer coupled class A power amplifier. Hence prove that the maximum conversion efficiency of a class A power amplifier is 50 %. [5+5]

b) Define the hybrid parameters for a basic transistor circuit in CE configuration. Determine the h-parameters for CB configuration in terms of h-parameters for CE configuration. [3+7]

No. of questions	**PART- II** Answer **question no. 6** and any **two from the rest**	Marks
6.	Answer ***any five*** questions: a. How the Bandwidth of an amplifier is enhanced due to application of negative feedback? b. How the ***gain*** of an amplifier is more stabilized for application of negative feedback? c. Why positive feedback is not applied for an amplifier? d. Why indirect band gap semiconductors are not used to fabricate a LED? e. How the colour of emitted light from a LED is changed? f. How a buffer amplifier is designed with OPAMP? g. How the slew rate of an OPAMP is measured? h. Define virtual short and virtual ground? i. Why the output of a practical OPAMP is not zero when two equal voltages are applied at the two input terminals.	5x2=10
7.	a) How the amplifier characteristics are changed due to the application of negative feed-back? b) Derive the expressions for lower and upper half power frequencies for an amplifier with negative feedback. Show that lower half power frequency with feedback is less than the lower half power frequency without feedback and upper half power frequency with feedback is greater than the upper half power frequency without feedback. How the frequency distortion of an amplifier is reduced with the application of negative feedback. Sketch the frequency response for an amplifier with and without feedback. c) Determine the voltage gain, input and output impedance for an amplifier with voltage shunt feedback having R_i = 10 KΩ, R_O = 20 KΩ and β = -0.5. d) Draw a circuit for a voltage shunt feedback using BJT and explain how this topology of feedback is occurred in this circuit?	2+(3+3+2+3)+3+4
8.	a) What is the function of comparator? Draw an OPAMP comparator circuit. Explain how an OPAMP comparator circuit generates the square wave output for the sinusoidal input waveform? b) The circuit shown in Fig. 1 has the following parameters: $R_1 = R_2$ = 1 KΩ, $R_F = R_3$ = 10 KΩ. Calculate (i) the gain and input resistance of the amplifier (ii) output voltage if v_x = 2.7 V peak to peak and v_y = 3 V peak to peak sine waves at 100 Hz. Derive the necessary relation you use. c) Design an OPAMP circuit to generate the output voltage is proportional to the	2+2+4+7+5