# BACHELOR OF COMPUTER SC. ENGG. EXAMINATION, 2017

(2nd Year, 1st Semester Supplementary)

**Digital Circuits**

Time : Three hours | Full Marks : 100

Answer any ***five*** questions

1. (a) What is semiconductor? Explain the energy band theory of crystal. In the light of energy band theory, explain semiconductor, metal, insulator.
   (b) Draw the $I_C$ versus $V_{CE}$ curves with respect to different $I_B$ in an npn transistor. Show the active, saturation and cut-off regions.
   (c) Explain the terms $I_{CO}$, $I_{EO}$, $V_{BE}$, $V_T$, $\alpha_N$,$\alpha_I$. Deduce the expression for $I_C$ and $I_E$ for an npn transistor with respect to $I_{CO}$, $I_{EO}$, $V_{BE}$, $V_T$, $\alpha_N$,$\alpha_I$. Deduce the expression for $V_{CE}$(sat) in terms of $V_T$, $h_{FE}$,$h_{FC}$,$\sigma$.

   8+3+9

2. (a) How is the transistor working as a switch?
   (b) Explain - how diode logic can be implemented as an AND gate? What are the problems of Diode logic?
   (c) Explain the current hogging problem in DCTL gate.
   (d) Draw the two inputs OR gate using RTL. Explain its operation.
   (e) What is the output of paralleling RTL gates.

   4+5+4+5+2

3. (a) Draw an IIL gate. What is the advantage of IIL gate? Why is IIL gate called merged-transistor logic?
   (b) With the help of a circuit diagram explain the operation of a DTL gate.
   (c) How is the circuit of DTL modified for Integrated version? What are its advantages over the discrete version?

   6+7+7

4. (a) Draw HTL gate. What is its advantage ?
   (b) Explain the operation of a TTL NAND gate. Compare DTL and TTL.
   (c) Explain the operation of an ECL gate. What is its advantage?

   6+8+6

5. (a) How does CMOS work as an inverter?
   (b) Deduce the pull-up to pull-down impedance ratio of an ideal CMOS inverter..
   (c) An n MOS inverter is driven by another nMOS inverter having pull-up to pull-down ratio of 4.50:1, through 3 pass transistors each having threshold voltage of 0.265 $V_{DD}$. Find the desired ratio of the pull-up to pull-down impedance of the driven inverter.

   4+11+5

6. (a) Explain the operation of the weighted-resistor D/A converter.
   (b) Explain the operation of a R-2R ladder type DAC.
   (c) Explain the operation of a 3 bit direct comparison type ADC.

6+7+7

7. Write short notes on
   (a) Transistor as a switch
   (b) RTL EXOR gate
   (c) NMOS Inverter
   (d) Sample-Hold circuit

4X5