EX/CSE/T/215A/2017(S)

B.CSE 2nd YEAR 1st Semester Supplementary EXAMINATION 2017

Computer Organization

Time : Three Hours | Full Marks : 100

Answer any ***five*** questions

All parts of a question are to be answered together

1a) What are the advantages of using normalized mantissa and biased exponents in floating point representation of binary numbers? What are the IEEE standards for representing floating point numbers ? Represent +1.0125 in both single precision and double precision IEEE formats.

b) Consider a 16-bit floating number with 6-bit exponent (excess 31 format) 9-bit normalized mantissa. The base is of scale factor 2. Find A+B , A-B and represent the results in the above format, use truncation method of rounding.A = 0 100001 111101111 B = 0 011111 011011011
(Consider an implicit 1 to the left of normalized mantissa as in IEEE format.) (10 + 10)

2. Consider the five stage pipelined processor specified by the following reservation table :

	1	2	3	4	5	6
S1	x					x
S2		x			x	
S3			x			
S4				x		
S5		x				

a) List the set of forbidden latencies and the collision vector
b) Draw the state transition diagram
c) List all the simple cycles from the state diagram
d) Identify the greedy cycles among the simple cycles
e) What is minimum average latency ?
f) What is minimum allowed constant cycle for this reservation table ?
g) What will be the maximum throughput if pipeline clock period be 20 micro seconds ?
h) Is the MAL obtained in (e) is the lower bound ? If not, what to do to achieve lowest MAL ? (20)

3. Write a code segment to evaluate the statement A x B + A x {(B x D) + (C x E / (A x F)}

i) Using general register register computer with 3 address instructions
ii) Using general register register computer with 2 address instructions
iii) Using general register register computer with 1 address instructions
iv) Using stack organized computer with 0 address instructions (20)

4a) The memory unit of a computer has 256K words of 32 bit each. The computer has an instruction format with four fields : an opcode field, a mode field to specify one of seven addressing modes, a register address field to specify one of 25 processor registers and memory address. Specify the instruction format and the no. of bits in each field, if each instruction is one memory word long. Also find the total no. of operations that can be performed by the ALU.

b) Design a combinational circuit for adding two BCD numbers. Indicate properly the carry-in and carry-out terminals for cascading. (10 + 10)

5a) Describe Booth's modified algorithm and show that just N/2 partial products are required to multiply two N bit binary numbers. Illustrate the algorithm with the example of multiplication of +29 and -31.

b) Describe Restoring type binary division algorithm and the corresponding sequential circuit for implementing it. Next verify your circuit with the example of 18 divided by 5. (10+10)

6a) Draw the CSA organization to add 8 signed nos. of 5-bit each having CLA at last stage. Count the minimum no of full adders, basic adders and CLCs required for your design. Also calculate the gate delay in your addition process.

b) Design a minimal combinational circuit for multiplying two 4-bit signed binary numbers. Also calculate the gate delay for your circuit. (10+10)

7a) In a certain computer system with cache memory 750 micro sec. is the access time for cache miss and 50 micro sec. is the access time for cache hit. Find the percentage decrease in the effective access time if the hit ratio is increased from 75% to 95%.

b) Consider the following page reference sequence in a two level virtual memory system which uses demand paging and has a memory capacity of four pages.

1,2,3,4,5,1,2,6,1,2,3,4,5,6,5

Which of the page replacement policies FIFO or LRU is more suitable for usein this case ? Give an intuitive justification for your answer. (10+10)

8. Write short notes on :

i)	Carry look-ahead addition	ii)	Non-restoring division	
iii)	Associative memory	iv)	Series parallel adder	(4x5 = 20)