Ref No.: Ex/CSE/T/225A/2017

B.E.Computer Science and Engineering 2nd Yr 2nd Semester Exam-2017

COMPUTER ARCHITECTURE

Time: Three Hours **Full Marks:100**

Group-A

Match the correct pairs. 13×1=13

Set-I	Set-II
1.Backpressure	(i) 16-bits
2.B0..B77	(ii) 64-bits
3. Crossbar	(iii) bandwidth and storage allocation
4. Flit	(iv) bus watching
5. JMP	(v) flow control
6. Maximum length of a phit	(vi) multiplexers
7. MIPS floating-point unit	(vii) register renaming
8. Packet	(viii) reservation station
9.Parcel	(ix) RI and SN
10. SAL	(x) state
11. Snoopy Protocols	(xi) subroutine linkage
12. Virtual channel	(xii) U-pipeline
13. WAR	(xiii) V-pipeline

Group-B

Answer eighteen(18) questions 18×4=72

Choose the unique correct answer.

14. Consider the following instruction sequence executed on a 5-stage pipeline (IF,ID,EX,MEM,WB):

```
lw   $s0, 20($t1)
sub  $t2, $s0, $t3
```

If 'lw' is initiated (IF-stage) in cycle-1, 'sub'

(a) can never be initiated before cycle-4
(b) can be initiated in cycle-2
(c) can be initiated in cycle-3
(d) must be initiated in cycle-5

For Q15..Q18

Consider the following instruction sequence executed on a 5-stage pipeline IM,Reg,EX,DM,Reg).

```
lw    $2,20($1)
and   $4,$2,$5
or    $8,$2,$6
add   $9,$4,$2
```

Instruction 'lw' is initiated (IM-stage) in cycle-1.

15. 'or' executes in Reg-stage (before EX) in

(a) cycle-4
(b) cycle-5
(c) cycle-6
(d) cycle-7

16.'and' executes Reg-stage (before EX) in

(a) cycle-3
(b) cycle-4
(c) cycle-5
(d) both cycle-3 and cycle-4

17. A bubble is inserted into the pipeline in
(a) cycle-3
(b) cycle-4
(c) cycle-5
(d) cycle-6

18. The 'add' instruction receives its input $4 (during EX-stage)
(a) by reading $4 already written into by 'and'
(b) fron DM-stage of 'and' by forwarding
(c) from Reg-stage of 'and' by forwarding
(d) in cycle-8 because 'and' has finished

For Q19..Q21

A pipeline with floating-point operations has the following latencies:

Instruction producing Result	Instruction using result	Latency in clock cycles
FP ALU op	Another FP ALU op	3
FP ALU op	Store double	2
Load double	FP ALU op	1
Load double	Store double	0

Consider the following program for adding a scalar to each element of a 1000-element array:

```
Loop: L.D      F0,0(R1)    ; F0 = array element
      ADD.D    F4,F0,F2    ; add scalar in F2
      S.D      F4,0(R1)    ;store result
      DADDUI   R1,R1,#-8   ;decrement pointer 8 bytes (per DW)
      BNE      R1,R2,Loop
```

The first instruction, i.e., "L.D" is issued in cycle-1. Now consider the first (initial) iteration of the loop.

19. "S.D" is issued in
(a) cycle-3
(b) cycle-4
(c) cycle-5
(d) cycle-6

20. "ADD.D" is issued in
(a) cycle-2
(b) cycle-3
(c) cycle-4
(d) cycle-5

21. "DADDUI" is issued in
(a) cycle-5
(b) cycle-6
(c) cycle-7
(d) cycle-8

For Q22..Q24

Consider the following Cray X-Mp program with vector-chaining.

Line	Instruction	
1	A1	10
2	VL	A1
3	V4	V3+FV2
4	V5	V4*FV7

Line-1 is issued in cycle-1.

22. Line-4 begins execution in
(a) cycle-13
(b) cycle-14
(c) cycle-15
(d) none of the above

23. The first result of line-3 emerges from the pipeline after
(a) cycle-11
(b) cycle-12
(c) cycle-13
(d) cycle-14

24. The last result of line-4 emerges at the end of
(a) cycle-30
(b) cycle-31
(c) cycle-32
(d) none of the above

For Q25..Q27
Consider the MSI Protocol for cache coherence.

25. The current state is S. If the controller observes a PrWr event, the next state
(a) becomes M
(b) remains S
(c) becomes I
(d) it is impossible for such an event to occur in state S

26. The current state is S. If the controller observes a BusRsX event,the next state
(a) remains S
(b) becomes I
(c) becomes M
(d) none of the above

27. The current state is I. If the controller observes a PrRd event, the next state
(a) remains I
(b) becomes M
(c) becomes S
(d) it is impossible for such an event to occur in state I

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28. Resources are allocated to packets and not messages because
(a) messages are platform-dependent
(b) packets specify the resources they need
(c) messages are transferred in asynchronous mode
(d) packets have a restricted maximum length

29. A multiprocessor in which all caches form a global address space, i.e. there is no memory hierarchy at each processor node is
(a) COMA
(b) NUMA
(c) UMA
(d) CC-NUMA

30. In decentralized rotating arbiter scheme,
(a) a master must use the bus when its turn comes even if it doesn't need to
(b) the master that releases the bus has the lowest priority
(c) there is no fairness
(d) all of the above

31. A flit is subdivided into one or more
(a) packets
(b) messages
(c) phits
(d) buffers

32. Virtual channel flow control
(a) is less efficient than wormhole flow control
(b) associates several virtual channels with a single physical channel
(c) associates a single virtual channel with several physical channels
(d) none of the above

33. Message passing achieves
(a) communication
(b) synchronization
(c) both communication and synchronization
(d) none of the above

34. When the arbiter activates the grant line in centralized arbitration of a shared bus, the requestor
(a) activates its request line
(b) activates the bus busy line
(c) deactivates its grant line
(d) deactivates the bus busy line

35.In a daisy-chained grant scheme for bus-arbitration
(a) the master closer to the arbiter has higher priority
(b) the master farther from the arbiter has higher priority
(c) priority has no relation with position in the chain
(d) priorities are decided by dynamic voting

36. If a node in a scalable multiprocessor incurs a miss on a read of a block which is in dirty state, it
(a) reads the block from the directory
(b) reads the block from the owner node
(c) reads the block from the home node
(d) encounters a trap due to memory protection violation

Group-C

37. A processor has a five-stage pipeline: IF (fetch), ID (decode), RR (read registers), EX (execute), WB (write results back into registers). An instruction is said to have issued when it passes from the RR stage to the EX stage. The latency between an instruction I_1, and an instruction I_2 dependent on I_1, is the time-delay (cycles) between their issue cycles. If I_1 is an arithmetic operation, the latency is three(3) cycles because the RR stage of I_2 follows the WB stage of I_1.

Now consider the following instruction sequence:

```
------------------------
ADD     r3,r4,r5
SUB     r7,r3,r9
MUL     r8,r9,r10
SAL     r4,r8,r12
------------------------
```

What is the execution time (in cycles) ? [Bypassing(forwarding) is NOT ALLOWED]. 15

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