Ref. No.: **EX/CSE/T/115A/2017(S)**

B.C.S.E. 1st Year, 1st Semester Supplementary Examination, 2017
Digital Logic

Full Marks: 100 Time : 3 Hr

Answer Five Questions : Answer any five.
Write answers to the point and state all the assumptions (wherever required).
ALL PARTS OF THE QUESTION SHOULD BE ANSWERED TOGETHER

Q 1) (a) An engine has 4 fail-safe sensors. The engine should keep running unless any of the following conditions arise: (2+4+4)

* If sensor 2 is activated.
* If sensor 1 and sensor 3 are activated at the same time.
* If sensor 2 and sensor 3 are activated at the same time.
* If sensors 1, 3, 4 are activated at the same time.

(i) Derive the truth table for this system.

(ii) Design, using Karnaugh Map techniques, a minimum AND-OR gate network for this system. Draw the resulting digital circuit diagram.

(iii) Design, a digital circuit that will implement the above minimal AND-OR gate network using NOR gates only. Assume that each logic gate can have any number of inputs and that inverted inputs are available.

(b) Explain the operation of a JK flip-flop. How does it differ from an RS flip-flop? What are the limitations of a JK flip-flop? (4+3+3)

Q 2) (a) Make a K-Map for the following function:
$f = AB + A\overline{C} + C + AD + A\overline{B}C + ABC$ (10)

(b) A multiplier circuit takes two 2-bit binary numbers y_1y_0 and x_1x_0 and produces an output number $z_3z_2z_1z_0$ that is equal to the arithmetic product of the two input numbers. Design the logic circuit for multiplier. (10)

Q 3) (a) Convert an S-R flip-flop to J-K flip-flop. (5)

(b) Design a 3 bit binary DOWN counter. (10)

(c) Write short notes on any two: (2.5 × 2)

(i) Encoders and Decoders

(ii) Shift Registers

(iii) Multiplexer and Demultiplexer

(iv) Flip-flops

Q 4) (a) Solve the following using Quine-McCluskey Method (10)

$$F(A, B, C, D) = \Sigma(23, 7, 9, 11, 13) + \Sigma\phi(1, 10, 15)$$

(b) Prove the rule of Boolean algebra: $(A + B)(A + C) = A + BC$ (4)

(c) Represent $(27)_{10}$ in binary form using : $(2 \times 3 = 6)$
(i) BCD Code (ii) Excess-3 Code (iii) Gray Code

Q 5) (a) Do the following $(3 + 3 + 2 + 2 = 10)$

(i) Convert the following $(111011101)_2$ to octal, decimal and hexadecimal format

(ii) Convert the following decimal number, $(3479)_{10}$ to binary, octal and hexadecimal formats

(iii) Perform the following addition: $(BCD)_{16} + (A34)_{16}$

(iv) Perform the following subtraction using two's complement $(1101011)_2 - (111010)_2$

(b) State the logic circuit, truth table and derive the equivalent logic expression from the truth table of the following Boolean expression $Y = A\overline{B} + \overline{B}C$
$(3 + 4 + 3 = 10)$

Q 6) (a) Design the full subtractor using NAND gates only. (5)

(b) Explain the working of bi-directional shift registers. (5)

(c) Realise the function with the help of NAND gates: (5)

$$f(A, B, C, D) = \Sigma(0, 1, 4, 6, 9, 12, 15) + \phi(2, 3, 6)$$

(d) (i) Convert the following 29_{16} to binary. Show each step clearly. (2)

(ii) Perform the following: $411 - 332$ using 9's complement Binary Coded Decimal (BCD) subtraction. (3)

Q 7) (a) Design a MOD-6 **synchronous counter** using J-K Flip-Flops. (10)

(b) Design a digital circuit for generating a sequence $1 - 1 - 2 - 3 - 5 - 7 - 1 - 1 - 2 \ldots$
(10)